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Photovoltaic CdHgTe - silicon hybrid focal planes

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Abstract

Photovoltaic C.M.T.-Si hybrids have been demonstrated in a number of array configurations from 32 x 1 to 64 x 64. The photodiode and hybrid interconnection technology is based on the loophole technique, which has the main advantages of high density and therefore good material utilisation in two dimensional arrays. For linear arrays, the CCD multiplexer is suitable for most applications. For two-dimensional arrays, however, the co-ordinate addressed array may offer significant benefit over the CCD particularly at long wavelength. 32 x 32 arrays of both types have been fabricated. A co-ordinate addressed array of 11.4μm cut-off produced an NETD of < 0.1K in an imaging demonstration.

Introduction

Many future infrared systems will use multiplexed linear or two-dimensional arrays. The incorporation of multiplexing circuitry on the focal plane results in reduced encapsulation size and cost. It also provides a capability to fabricate and scan large, high density arrays for staring applications.

The specialised nature of many applications often calls for a custom design approach, particularly with regard to the array format and infrared cut-off wavelength. The best design philosophy, then, is the hybrid approach where the infrared sensitive material and the readout electronics are optimised independently and combined using an appropriate interconnect technology. The CdHgTe diode array technology described in Section 2 meets this requirement, in that it is applicable to a wide range of cut-off wavelengths, array formats and silicon multiplexers.

For linear arrays, CCDs are suitable for the whole range of cut-off wavelengths. However, the situation is less straightforward for two-dimensional arrays, and at longer wavelengths the co-ordinate addressed array has many advantages. Section 3 describes the issues relating to the choice of two-dimensional multiplexer, and research on two devices, a 32 x 32 CCD and RALSA, a random access co-ordinate addressed array, is described subsequently.

2. Hybrid technology

There are two main approaches to the fabrication of silicon-C.M.T. hybrids. The most commonly reported (References 1 and 2) is the indium bump interconnect. This is a useful technique for fairly widely spaced arrays, but there are mechanical problems at interelement pitches of 40μm or less. Also, there is some evidence that the mechanical stresses involved in the bonding process can impair the performance of long wavelength detectors, and in general the extra C.M.T. handling processes are not conducive to long material lifetimes (Reference 3). 32 x 32 hybrids have been fabricated successfully using indium bumping as a comparative exercise, but the manufacturability does not compare favourably with alternative techniques. For certain technologies, however, this approach is the only practical one.

The second technology is often known as the metal strap interconnect. The diodes are joined using a metal track which connects the top of each diode to a pad on the silicon integrated circuit. The general approach is to use the silicon chip as a substrate for the manufacture of the diode array and interconnection. The C.M.T. handling is minimised, and the processes are well established. The main technical problem is that the interconnection metallisation and the gaps in the C.M.T. monolith next to each diode consume area that would otherwise be photosensitive. Therefore the focal plane obscuration is much higher than with indium bumped arrays.

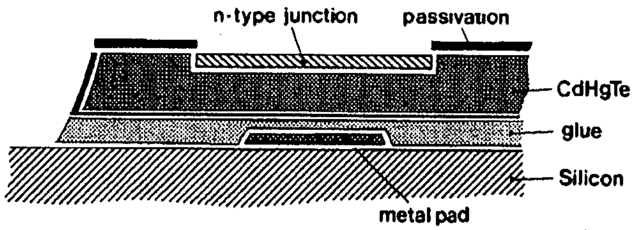

Figure 1a
Formation of planar junction

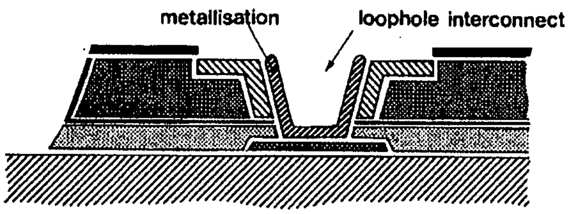

Figure 1b

Hybrid interconnect
for planar junction

Stages in manufacture of loophole-interconnected diode array

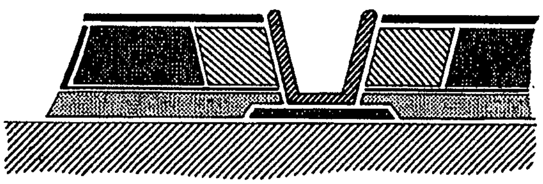

Figure 1c

Simple loophole diode for close-packed arrays

Figure 1. Schematic of hybrid technology

A process which has all the advantages of the metal strap interconnect but an obscuration of only 5% on a 40μm pitched array has been devised. The diodes have a unique structure and have been named loophole diodes. The loophole technology is illustrated in Figure 1. The silicon integrated circuit is prepared with alignment features for the CdHgTe monolith and subsequent masking stages. The metallisation is a titanium-platinum-gold multilayer which gives better resistance to the chemical and mechanical side effects of the hybrid process. With reference to Figure 1a, the CdHgTe monolith is polished to a flatness and parallelism of <1μm, passivated on both sides and bonded to the silicon chip.

Using the chip as a substrate, a matrix of junctions is ion implanted or diffused into the 'p'-type monolith. The junctions are then individually connected to the underlying pads on the silicon by cutting 10μm diameter holes through the junctions, doping the exposed CdHgTe in each hole and backfilling with metallisation, (Figure 1b). In high density, two-dimensional arrays the first diffusion stage may be omitted and the loophole diffusion driven deeper so that photosensitivity is achieved by lateral collection to a cylindrical junction (Figure 1c). Finally an ohmic contact is made to the 'p' monolith to complete the structure.

The main advantage of the loophole technique is that it requires just one masking stage to achieve a junction and interconnection to the silicon. Also the structure is thermally and mechanically stable, and the connection yield is high, currently 99.8%. Research has resulted in a good phenomenological understanding of diffusion in 'p'-type CdHgTe for array fabrication.

The single diffusion technology, such as that illustrated in Figure 1c, is usually adopted and in this case, the sensitive area is an annulus centred on the circular junction. The dimensions of the annulus depend upon the diffusion lengths of minority carriers in both the 'p' and 'n' regions. In practice these diffusion lengths fall into the range 5-10μm for 10-12μm cut-off wavelength material. A natural choice of pitch for two-dimensional arrays of loopholes is about 40μm. At this value both the crosstalk and the dead space between elements are minimised. Figure 2 shows a scanning electron microscope photograph of a 10μm diameter loophole interconnect.

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