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Fixed-Pattern Noise in Photomatrices

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Abstract—Two MOS photomatrix configurations, voltage sampling and recharge sampling, have been compared with regard to sources of fixed-pattern noise (FPN). Voltage sampling provides a high-amplitude low-impedance photosignal, with FPN primarily due to threshold variation in the amplifying MOST at each element. Recharge sampling is used for large high-yield rapidly scanned arrays, with FPN caused mostly by variations in spurious capacitive breakthrough. Production peak-to-peak signal to FPN ratios are 20:1 for voltage sampling and 50:1 for recharge sampling.

Introduction

VARIOUS photomatrices have been under development for the past 5–7 years [1]–[6]. Until recently they have formed the basis of considerable research and development programs but, with the exception of the electron-beam-scanned array [7], have not been applied to real environments such as steel mills, computer peripherals, etc.

However, with many teams actively applying photomatrices to pattern recognition, especially optical character recognition, measurement, position sensing, edge sensing, etc., the authors consider that the time has come to define various relevant parameters of signals that are obtained from such arrays, with particular regard to the signal-to-noise ratios (SNR) obtained. This paper attempts to classify the sources of noise present in some forms of photodiode arrays with integral MOS switching and amplification that are currently being manufactured.[1]

We would suggest that the following standard nomenclature be adopted to simplify future correspondence.

1) Video Window (VW): Peak-to-peak signal obtainable from an array, or the output swing between dark and overload conditions.

2) Fixed-Pattern Noise (FPN): Peak-to-peak output signal of a fixed pattern nature, obtained under uniform (or zero) illumination of all photodiodes.

3) Signal-to-Noise Ratio (SNR): The VW/FPN ratio VW/FPN.

It is not intended in this paper to dwell on the various external (or internal) methods of reducing FPN. It is sufficient to say that FPN has been reduced by the authors to <1 mV giving SNR of 10 000:1. However, this involves a complex array and external circuitry. It is also acknowledged that, with the recharge array, virtually all switching spikes can be eliminated by signal processing. The point of this paper, however, is to show that acceptable video signals can be obtained by relatively simple arrays, with high yield for production purposes.

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[1] For example, IPL 20, a 50 × 1 array with integral scanning, Integrated Photomatrix, Ltd.

Voltage Sampling

The basic element of one major type of photodiode array is illustrated in Fig. 1. This consists of the photodiode D, the recharging switch M_1, amplifying transistor M_2 and output switch M_3. This is the typical format for a voltage-sampled element of an array. The array is scanned by means of an MOS shift register/ring counter providing sequential switching pulses to lines n and $n + 1$. The operation is such that when $n + 1$ is switched, the diode capacitance C_D is charged to a negative potential V_{DC}. The remaining diodes in the array are then charged sequentially until line n is switched. This turns M_3 on thus providing a current path via M_2, M_3, and R_L and giving rise to a voltage V_{out} across R_L. R_L is common to the entire array and is generally external. Ideally V_{out} should bear a linear relationship to incident illumination integrated over a scan period. Whereas all voltages referred to are negative relative to earth, this has been ignored in order to simplify the presentation. Where necessary, sign reversals are used, but the conclusions are still valid since differences in voltage (signal) are derived.

$$V_{out} = M(V_{DT} + K)$$

$$V_{DT} = V_{DC} - V_s$$

$$V_s = \text{constant} \times \int_{t_1}^{t_2} P\,dt = P\,\Delta t$$

for steady illumination where V_{DT} is diode voltage after discharge due to illumination, V_s is voltage through which the diode has decayed, P is light incident power at time t, $\Delta t = t_2 - t_1$ the integration period, M is the gain, and K the offset of the amplifying circuitry to the left of point X.

However, in practice various mechanisms give rise to errors that vary in random fashion over the array. These random errors set a lower limit to the light-intensity change required to obtain a meaningful change in output signal. Since they are a form of spatial noise that is fixed in position for any given array, they are given the name fixed-pattern noise (FPN). In the above, they correspond to variation in the constants V_{DC}, K, and M, and in the coefficient of $P\Delta t$.

A. Diode-Charging Level V_{DC}

The diode will charge to a voltage dependent on the negative-rail voltage V_{DD} and the switching voltage V_L on the gate of M_1. If $V_L < V_{DD} + V_{T1}$ then $V_{DC'} =$

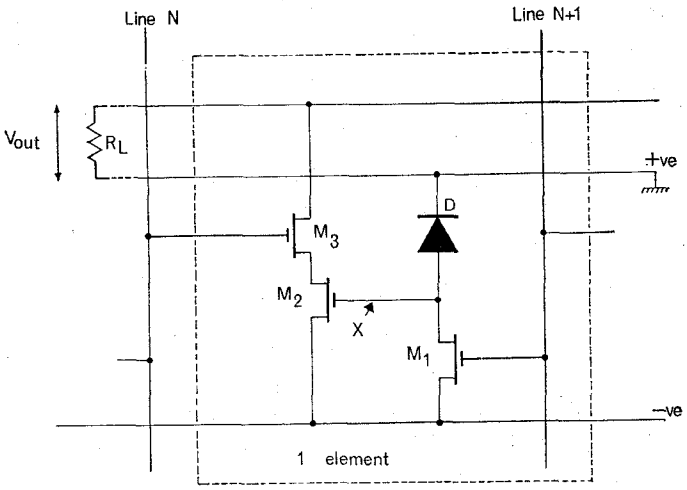

Fig. 1. Basic element.

$V_L - V_{T1}$ where V_{T1} is the threshold voltage of M_1 (which is dependent on source/substrate bias) and $V_{DC'}$ is the voltage attained by D while M_1 is on. When M_1 is switched off as its gate voltage rises towards 0 volts, a positive voltage step is added to $V_{DC'}$ due to the gate–source capacitance C_{GS} of M_1.

Given that the gate voltage of M_1 rises by $\Delta V_L \simeq V_L$, and that the photodiode capacitance is C_D (assumed constant as a first approximation), the step in voltage on the diode is approximately

$$\frac{\Delta V_L\, C_{GS}}{C_D + C_{GS}} \simeq \frac{\Delta V_L\, C_{GS}}{C_D}.$$

The final diode-charging voltage is therefore,

$$V_{DC} \simeq V_{DC'} - \Delta V_L(C_{GS}/C_D).$$

Two sources of FPN affect the value of V_{DC}. 1) V_{T1} is not constant across the array. This is represented by a term ΔV_{T1} in the following equation. 2) The ratio C_{GS}/C_D will vary across the array, mainly owing to variations in C_{GS}, which is affected by gate–source alignment, gate metallization etching accuracy, etc. This is represented by the term ΔC_{GS}.

The final diode-charging voltage now becomes

$$V_{DC} = V_L - (V_{T1} + \Delta V_{T1}) - V_L \frac{(C_{GS} + \Delta C_{GS})}{C_D}.$$

In practice $\Delta V_{T_1} \leq \pm 0.3$ volt and $V_{DC'} \simeq 18$ volts, giving a 30:1 ratio of maximum signal peak-to-peak FPN due to ΔV_{T1}. A voltage drop of about 6 volts in the following circuitry limits the final output swing to 12 volts, reducing this ratio to 20:1. If $V_L > V_{DD} + V_{T1}$, then $V_{DC'} = V_{DD}$ and $V_{DC} = V_{DD} - V_L/C_D\ (C_{GS} + \Delta C_{GS})$.

The first source of FPN is now eliminated; the second is still present, and so great care must be taken in design to ensure that $\Delta C_{GS}/C_D$ is minimized, bearing in mind the effects of mask alignment, etch undercutting, etc. A typical ratio obtained by the authors for this mode of operation is 100:1, which is quite acceptable for most purposes.

B. Voltage Drop Caused by Illumination V_s

For simplicity let us assume that C_D is independent of voltage. The photocurrent in the diode I_p is given by

$$I_p = \int_0^\infty A\eta\lambda KP\, d\lambda = AK \int_0^\infty \eta\lambda P\, d\lambda$$

where A is the diode area, η is the quantum efficiency at wavelength λ, P is the irradiant power per unit area per unit wavelength, $K = e/hc = 8.05 \times 10^3 A\ \mathrm{W^{-1}\cdot cm^{-1}}$.

$$\frac{I_p + I_D}{C_D} = \frac{dV}{dt}$$

Therefore,

$$V_s = \frac{T}{C_D}(I_p + I_D)$$

where I_D is the diode dark current and T is the integration period. Now $C_D = AC_A$, where C_A is the diode junction capacitance per unit area and so we can eliminate area from the above equation to give

$$V_s = T/C_A\left(K \int_0^\infty \eta\lambda P\, d\lambda + I_{DA}\right)$$

where I_{DA} is the dark current per unit area.

Significant errors between one diode of the array and the next occur in I_{DA} and η, and possibly C_A. The effect of I_{DA} on FPN is roughly inversely proportional to the photocurrent; the dark current level is typically equivalent to incident radiation of $<10^{-7}\ \mathrm{W\cdot cm^{-2}}$ (black body radiation at 2900°K), and variations are of the same order, so that by operating in excess of $10^{-5}\ \mathrm{W\cdot cm^{-2}}$ of light FPN will be <1 percent of signal. These figures refer to room-temperature (20°C) operation. I_{DA} increases by a factor 10 with every 30°C rise in temperature.

Variations in η and C_A account for less than 1 percent of signal-to-FPN ratio in diodes 75 microns square. Statistical considerations show that these effects decrease with an increase in diode area.

C. Offset in the Amplifier Circuit K

Let us assume that M_3, when on, is a resistor of value R_{on}. The source voltage of M_2, V_R is given by

$$(V_G - V_{T2} - V_R)^2 = \frac{2V_R}{\beta(R_{on} + R_L)}$$

where V_G is the gate voltage of $M_2(V_G = V_{DC} - V_s)$, V_{T2} is the threshold voltage of M_2 (including the effect of source/substrate bias), β is the gain factor of M_2, and R_L is the common load resistor.

We will, for the present, assume the gain of this source–follower circuit to be unity, i.e., $\beta(R_{on} + R_L) \to \infty$.

Hence $V_R = V_G - V_{T2}$ or, including a term ΔV_{T2} to represent the random variations in V_{T2},

$$V_R = V_G - (V_{T2} + \Delta V_{T2}).$$

The circuit output voltage V_{out} across R_L is given by

$$V_{out} = (V_R R_L)/(R_L + R_{on}).$$

We include variations (ΔR_{on}) in R_{on}, due to threshold voltage and gain factor variations in M_3, so that

$$V_{out} = (V_G - V_{T2} - \Delta V_{T2})\left(\frac{R_L}{R_L + R_{on} + \Delta R_{on}}\right).$$

The term in the first bracket has a typical value given by

$$\begin{aligned} V_G &= 18 \text{ volts} \\ V_{T2} &= 5 \text{ volts} \\ \Delta V_{T2} &= \pm 0.3 \text{ volts} \end{aligned}$$

so that the peak signal/FPN ratio $\simeq 20$ due to ΔV_{T2} alone.

The term in the second bracket is affected by the designed ratio of R_{on} to R_L. ΔR_{on} has a worst case value $\pm 0.1\ R_{on}$. Thus, if we design R_{on} to be less than $0.1\ R_L$, the variation in this term will be less than 2 percent of value.

D. Gain M of the Amplifier Circuit

In the above calculation of amplifier offset, we assumed $\beta(R_{on} + R_L) \to \infty$, making the source–follower gain unity. In fact, if we calculate the relationship between V_R and V_G from simple MOS theory, we obtain:

$$V_R = V_G - V_{T2} + \frac{1}{\beta(R_{on} + R_L)} - \sqrt{\frac{1}{\beta^2(R_{on} + R_L)^2} + \frac{2(V_G - V_{T2})}{\beta(R_{on} + R_L)}}$$

and

$$\frac{dV_R}{dV_G} = 1 - \frac{1}{\sqrt{1 + 2(V_G - V_{T2})\beta(R_{on} + R_L)}}.$$

The errors in this gain due to ΔV_{T2} and ΔR_{on} are dependent on the magnitude of the second term. Putting in typical values:

$$\begin{aligned} \beta &= 32\ \mu\text{A/V}^2 \\ R_{on} &= 5\ \text{k}\Omega \\ R_L &= 200\ \text{k}\Omega \\ V_G &= 10 \text{ volts} \\ V_{T2} &= 5 \text{ volts} \end{aligned}$$

$$\frac{dV_R}{dV_G} = 1 - (1/\sqrt{65}) = 0.876.$$

A $\pm$ 0.3 volt change in V_{T2} will change this by less than 0.6 percent. Changes in R_{on} will have negligible effect. The overall gain M is given by

$$M = \frac{dV_R}{dV_G}\frac{R_L}{R_L + R_{on}} = \frac{dV_{out}}{dV_G}.$$

This is affected by R_{on} in the same way as discussed under amplifier offset, giving a 2 percent peak signal to FPN ratio when $R_{on}/R_L = 0.1$.

Summarizing the above, we conclude that, given suitable design optimization one of the main limitations in terms of FPN is due to threshold voltage variations in the amplifying MOST M_2. This assumes extreme care in the design and manufacture to limit capacity coupling effects.

Comparison of Theoretical FPN With Practical Results

The basic element shown in Fig. 1 has been used in the 50 × 1 array now in full production by the authors' company (Fig. 2).[1] Typical figures established from over 1000 arrays are as follows, with scan rates from 10 kHz to 1 MHz.

	Typical	Best	
Peak video signal	12	14 volts	(with −22 volts applied to array)
Peak-to-peak FPN	±0.3	±0.1 volt	
SNR	20	70	

It can be seen that photomatrices can be readily made with SNR of 20 or more using the voltage-sampling technique.

Fig. 3 shows an oscilloscope trace of a 50 × 1 video output. Diodes 1–25 show response to a circle of light of graded intensity imaged onto half of the array. The remaining portion of the video trace shows the FPN peculiar to diodes 26–50 of this array. Perhaps it is worth noting that this array is 228 × 42 mils and typically gives production yields in excess of 30 percent at probe test. It is now in use in OCR equipment as well as measurement, edge sensing, and inspection.

Recharge Sampling

If high (>5 MHz) scanning rates and large arrays are required, it is often preferable to make use of the recharge-sampling technique. The circuit for this comprises M_1 and D only of Fig. 1 (see Fig. 4). The negative rail is taken to a "virtual negative" amplifier input (i.e., a "virtual earth" with negative offset), and the charge necessary to reinstate the bias on the diode is the signal taken as the video output. Different noise conditions prevail.

A. Diode Area and Quantum Efficiency Effects

We are now measuring the charge, and not voltage; thus diode area becomes significant. Again

$$I_p = AK \int_0^\infty \eta\lambda P\, d\lambda.$$

Let

$$K \int_0^\infty \eta\lambda P\, d\lambda = B.$$

Therefore,

$$I_p = AB.$$

The total charge lost by the diode in period T is

$$Q = (I_p + I_s)T = (AB + I_s)T$$

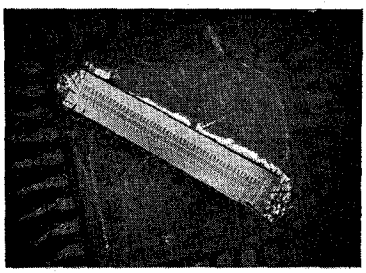

Fig. 2. Self-scanned array.

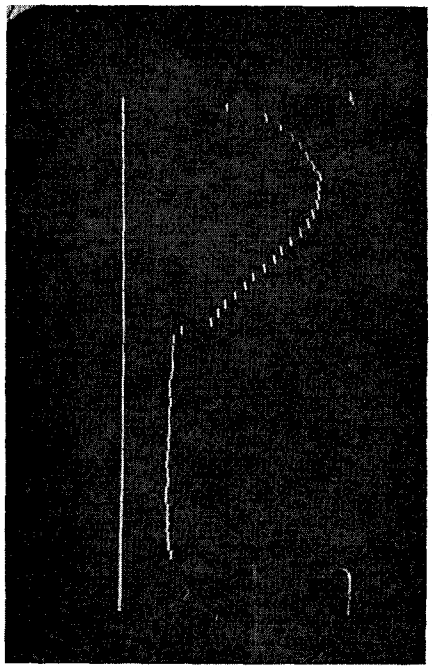

Fig. 3. Video output waveform.

I_D may be ignored since the main use of this technique is for high-speed sampling at high light level although low-speed applications do exist [9]. Therefore, $Q_s = ABT$.

Unlike the voltage-sampling system, the diode capacitance does not enter this equation; diode area does, however. Variations in B due to quantum efficiency η variations cannot be differentiated from variations in A.

B. Capacitive Charge Breakthrough

The gate–source capacitance of M_1 will again transfer charge to the diode when the gate goes positive at the end of the recharge pulse. An equal charge is, however, removed by the negative edge at the beginning of the next recharge pulse. No net charge is passed to the amplifier by this effect.

The gain–drain capacitance of M_1 will, however, transfer a charge spike to the amplifier superimposed on the recharge signal at the beginning of the recharge pulse. Again an equal opposite charge spike occurs at the end of the cycle, superimposed on the signal and charge spike from the next array element. The net effect of the two opposing edges is to cancel the contribution due to C_{DG} (the nominal capacitance) but to leave that due to ΔC_{DG}

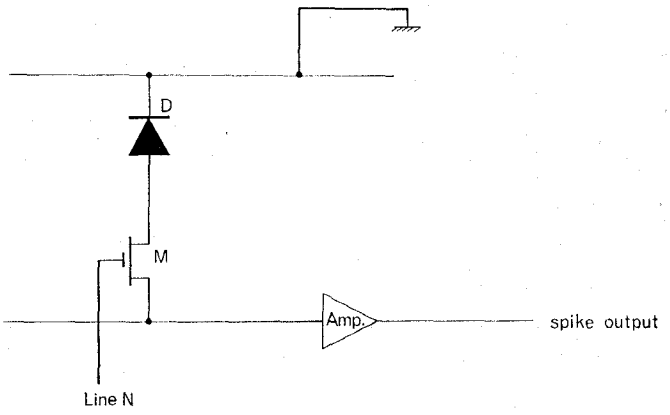

Fig. 4.

charge injected	$V_L(C_{DG} \pm \Delta C_{DG})$
charge removed	$V_L(C_{DG} \pm \Delta C_{DG})$
net charge (FPN)	$\pm 2V_L\ \Delta C_{DG}$.

Since capacitive breakthrough is independent of diode area A, and area variation is roughly proportional to diode perimeter, it is apparent that A must be maximized for best results.

The 50 × 1 array mentioned previously has also been used in the recharge mode and gives a typical peak signal/FPN ratio of 70:1. Therefore, it is obvious that for best results the recharge principle is the best for most applications such as OCR. At present an array, based on the recharge technique, is being made for a particular OCR requirement. This has 5 parallel output lines of over 70 serially scanned diodes (i.e., over 350 diodes in all). At present this device is in preproduction, but first samples are giving good SNR with scan rates of 5 MHz. Yield is such that 10–30 arrays 100 × 400 mils are being obtained at probe test from 2-inch slices. A new technique has been adopted for making this array in that the scanning and array are processed on separate slices and interconnected at assembly. The array is an infinite array 100-mils wide by 2 inches. Diodes are on 4-mil centers. The whole slice is probed in sections of 6 × 5 diodes and faulty sections marked by the prober. Then blocks of the correct size are cut from the slice. It is not unusual for flawless blocks up to 1 inch (250 diodes) in length to be found. Results are encouraging for photomatrices now in design, which include 32 × 32 arrays.

Conclusions

The basic conclusion that the authors draw from the foregoing is that by careful design and selection of the most appropriate methods of scanning, acceptable SNR can be achieved without recourse to excessive external signal processing.

The voltage-sampling technique gives consistent SNR of 20:1 and 35:1 and can be selected at about 10–15 percent of production level. This is adequate for all OCR and most measurement systems of which the authors have knowledge. The recharge technique is more applicable to

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