Kodak SV9600 Still Video Transceiver

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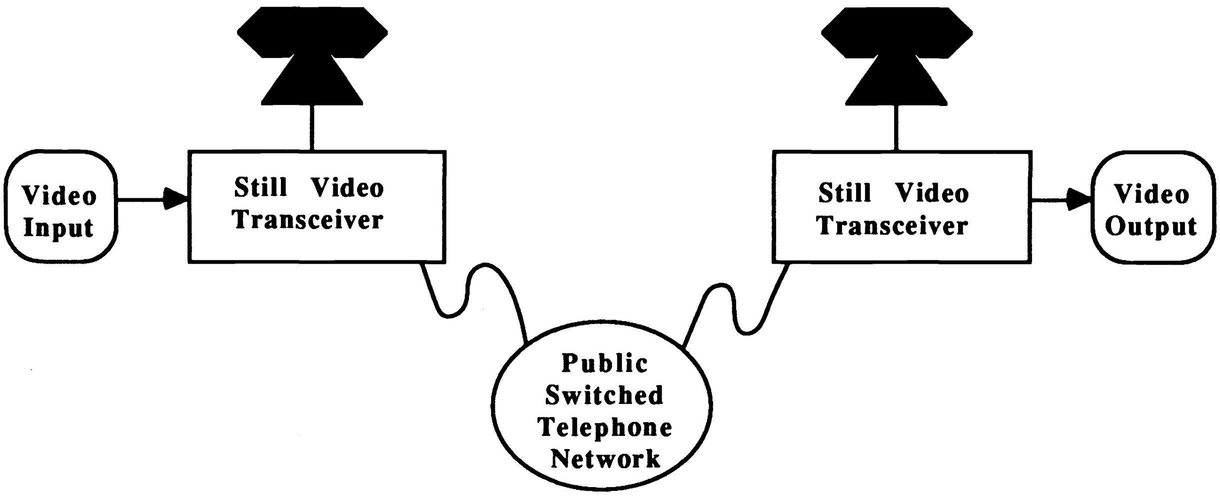
ABSTRACT

The Kodak SV9600 Still Video Transceiver is designed to electronically transmit and receive high quality video images over standard telephone lines. The transceiver captures a full frame of video, digitizes and stores it in memory for manipulation and display of the image data. The data is compressed using a highly sophisticated algorithm developed at Kodak. The compressed image data is transferred to a built-in modem for high-speed communication over standard telephone lines.

1) SYSTEM CONCEPT

The objective of the Kodak SV9600 Still Video Transceiver is to develop and market a system for electronically transmitting and receiving NTSC-quality color video images using the public dial-up telephone network.



The input to the system can be any source of NTSC composite or RGB video in still or motion form. The output from the system can be connected to any device that accepts NTSC composite or RGB video.

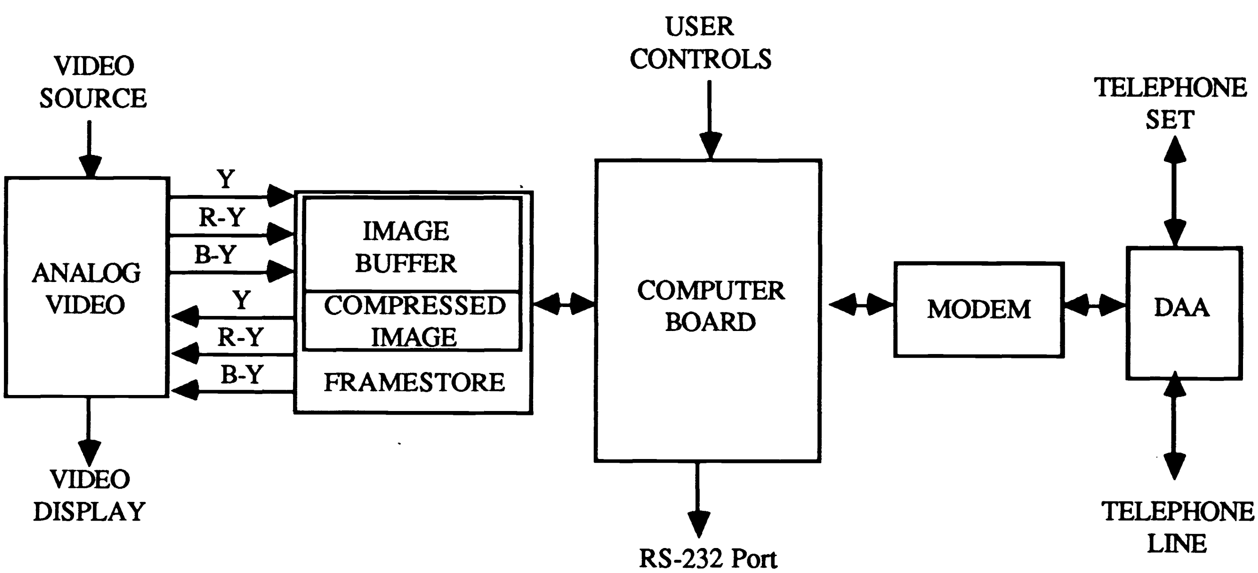
The transceiver captures a full frame of video and stores it in digital form in memory for purposes of manipulation and display of the image data. This data is then compressed using highly sophisticated image compression techniques to minimize the transmission time and storage requirements. The compressed data is then transmitted via a high-speed modem to another transceiver over standard voice-grade dial-up telephone lines. At the receiving transceiver, the compressed image is expanded and converted back to an analog video signal for display on a video monitor.

2) PRODUCT SPECIFICATIONS

* The image compression/expansion algorithm allows transmission of continuous-tone color video images over normal dial-up telephone lines in less than 1 minute.
* Preview mode provides a color image in about 10 seconds for immediate verification.
* Field mode eliminates flicker from motion images.
* External computer interface allows for storage of images in compressed digital form on a PC diskette.
* External computer interface also permits auto sequencing of images in batch form, auto-dial, auto-answer, storage of uncompressed digital images, and different modes of transmission.
* Standard NTSC composite and RGB video inputs and outputs.
* Standard RJ11C jacks for telephone line and telephone set.

3) HARDWARE OVERVIEW

The major functional blocks of the transceiver are the printed circuit board assemblies. The analog video board converts the NTSC composite or RGB input signal to luminance and color difference analog video signals. The framestore board contains the A/D converters which digitize these signals and store the values in memory. The memory contents are converted back to analog luminance and color difference signals. The analog video board converts these signals to the NTSC composite and RGB analog video output signals.



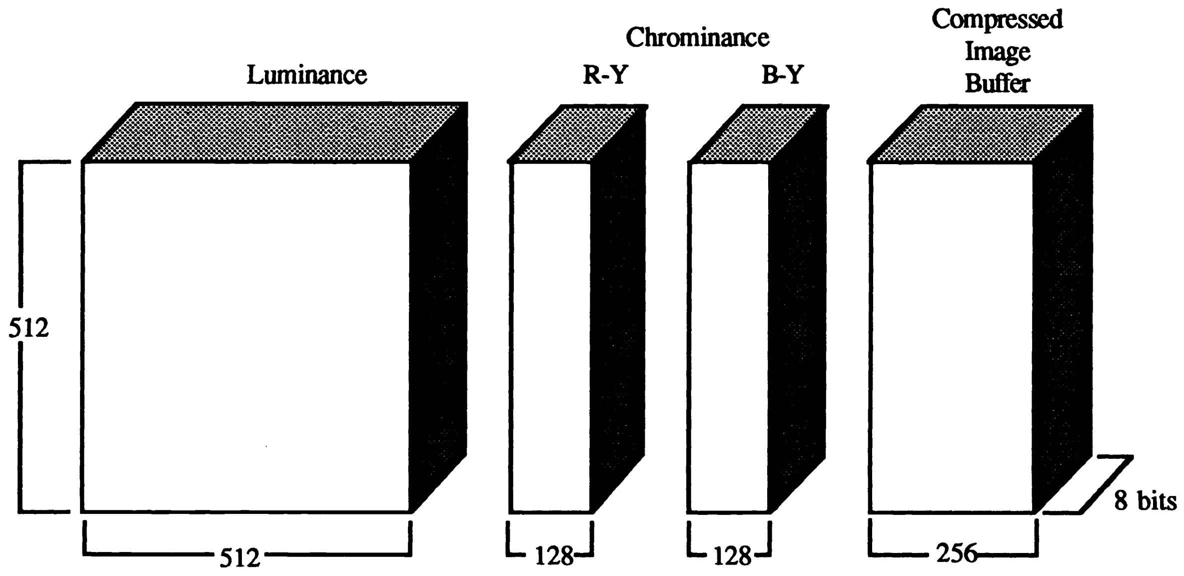
The computer board contains the microprocessor which controls the operation of the transceiver. User controls and the RS-232 serial port for the external computer interface provide the inputs and outputs to and from the microprocessor. The microprocessor along with a digital signal processor execute the compression algorithm on the image data in the framestore and store the compressed image data in memory. These two processors also perform the expansion algorithm on the compressed image data and store the resulting image data in the framestore. The computer board also contains the channel coder which is used to control the operation of the internal modem and detect errors during the transmission of the image.

The modem board supports four different data rates; 9600, 7200, 4800, & 2400 bps. In addition to the interface to the channel coder on the computer board, the modem has an interface to the microprocessor which is used to configure the modem to the different data rates and obtain diagnostic information from the modem.

In order to meet FCC requirements for connection to the telephone network, the modem board is isolated from the telephone line by the DAA (Data Access Arrangement) board. The DAA board also provides capability for auto-dialling and auto-answer.

4) FRAMESTORE ARCHITECTURE

The framestore is organized as luminance and color difference samples in order to take advantage of the human visual system. The human visual system is more sensitive to detail in luminance, or black and white, than it is in chrominance. For this reason, the color difference signals are sampled at the rate of 128 samples per line of video, while the luminance signal has 512 samples per line. This scheme is similar to the bandwidth of the Y, I and Q signals which make up the standard NTSC composite video signal. All three video signals have vertical resolution of 512 lines, although the color difference samples are averaged and subsampled vertically to a resolution of 128 lines by the microprocessor before being compressed.

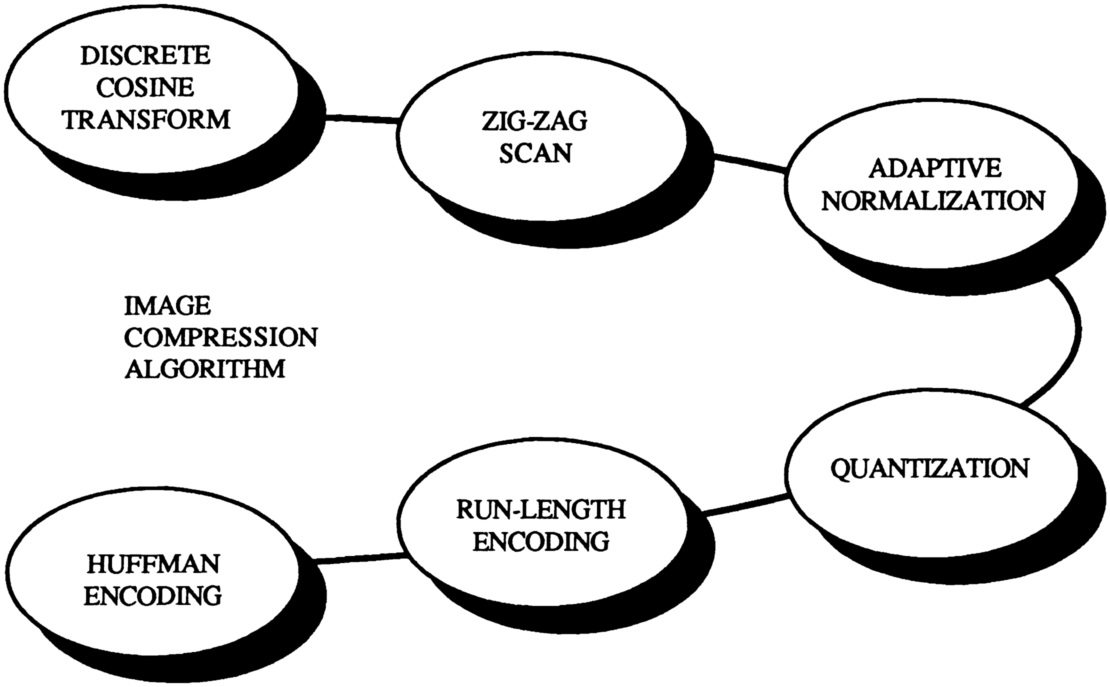


The framestore board, which has a total capacity of 512 kbytes, includes memory space for the compressed image data. The original uncompressed image occupies 384 kbytes of memory, therefore 128 kbytes are available to be used as the compressed image buffer.

The device used to control the video display and dynamic memory of the framestore allows the host microprocessor to directly address all the framestore memory locations or indirectly address the framestore by automatically adjusting the address during each access to the framestore for the next access. This indirect method is very useful in high-speed data transfers to and from the framestore.

5) COMPRESSION ALGORITHM

The image compression algorithm is based on the Discrete Cosine Transform. A 16 x 16 block of image data is used as the input to the discrete cosine transform. This 16 x 16 block can either represent original image data, or it can be the result of a 64 x 64 block of image data that has been averaged and subsampled. The discrete cosine transform is used to reduce the correlation between pixels, it can be quickly executed, and it avoids the spurious spectral components associated with a Discrete Fourier Transform.



The results of the transform, which are coefficients representing the spatial energy within the block, are then scanned into a one-dimensional array so that the first term represents the lowest spatial frequency and the last term represents the highest spatial frequency.

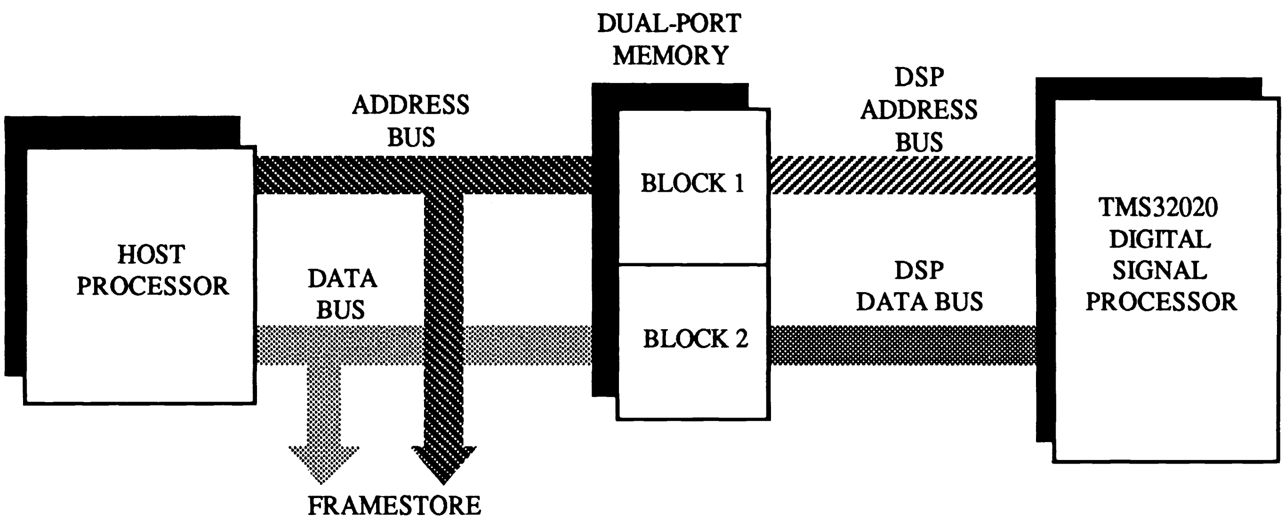
These coefficients are then normalized using an adaptive normalization process developed by Majid Rabbani and Scott Daly in the Kodak Research Labs. The normalization process is done for two reasons: 1) reduce the values of the coefficients to a smaller range for subsequent Huffman encoding; 2) create strings of very small coefficients which can be set to zero for run-length encoding. This adaptive normalization process takes into account the human visual system and is designed to be a single-pass algorithm which is necessary for it to be executed as fast as possible. The artifacts caused by this process are distributed so that they are less visible or invisible to the observer by introducing more distortion in areas where it will be less noticeable. The normalized coefficients are quantized to the nearest integer.

Up to this point no compression has been accomplished. It is in the following steps that the compression occurs. The strings of zero coefficients are run-length encoded, and finally the nonzero coefficients and run-length values are Huffman encoded using a look-up table developed in the Kodak Research Labs to be optimized for values obtained from continuous-tone color images.

6) COMPRESSION/EXPANSION HARDWARE

The TMS32020 Digital Signal Processor (DSP) is used as a parallel-processing element on the computer board. It performs a portion of the image compression/expansion algorithm while the microprocessor performs the remaining portion of the algorithm.

This is accomplished by using a dual-port memory , thereby allowing both processors simultaneous access to the data memory. The memory is divided into two blocks which are alternately accessed by the DSP and microprocessor in an alternating manner. While the microprocessor operates on the second half of the memory, the DSP works on the first half. When the microprocessor has finished with the second half, it proceeds to the first half where the DSP has placed its resulting values. Meanwhile, the DSP operates on the data of the second block.



This switching back and forth is repeated until the entire image is processed. A single memory location is defined for each block as the communication link between the two processors. Writing to its location allows the microprocessor to instruct the DSP as to which operation should be performed, and the DSP notifies the microprocessor it has completed its processing on the block by writing to its location.

7) COMPRESSION RATIO/TRANSMISSION TIME

If the image was stored as red, green and blue (RGB) with 512 samples per line in all three colors, and the vertical resolution was 512 lines of video, the digital image would require 786,432 bytes for memory space. This assumes each sample has 8 bits per pixel which is equivalent to a bit rate of 24 bits per pixel. The stored image in the transceiver only requires 393,216 bytes, but only 294,912 bytes are used since the color difference samples are subsampled and averaged vertically. Therefore, the architecture of the framestore has already provided a 2.7:1 compression ratio relative to the original RGB image. The compression algorithm typically provides a compression ratio of 6:1, which gives a total compression ratio relative to the RGB image of 16:1. In other words, the resulting bit rate of the compressed image is 1.5 bits per pixel. Therefore, a typical compressed image requires 48k bytes of memory space.

It should be pointed out that the compression algorithm will result in a compressed image size and bit rate that is dependent on the amount of spatial frequency information contained in the image. Images with more detail will have a higher bit rate.

If the original RGB image was sent at 1200 bps, the transmission time would be 90 minutes. Increasing the

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