ARM610

Data Sheet

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Proprietary Notice

Change Log

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Preface

The ARM610 is a general purpose 32-bit microprocessor with 4kByte cache, write buffer and Memory Management Unit (MMU) combined in a single chip. The ARM610 offers high level RISC performance yet its fully static design ensures minimal power consumption, making it ideal for portable, low-cost systems.

The innovative MMU supports a conventional two-level page-table structure and a number of extensions which make it ideal for embedded control, UNIX and Object Oriented systems. This results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective chip.

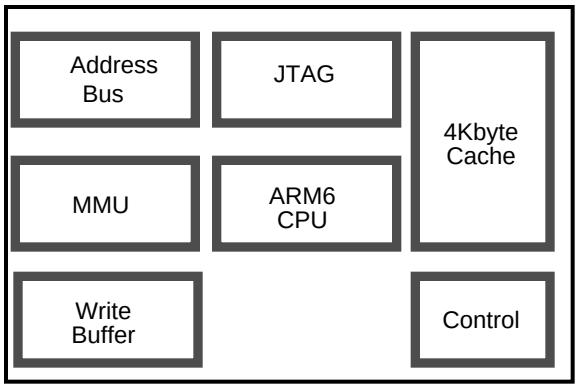
Applications

The ARM610 is ideally suited to those applications requiring RISC performance from a compact, power efficient processor. These include:

- *Personal computer devices e.g.PDAs*
- *High-performance real-time control systems*
- *Portable telecommunications*
- *Data communications equipment*
- *Consumer products*
- *Automotive*

Feature Summary

- *High performance RISC*
  15 MIPS sustained @ 20 MHz (20 MIPS peak)
- *Fast sub microsecond interrupt response*
  for real-time applications
- *Memory Management Unit (MMU)*
  support for virtual memory systems
- *Excellent high-level language support*
- *4kByte of instruction & data cache*
- *Big and Little Endian operating modes*
- *Write Buffer*
  enhancing performance
- *IEEE 1149.1 Boundary Scan*
- *Fully static operation, low power consumption*
  ideal for power sensitive applications
- *144 Thin Quad Flat Pack (TQFP) package*



1.0 Introduction

ARM610, is a general purpose 32-bit microprocessor with 4kByte cache, write buffer and Memory Management Unit (MMU) combined in a single chip. The CPU within ARM610 is the ARM6. The ARM610 is software compatible with the ARM processor family and can be used with ARM support chips, eg IO, memory and video.

The ARM610 architecture is based on 'Reduced Instruction Set Computer' (RISC) principles, and the instruction set and related decode mechanism are greatly simplified compared with microprogrammed 'Complex Instruction Set Computers' (CISC).

The on-chip mixed data and instruction cache together with the write buffer substantially raise the average execution speed and reduce the average amount of memory bandwidth required by the processor. This allows the external memory to support additional processors or Direct Memory Access (DMA) channels with minimal performance loss.

The MMU supports a conventional two-level page-table structure and a number of extensions which make it ideal for embedded control, UNIX and Object Oriented systems.

The instruction set comprises ten basic instruction types:

- Two of these make use of the on-chip arithmetic logic unit, barrel shifter and multiplier to perform high-speed operations on the data in a bank of 31 registers, each 32 bits wide;
- Three classes of instruction control data transfer between memory and the registers, one optimised for flexibility of addressing, another for rapid context switching and the third for swapping data;
- Two instructions control the flow and privilege level of execution; and
- Three types are dedicated to the control of external coprocessors which allow the functionality of the instruction set to be extended off-chip in an open and uniform way.

The ARM instruction set is a good target for compilers of many different high-level languages. Where required for critical code segments, assembly code programming is also straightforward, unlike some RISC processors which depend on sophisticated compiler technology to manage complicated instruction interdependencies.

The memory interface has been designed to allow the performance potential to be realised without incurring high costs in the memory system. Speed-critical control signals are pipelined to allow system control functions to be implemented in standard low-power logic, and these control signals permit the exploitation of paged mode access offered by industry standard DRAMs.

ARM610 is a fully static part and has been designed to minimise its power requirements. This makes it ideal for portable applications where both these features are essential.

Datasheet Notation:

0x	- marks a Hexadecimal quantity
BOLD	- external signals are shown in bold capital letters
binary	- where it is not clear that a quantity is binary it is followed by the word binary

ARM610 is a variant of the ARM600, differing from that device in the following respects:

- No external coprocessor bus interface
- Internal Address latches controlled by **ALE** added
- **nRW**, **nBW**, **LOCK** also latched by **ALE**, and tristated by **ABE**. (**CBE** therefore removed)
- Dedicated chip test port added
- Device packaging

1.1 Block Diagram

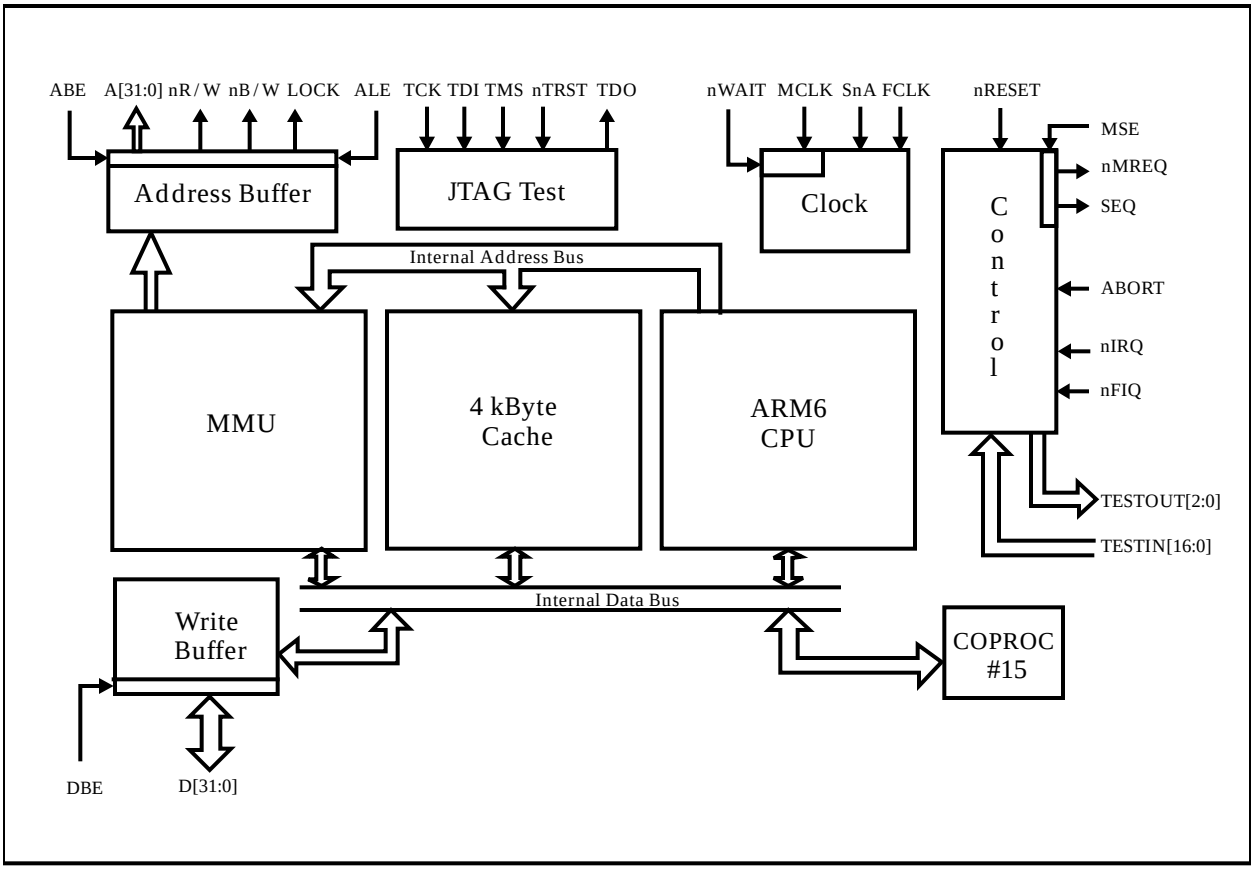


Figure 1: ARM610 Block Diagram

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