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Asynchronous HDLC

MC68360 ASYNC HDLC Protocol Microcode

User's Manual

Rev 1.1

January 24, 1996

Freescale Semiconductor, Inc.

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Asynchronous HDLC

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1 ASYNC HDLC Controller Overview

Asynchronous HDLC is a frame-based protocol which uses HDLC framing techniques in conjunction with UART-type characters. This protocol is typically used as the physical layer for the Point-to-Point (PPP) protocol. While this protocol can be implemented by the UART controller on the QUICC in conjunction with the CPU32+, it is more efficient and less compute-intensive for the CPU to allow the Communications Processor Module (CPM) of the QUICC to perform the framing and transparency functions of the protocol.

2 ASYNC HDLC Controller Key Features

- Flexible data buffer structure which allows an entire frame or a section of a frame to be transmitted and received.
- Separate interrupts for received frames and transmitted buffers
- Automatic CRC generation and checking (CRC-CCITT)
- Support for NMSI control signals (Carrier Detect, Clear to Send, Ready to Send)
- Automatic generation of opening and closing flags
- Reception of frames with only one “shared” flag
- Automatic generation and stripping of transparency characters according to RFC 1549 utilizing transmit and receive control character maps.
- Automatic transmission of the ABORT sequence (0x7D,0x7E) after the STOP TRANSMIT command is issued.
- Automatic transmission of IDLE characters between frames and characters.
- “Small” RAM Microcode (consumes 768 bytes of Dual-Port RAM)

2.1 ASYNC HDLC Channel Frame Transmission Processing

The ASYNC HDLC Controller is designed to work with a minimum amount of intervention from the CPU32+ core. It operates in a similar fashion to the HDLC controller on the QUICC.

When the core enables one of the transmitters and sets the ready (R) bit in the first Buffer Descriptor, the ASYNC HDLC Controller fetches the data from memory and start transmitting the frame (after transmitting the opening flag). When the controller reaches the end of the current BD, the CRC and the closing flag are appended if the last (L) bit in the Tx BD is set. If the continuous mode (CM) bit is clear, the ASYNC HDLC transmitter writes the frame status bits into the BD and clears the ready bit. If the interrupt (I) bit is set, the controller sets the TXB event bit in the event register. Thus, the I bit may be used to generate an interrupt after each buffer, after a group of buffers, or after each complete frame has been transmitted.

If the CM bit in the Tx BD is set, the ASYNC HDLC controller will write the signal unit status bits into the BD after transmission but it will not clear the ready bit.

The ASYNC HDLC controller will then proceed to the next Tx BD in the table. If it is not ready, the ASYNC HDLC controller will wait until the Tx BD is ready.

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