

EXHIBIT

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Wheatley

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(54) **FRAME SYNCHRONIZATION IN DATA COMMUNICATION SYSTEM**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 746 days.

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(30) **Foreign Application Priority Data**
Sep. 18, 2000 (EP) 00308080

(51) **Int. Cl.**
H04L 7/00 (2006.01)

(52) **U.S. Cl.** **375/368**

(58) **Field of Classification Search** 375/365-368, 375/354, 355, 362
See application file for complete search history.

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Primary Examiner—Kevin Burd

(57) **ABSTRACT**

In order to provide a simple and reliable means of frame synchronization in a serial data communication system, which avoids the problem of 'bit-stuffing' in known HDLC systems, the data communication system comprises a transmitter arranged to transmit data as a sequence of frames, each frame comprising a synchronization section and a payload section of data, and the transmitter including in the synchronization section of each frame a count value of a sequence of count values (a part of a predetermined code sequence), wherein successive frames contain successive count values (other parts of the predetermined code sequence) The receiver includes a FIFO buffer for storing three successively received frames, and a processor for assessing the stored data within the frames in order to locate and recognize the count values, whereby to synchronize to the received frames.

18 Claims, 3 Drawing Sheets

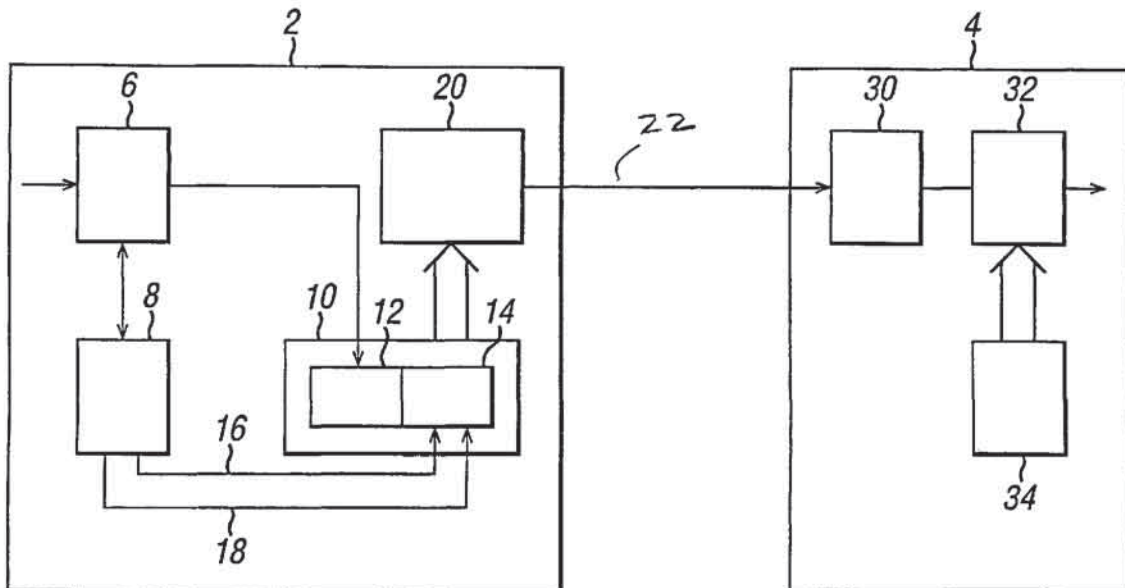


FIG. 1

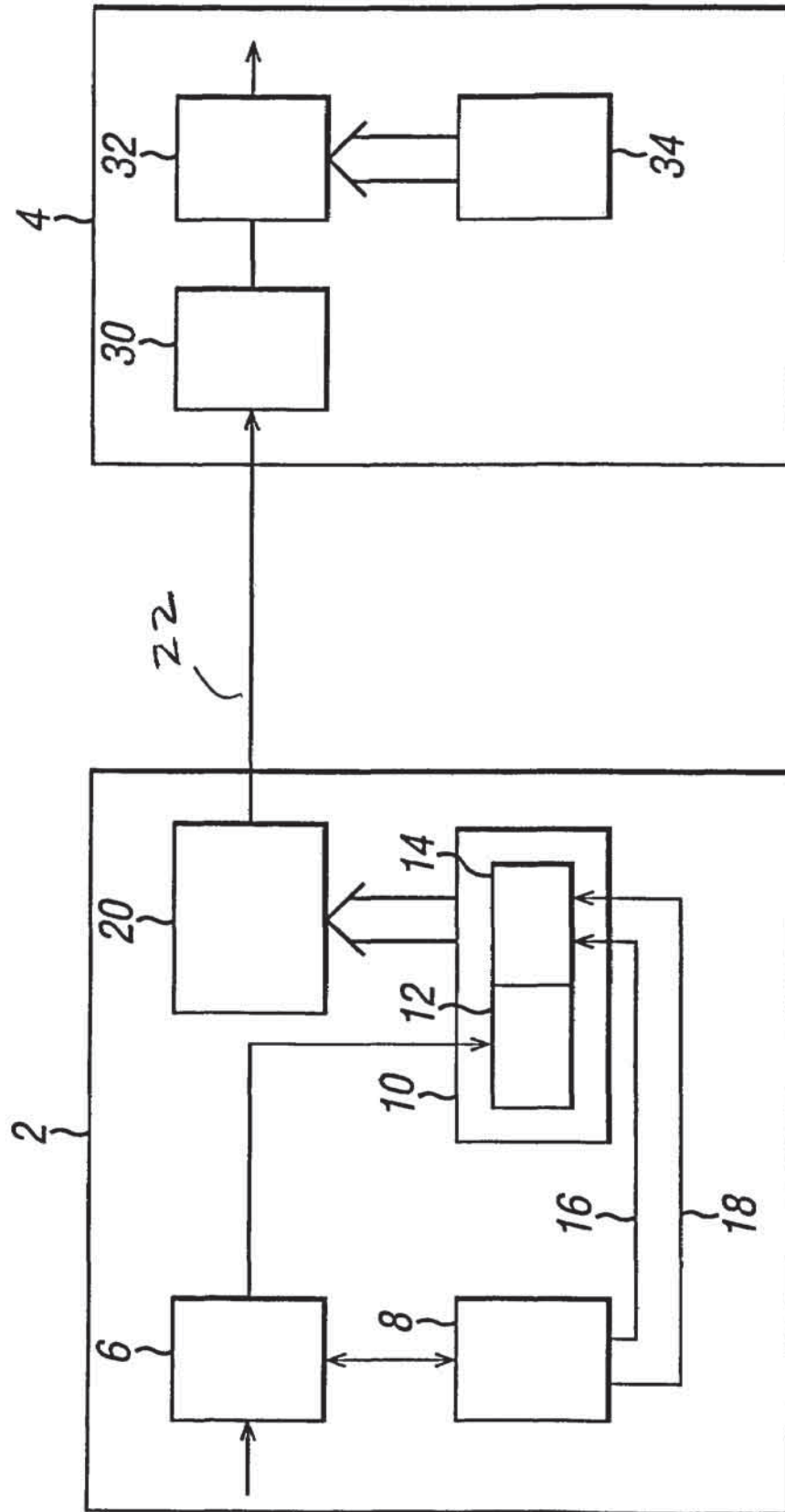
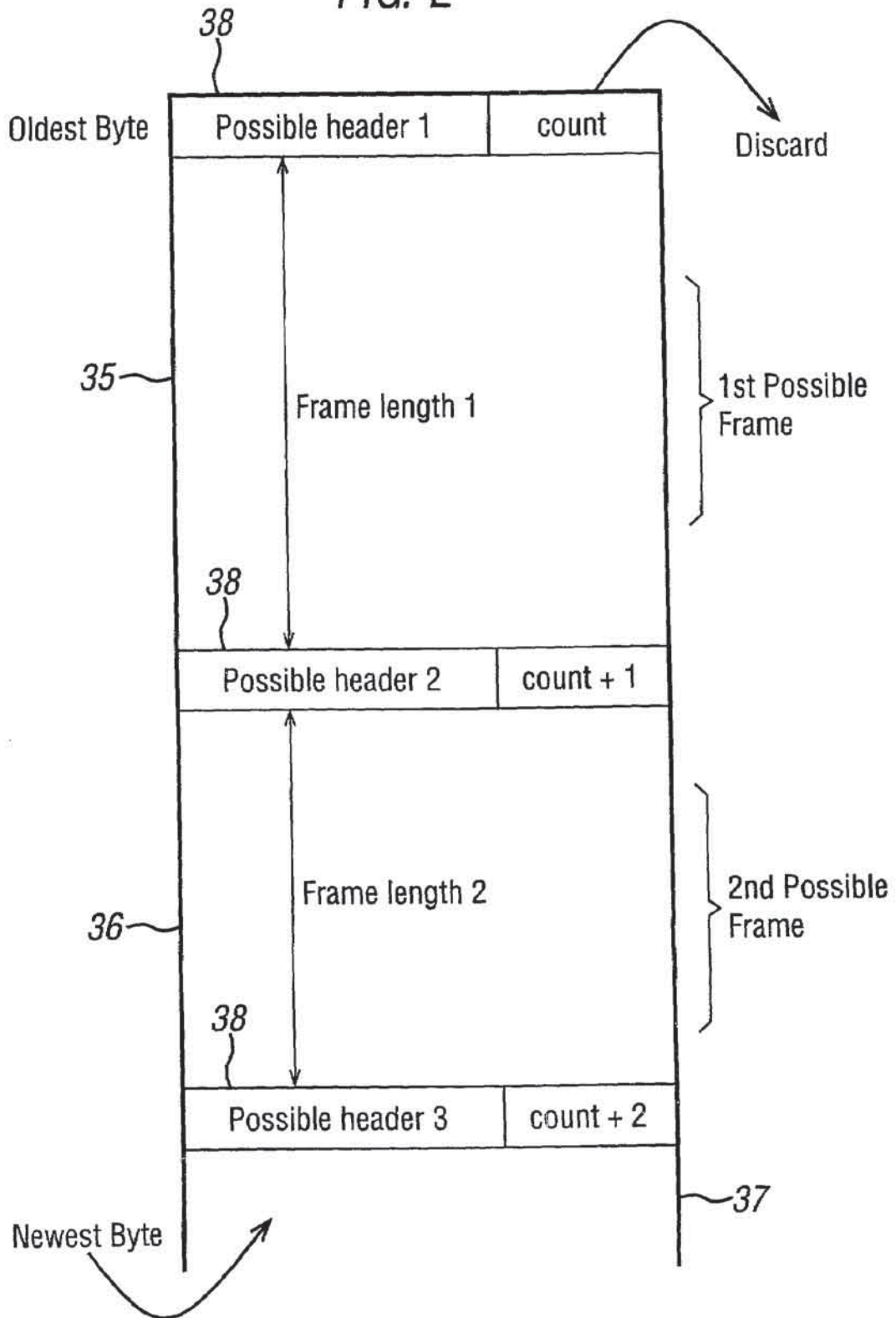


FIG. 2



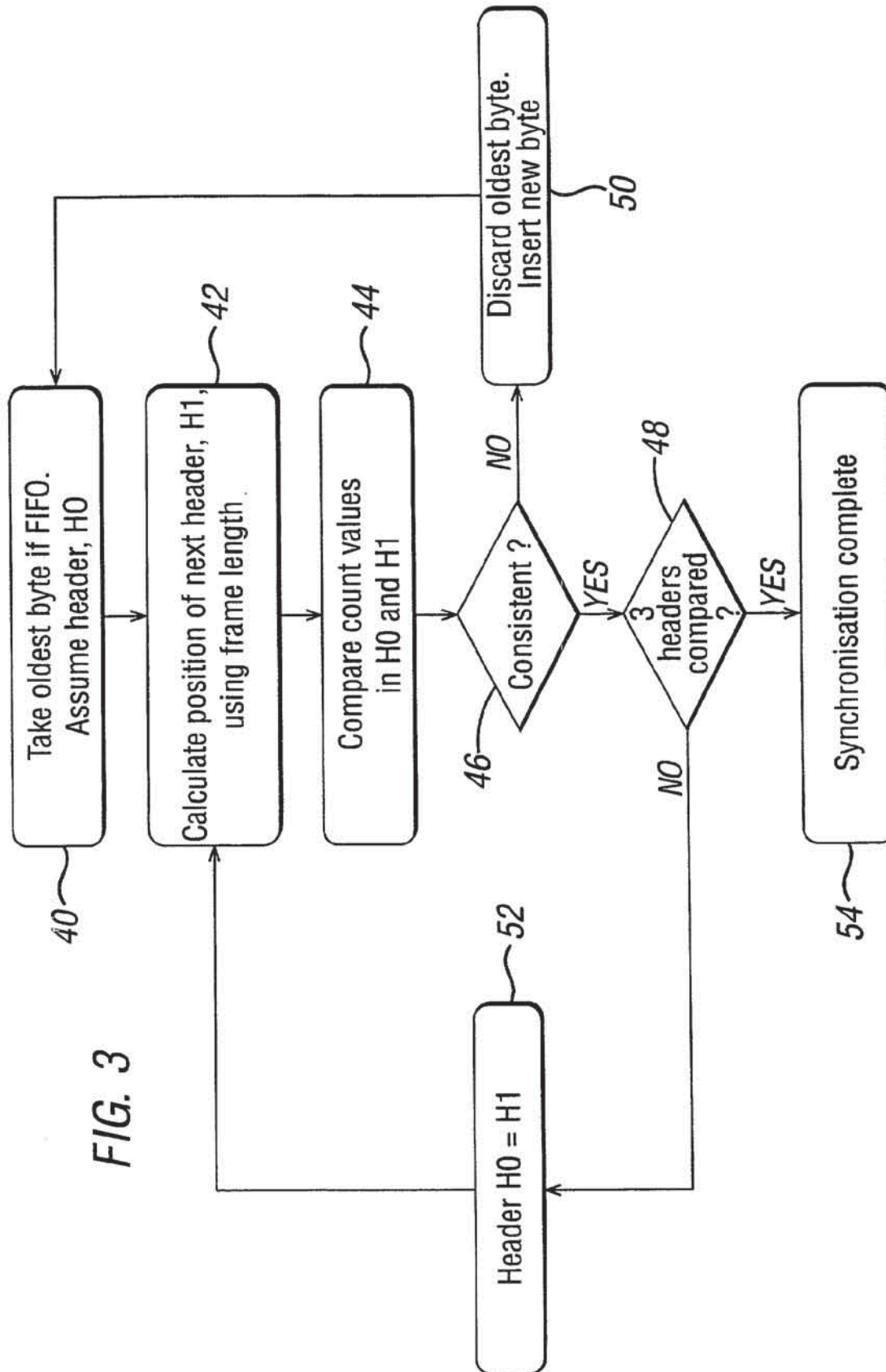


FIG. 3

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