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Grants et al.

[11] **4,281,392**

[45] **Jul. 28, 1981**

[54] **MEMORY CIRCUIT FOR PROGRAMMABLE MACHINES**

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[51] **Int. Cl.**[3] **G06F 13/06**; G11C 5/06; G11C 7/00; G11C 9/00

[52] **U.S. Cl.** **364/900**

[58] **Field of Search** ... 364/200 MS File, 900 MS File; 371/21; 324/73 R

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,967,251	6/1976	Levine	364/200
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Assistant Examiner—C. T. Bartz
Attorney, Agent, or Firm—Quarles & Brady

[57] **ABSTRACT**

A memory circuit receives memory modules which may vary in their size and their type. The memory circuit includes a decoder circuit which receives size feedback signals from each memory module which enables it to automatically assign each module the address space it requires. If the size of a memory module is changed, the decoder circuit reassigns the address space to accommodate the new module. Type feedback signals generated by each memory module enable the memory circuit to apply the proper control signals and enable the proper supporting circuitry when the memory module is addressed.

9 Claims, 4 Drawing Figures

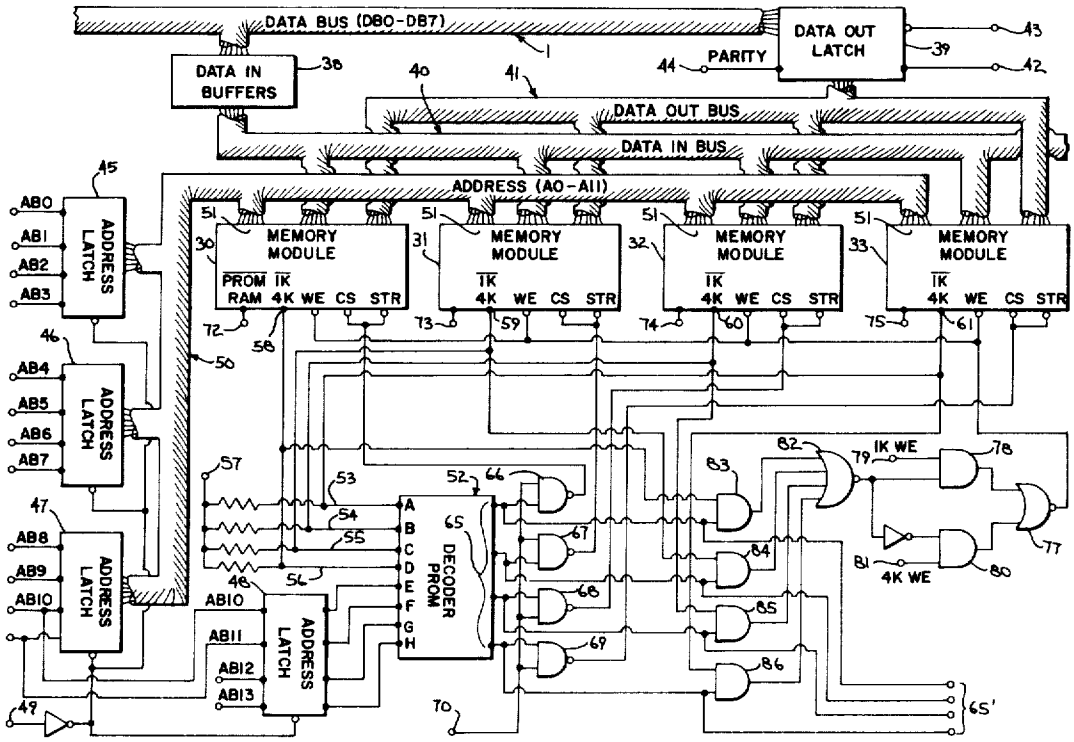
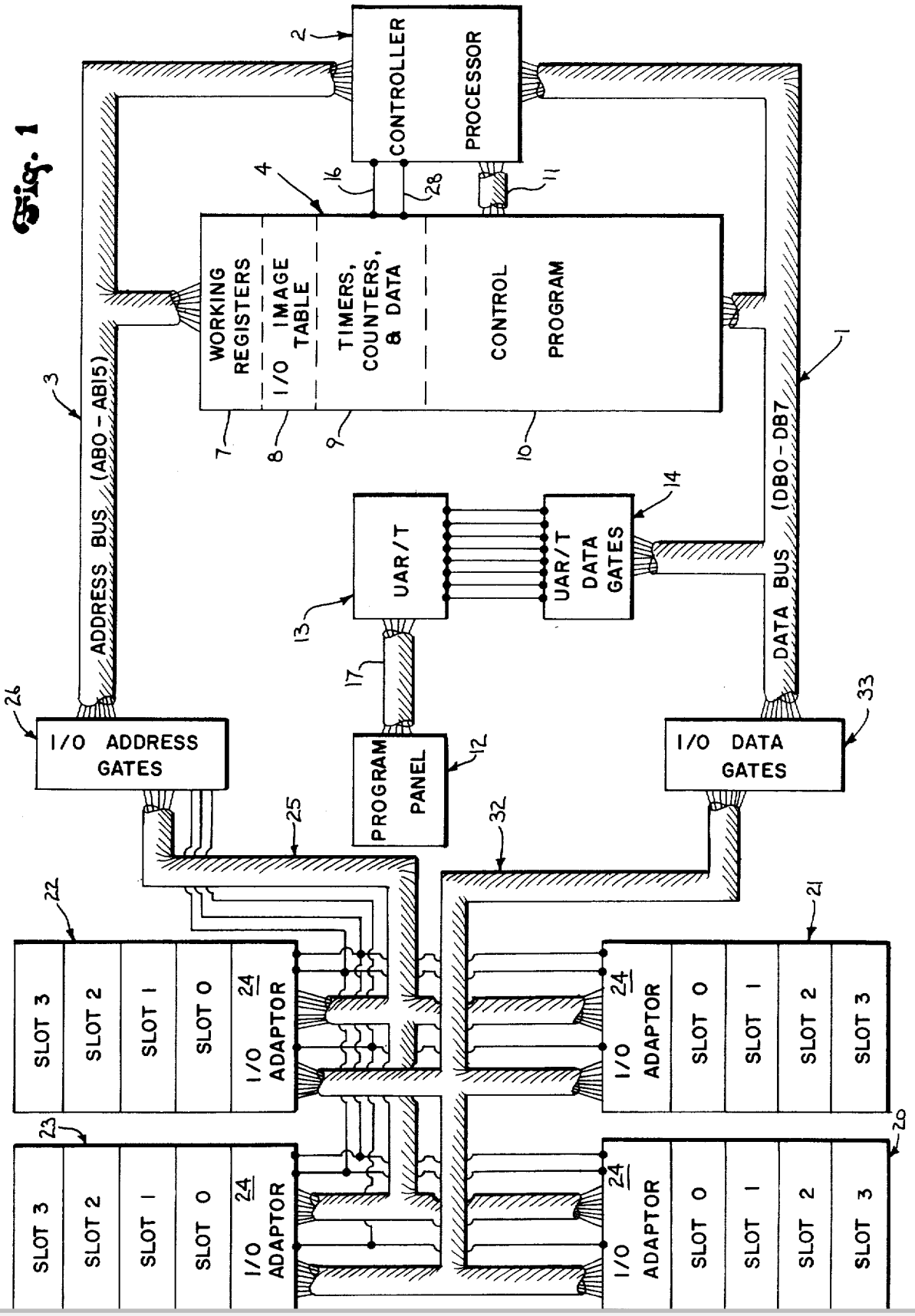


Fig. 1



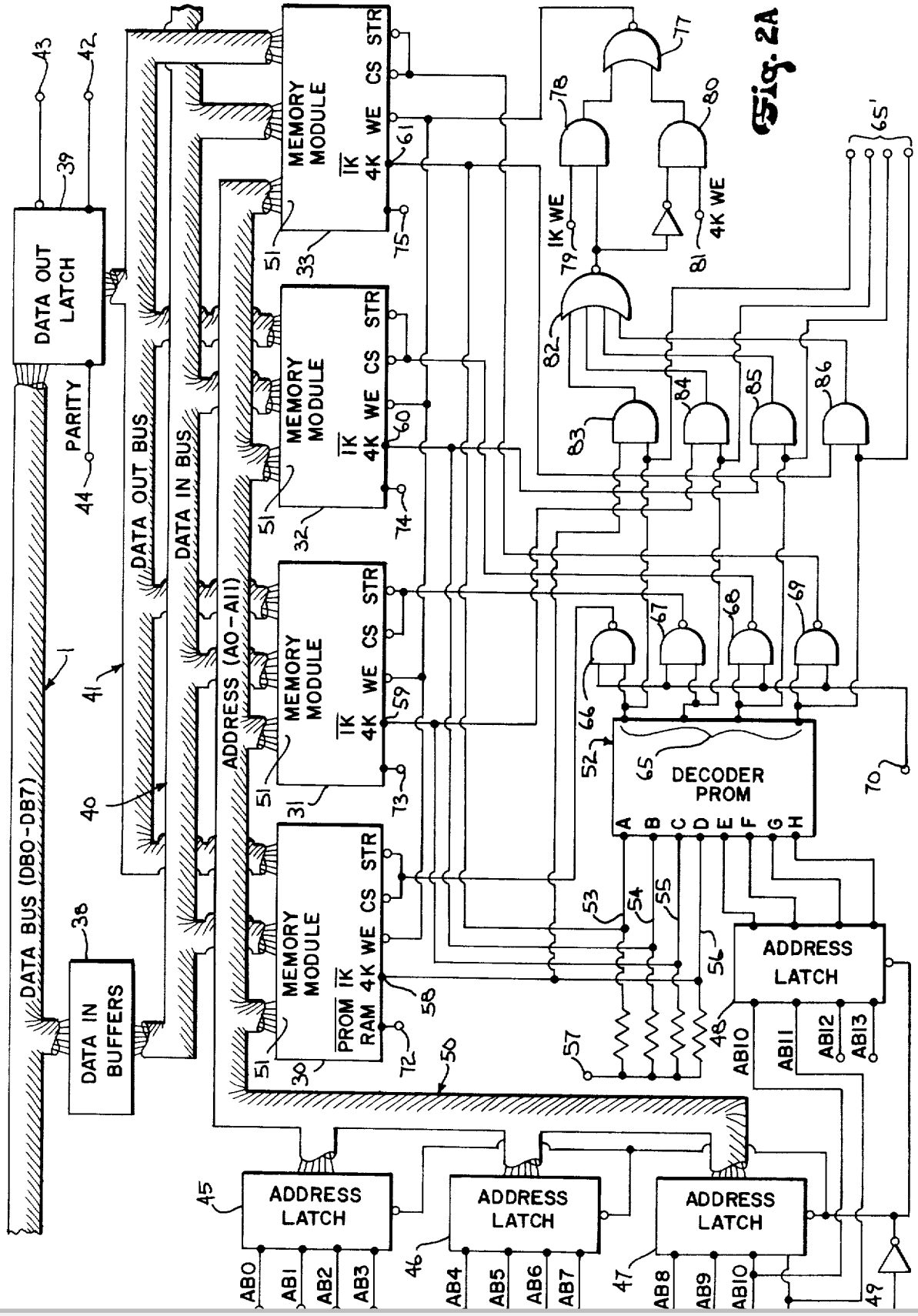


Fig. 2A

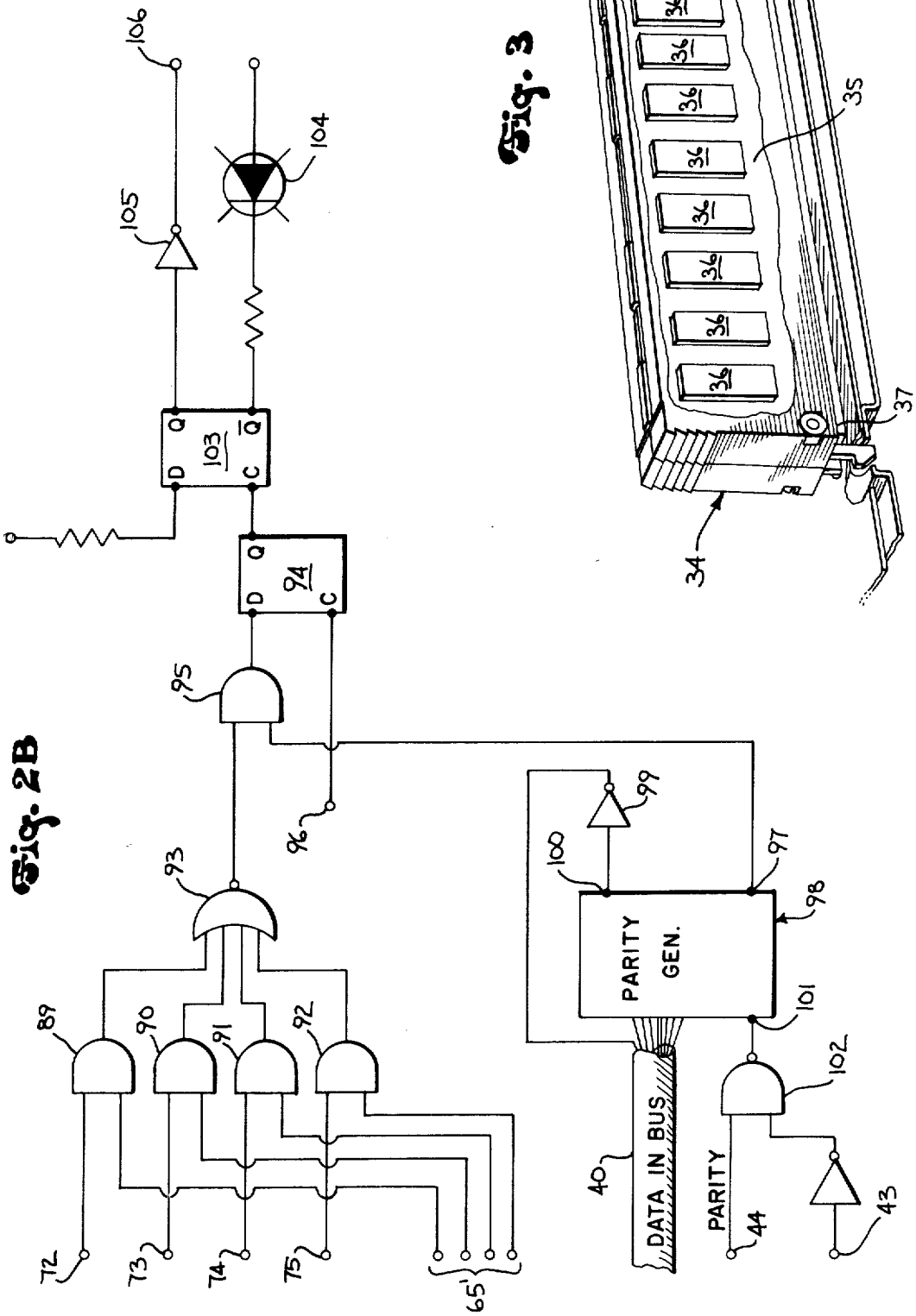


Fig. 2B

Fig. 3

MEMORY CIRCUIT FOR PROGRAMMABLE MACHINES

BACKGROUND OF THE INVENTION

The field of the invention is programmed machines which store programs and other data in addressable memory devices, and particularly, machines in which the user can readily add or exchange memory devices of various sizes and types.

In programmable machines such as programmable controllers the user employs a program panel to develop a control program which is stored in a memory device such as a random access memory (RAM) or a read-only memory (ROM). The control program which is developed may be very short in some applications (less than 1K memory lines) while in other applications it may become quite lengthy (16K memory lines or more). Also, some portions of the control program may be fixed, and thus suitable for employing read-only memory devices, whereas other portions may undergo periodic change and be more suitably stored in read/-write memory devices. It is desirable, therefore, to allow the user flexibility in the size of the memory he may use and the type of memory devices he may employ.

Nearly all programmed machines have a limited amount of address space and most of this space is occupied by memory devices. In both microprocessor-based and minicomputer-based machines, for example, a 16-bit address bus is employed which provides a 64K address space. Although address expansion techniques are well known, these require additional hardware and more execution time. In providing a flexible system in which the user may interchange memory devices of varying sizes, therefore, it is important that the available address space be efficiently used.

SUMMARY OF THE INVENTION

The present invention is a memory circuit for a programmable machine in which memory devices in the form of memory modules of various sizes and types may be used without alteration of the circuit. More specifically, the memory circuit includes a decoder circuit which connects to selected leads in the machine's address bus and which connects to size feedback lines that connect to the memory modules and which indicate to the decoder circuit the size of the memory modules being used. The decoder circuit is responsive to signals on the machine's address bus to provide signals which enable the memory modules in such manner that they occupy a contiguous address space regardless of the size of the memory devices employed in them. Also, gates are provided for receiving signals from each memory module on type feedback lines and for enabling the proper supporting circuitry for each memory module as it is addressed.

A general object of the invention is to provide a memory circuit into which memory modules of differing sizes can be inserted without alteration of the circuitry or waste of address space. When a memory module is inserted in place of a memory module of larger size, the size feed-back signal which it generates alters the decoder circuit operation such that the address space allocated to other memory modules is shifted to close the gap in address space which would otherwise occur. On the other hand, if a small memory module is replaced by a larger memory module, the size feedback signal which it generates causes the decoder circuit to enlarge the address space gap to the required size.

Another object of the invention is to provide a memory circuit into which memory modules of differing types can be inserted without alteration of the circuitry. When a random access memory module is inserted in place of a read-only memory module, the type feedback signal which it generates enables parity circuitry. The parity circuitry includes a parity generator which writes a parity bit into the random access memory during write operations and which checks the parity of data read from the random access memory. Ths circuitry is automatically disabled when a read-only memory is employed.

Another object of the invention is to enable memory modules of differing sizes and types to be intermixed in the same memory circuit. The feedback signals generated by each memory module indicate to the circuitry its size and type, and the circuitry automatically allocates the proper amount of address space and enables the proper control signals and supporting circuitry when the memory module is addressed.

The foregoing and other objects and advantages of the invention will appear from the following description. In the description, reference is made to the accompanying drawings which form a part hereof, and in which there is shown by way of illustration a preferred embodiment of the invention. Such embodiment does not necessarily represent the full scope of the invention, however, and reference is made therefore to the claims herein for interpreting the scope of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is an electrical block diagram of a programmable controller which employs the memory circuit of the present invention;

FIGS. **2A** and **2B** are electrical schematic diagrams of the memory circuit which incorporates the present invention; and

FIG. **3** is a perspective view with parts cut away of a memory module which forms part of the circuit of FIG. **2A**.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The memory circuit of the present invention is employed in a programmable controller. Referring to FIG. **1**, this programmable controller is structured around an eight-bit bidirectional data bus **1** and includes a controller processor **2** which directs the flow of data thereon by means of control lines and a sixteen-bit address bus **3**. A memory circuit **4** connects to both the data bus **1** and the address bus **3** and an eight-bit data word may be written into an addressed line or read out of an addressed line of the memory **4** in response to control signals applied to "data strobe" and "WE" control lines **16** and **28**. The memory **4** may include anywhere from 1K to 16K lines of memory which store working registers **7**, an I/O image table **8**, a timers, counters and data storage **9** and a control program **10**.

The control program portion **10** of the memory circuit **4** stores a series or programmable controller type instructions such as those defined in U.S. Pat. No. 3,942,158. Each controller instruction is stored on two 8-bit memory lines and when it is read out through the data bus **1** to the controller processor **2**, an operation code therein directs the processor **2** to perform a desig-

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