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[54] **SINGLE IN-LINE MEMORY MODULE**

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[57] **ABSTRACT**

What is disclosed is a memory module to and from which multibit binary words are stored and read out. Each multibit binary word comprises a standard word size and another memory bit that may be used for purposes such as parity checking. The modules may be mounted on a printed circuit mother board from which power, control signals and binary words are applied to and taken from the module.
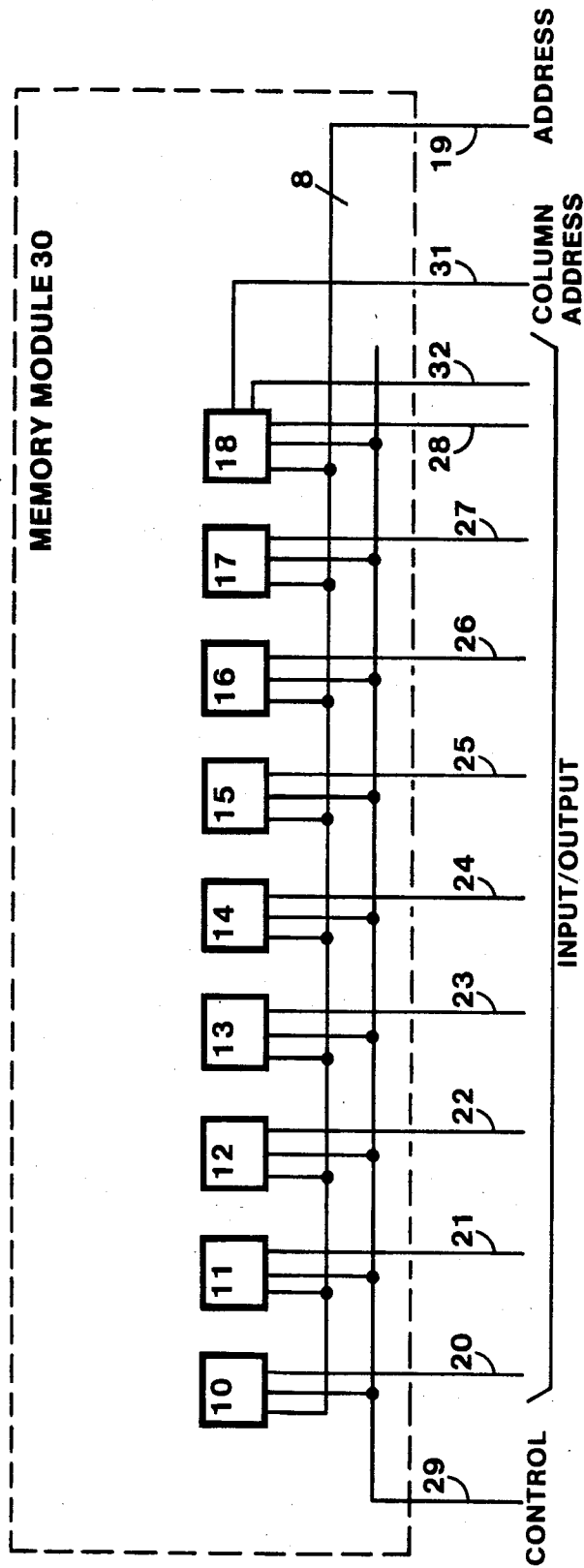
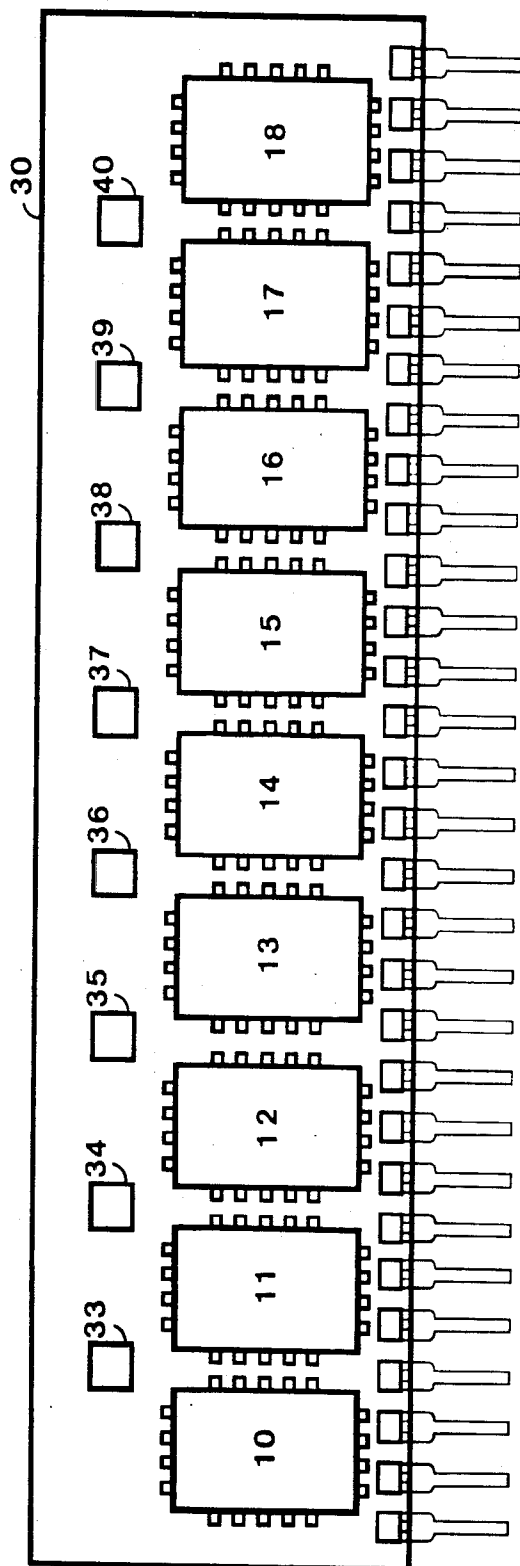**1 Claim, 2 Drawing Figures**
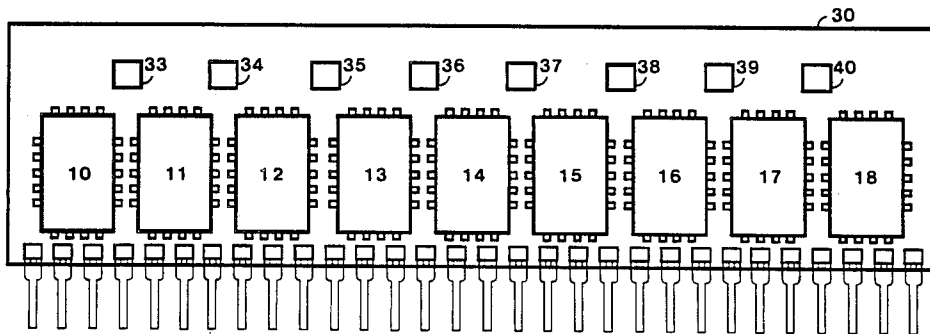
FIGURE 1

FIGURE 2

SINGLE IN-LINE MEMORY MODULE

The present application is a continuation of U.S. patent application Ser. No. 528,817 filed Sept. 2, 1983 by James E. Clayton for a SINGLE IN-LINE MEMORY MODULE, subsequently abandoned.

BACKGROUND OF THE INVENTION

This invention relates to memories and more particularly to modular memories providing storage and retrieval of binary words.

What is disclosed is a memory module to and from which multibit binary words are stored and read out. Each multibit binary word comprises a standard byte size and one or more other memory bits that may be used for purposes such as parity checking. The modules may be mounted on a printed circuit mother board from which power, control signals and binary words are applied to and taken from the module.

SUMMARY OF THE INVENTION

The present invention is a memory module on which a plurality of memory components each storing or reading one binary bit at a time have their power, control, input/output and other access leads interconnected so there is only one set of these leads available at terminals of the module. A first plurality of these memories provide for one binary word being input or output to the memory module at a time. In addition, I add another individual memory intended for purposes such as parity checking and error correction. This additional memory has its power and control leads interconnected with the other memories within the module, but has separate input/output lead(s) and column address select leads to enable independent accessing or addressing of the parity memory.

DESCRIPTION OF THE DRAWING

My invention will be understood on reading the following detailed description in conjunction with the drawing in which:

FIG. 1 is an electrical block diagram of my novel memory module; and

FIG. 2 is a mechanical layout drawing of the memory module.

DETAILED DESCRIPTION

In FIG. 1 is seen the electrical block diagram of my invention. In one embodiment of my invention, the embodiment shown in FIG. 1, eight individual memory chips 10–17, each capable of storing a zero or a one binary bit at each memory location, are accessed by a multi-bit address applied to address leads 19 which comprises eight leads. With this embodiment of my invention, single input/output leads 20–27 are provided respectively to each of memory chips 10–17 to provide a total of eight input/output leads making up an eight bit binary word. Control lead 29 connected to one input of each of memory chips 10–17 on the module 30 indicates whether a read or write operation is being performed at the location identified by the address present on the eight address leads 19 which are interconnected to the addressing inputs of each of chips 10–17.

In a manner well known in the art the concurrent addressing and control of chips 10–17 which are connected in parallel permits an eight bit byte or binary

word to be store in or read out of memory chips 10–17 for each read or write operation.

In accordance with the preferred embodiment of my invention I provide an extra memory chip 18 similarly connected in parallel with memory chips 10–17, the read/write control leads of which are interconnected with the control leads 29 connected to memory chips 10–17 with the exception of the column address select lead 31. Memory chip 18 has a data input lead 28 and a separate data output lead 32 as distinguished from memory chips 10–17 which respectively use common input-/output data leads 20–27 for both data input and output. A total of ten input/output data leads 20–28 and 32 are therefore provided on the edge of the memory module 30 as shown and eight bit binary words plus and extra ninth bit for functions such as parity checking are stored in or read out of the memory module 30. A separate column address select lead 31 is provided for memory chip 18 to enable independent operation for the parity function.

When it is desired to store a binary word made up of an eight bit byte/word with a ninth parity bit in a specific address location in memory chips 10–17 and 18, the binary bits are applied to terminals on the edge of memory module 30 which are connected to common input-/output leads 20–27 and to input lead 28. Each of the nine binary bits is thereby applied to the input respectively of memory chips 10–18. A signal is then applied to control lead 29 at a terminal on the edge of memory module 30, which control lead 29 is connected to the read/write control input of chips 10–18. Finally, a multibit binary address is applied to the multiple address leads 19 also on the edge of memory module 30, which addressing leads are connected to the addressing inputs of each of memory chips 10–18. In response to all the above signals applied to the appropriate terminals of memory module 30, the binary word on input/output leads 20–27 and the extra binary bit on input lead 28 are stored respectively in memory chips 10–17 and 18 at the address indicated by the binary number on address leads 19.

Similarly, when it is desired to read a binary word out of memory module 30, a read signal is applied to read-/write control lead 29 and a binary address is applied to address leads 19. In response thereto, the binary word stored in memory module 30 at the indicated address is read out of memory chips 10–17 and 18 respectively onto input/output leads 20–27 and output lead 32.

Referring to FIG. 2, there is shown a physical layout of my memory module 30. The nine memory chips 10–18 are mounted on a substrate 31 that may be a printed circuit board (glass-epoxy) or ceramic. The memory chips 10–18 may be dynamic RAMs (D-RAM) advantageously packaged in small plastic leaded chip carriers available from Texas Instruments and soon from other companies such as National Semiconductor, Motorola, and AMD. Also mounted on the substrate of module 30 are small ceramic decoupling capacitors 33–40, having a value bewteen 0.1 and 0.22 ufd, and connected between each of memory chips 10–18 to suppress transient voltage spikes. By using the small D-RAMs and small capacitors, module 30 may have physical dimensions in the order of three-quarter inch by three inches while providing large memory capacity. Sixty-four thousand words on the module are presently possible and two hundred fifty-six thousand bytes are feasible with the physical dimensions of module 30 only being slightly larger.

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With my invention the input, output and control of the memory elements **10–18** on module **30** may be accomplished via only thirty terminals on the edge of the module. Use of module **30** in lieu of memory chips in conventional dual in line terminal packages normally mounted in rows and columns on a printed circuit board enables an eight-fold density increase over previous circuit assembly technology,

In addition, by having an extra memory chip parity may be checked. By having separate control of the extra memory chip a system designer has more flexibility in designing parity operation.

While what has been described hereinabove is the preferred embodiment of my invention, it will be obvious to those skilled in the art that numerous changes may be made without departing from the spirit or scope of the invention. More than one bit may be used for parity checking or other purposes. In addition, rather than using discrete memory chips, the unpackaged dies may be mounted on a substrate to implement my invention in a hybrid integrated circuit package or in a large scale integrated circuit package.

I claim:

1. A memory module for installation on a printed circuit motherboard comprising:

eight data memory chips for storing digital data, each having a data input and output, a control input, and an address input, and each being packaged in a plastic leaded chip carrier;

a ninth memory chip for storing error detection and correction information associated with the eight data memory chips, said ninth memory chip having

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a data input and output, a control input and an address input interconnected with those of the eight memory chips, and a control input to provide writing in or reading out of the ninth memory chip at times other than when said bytes of digital information are written into or read out of the eight data memory chips to thereby facilitate said error detection and correction operation;

an epoxy-glass printed circuit board substrate having a length and width adequate for mounting thereon only in a single row said nine memory chips and for interconnecting the control inputs and the address inputs of the memory chips so that bytes of digital information may be input to or output from the memory chips one at a time;

the substrate including thirty terminals for providing access to the data inputs and outputs, control inputs, and address inputs of the nine memory chips to enable reading and writing of bytes of digital information into and out of the eight memory chips and to enable reading and writing of error detection and correction information into and out of the eight memory chips;

support means for supporting the memory module at an angle with respect to the printed circuit motherboard when the memory module is installed thereon; and

eight decoupling capacitors, mounted on said substrate and connected between the nine memory chips, for supressing transient voltage spikes between said memory chips.

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