IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of:	Morton et al.	Case Nos.:	IPR2015-00159
U.S. Patent No.:	7,296,121		IPR2015-00161
Issue Date:	Nov. 13, 2007		IPR2015-00163
Appl. Serial No.:	10/966,161		IPR2015-00172
Filing Date:	Oct. 15, 2004		

Title: REDUCING PROBE TRAFFIC IN MULTIPROCESSOR SYSTEMS

DECLARATION OF DR. ROBERT HORST

1. My name is Dr. Robert Horst. I am the Chief Technology Officer, Robotics of AlterG, and I am an independent consultant at HT Consulting. I have been asked to offer technical opinions relating to U.S. Patent No. 7,296,121, and prior art references relating to its subject matter. My current *curriculum vitae* is attached and some highlights follow.

2. I earned my M.S. (1978) in electrical engineering and PhD (1991) in computer science from the University of Illinois at Urbana-Champaign after earning my B.S. (1975) in electrical engineering from Bradley University. During my master's program, I designed, constructed and debugged a shared memory parallel microprocessor system. During my doctoral program, I designed and simulated a massively parallel, multi-threaded *task flow* computer.

3. After receiving my bachelor's degree and while pursuing my master's degree, I worked for Hewlett-Packard Co. While at Hewlett-Packard, I designed the micro-sequencer and cache of the HP3000 Series 64 processor. From 1980 to

1999, I worked at Tandem Computers which was acquired by Compaq Computers in 1997. While at Tandem, I was the designer and architect of several generations of fault-tolerant computer systems and was the principle architect of the NonStop Cyclone superscalar processor. Since leaving Compaq in 1999, I have worked with several technology companies, including 3Ware and Network Appliance, and have focused in the areas of computer design and biomedical devices.

4. At HP, Tandem, Compaq, 3Ware and Network Appliance my computer design work was done using computer aided design (CAD) tools, with most designs specified in a hardware description language. In fact, the designs used integrated circuits and some involved the creation of new ASICs (application specific integrated circuits) that were manufactured using masks based on the netlists produced by the CAD software.

5. I have authored over 30 publications, including: "The Risk of Data Corruption in Microprocessor-based Systems," *Proc. 23rd International Symposium on Fault-tolerant Computing*, June 1993; and "Reliable Design of High-speed Cache and Control Store Memories," *Proc. 19th Int. Symp. Fault-Tolerant Computing, June 1989*. In 1998, the University of Illinois department of Electrical and Computer Engineering awarded me the Distinguished Alumni Award for "Pioneering Contributions to Fault-tolerant Computer Architecture."

And, in 2001, I was named IEEE Fellow "for contributions to the architecture and design of fault tolerant systems and networks."

6. I am a named inventor on 78 issued U.S. patents. These patents include U.S, Patent No. 5,751,932, entitled "Fail-fast, fail-functional, fault-tolerant multiprocessor system" and U.S. Patent No. 5,390,355, entitled "Computer architecture capable of concurrent issuance and execution of general purpose multiple instructions."

7. I am familiar with the content of U.S. Patent No. 7,296,121 (the "'121 patent"). Additionally, I have reviewed the following: U.S. Patent Application Publication Number 2002/0053004 to Pong ("Pong"); David Chaiken *et al.*, "Directory-Based Cache Coherence in Large-Scale Multiprocessors," *Computer* vol. 24, issue 9 (Jun 1990) ("Chaiken"); Daniel Lenoski *et al.*, "The Directory-Based Cache Coherence Protocol for the DASH Multiprocessor," *ISCA '90 Proceedings of the 17th annual international symposium on Computer Architecture*, pp. 149-159 (May 1990) ("Stanford DASH"); U.S. Patent Number 6,490,661 to Keller *et al* ("Keller"); Jose Duato *et al.*, INTERCONNECTION NETWORKS – AN ENGINEERING APPROACH (1997) ("Duato"); Michael John Sebastian Smith, APPLICATION-SPECIFIC INTEGRATED CIRCUITS (1997) ("Smith"); U.S. Patent No. 7,698,509 to Koster *et al.* ("Koster"); U.S. Patent No. 7,315,919 to O'Krafka *et al.* ("O'Krafka"); U.S. Patent No. 6,338,122 to Baumgartner *et al.*

("Baumgartner"); Anant Agarwal *et al.*, "An Evaluation of Directory Schemes for Cache Coherence," *Conference Proceedings of 15th Annual International Symposium on Computer Architecture* (1988); Louis G. Johnson, "Multiprocessors," ECEN 6253 Lecture Notes (April 28, 2003); Luca Benini and Giovanni De Micheli, "Networks on chips: a new SoC paradigm," *Computer* vol. 35, issue 1 (Jan. 2002) ("Benini"); "HyperTransport™ Technology I/O Link - A High-Bandwidth I/O Architecture" (Jul. 20, 2001) ("HyperTransport"); U.S. Publication No. 2005/0228952 to Mayhew *et al.* ("Mayhew"); and U.S. Patent No. 6,662,277 to Gaither ("Gaither"). I have also reviewed the two Notices of Allowances included in the prosecution history of the '121 patent.

8. Counsel has informed me that I should consider these materials through the lens of one of ordinary skill in the art related to the '121 patent at the time of the earliest purported priority date of the '121 patent, and I have done so during my review of these materials. I believe one of ordinary skill as of November 4, 2002 (the priority date of U.S. Patent No. 7,003,633, to which the '121 patent claims continuation-in-part priority) would have a bachelor's degree in electrical engineering, computer engineering, or computer science and at least two years of experience in the design of multiprocessor systems. I base this on my own personal experience, including my knowledge of colleagues and others at the time.

9. I have no financial interest in either party or in the outcome of this proceeding. I am being compensated for my work as an expert on an hourly basis. My compensation is not dependent on the outcome of these proceedings or the content of my opinions.

10. My opinions, as explained below, are based on my education, experience, and background in the fields discussed above.

11. This declaration is organized as follows:

I. Brief Overview of Relevant Technology

12. A shared-memory multiprocessor is a computer system in which multiple processors share memory. Memory (and I/O devices) are shared by each

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