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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC., HTC CORPORATION, HTC AMERICA, INC.,
SAMSUNG ELECTRONICS CO. LTD,
SAMSUNG ELECTRONICS AMERICA, INC., and
AMAZON.COM, INC.,
Petitioner,

v.

MEMORY INTEGRITY, LLC,
Patent Owner.

Case IPR2015-00172
Patent 7,296,121 B2

Before JENNIFER S. BISK, NEIL T. POWELL, and KERRY BEGLEY, *Administrative Patent Judges*.

BEGLEY, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
37 C.F.R. § 42.108

Apple Inc., HTC Corporation, HTC America, Inc., Samsung Electronics Co. Ltd., Samsung Electronics America, Inc.,[1] and Amazon.com, Inc. (collectively, "Petitioner") filed a Petition requesting *inter partes* review of claims 1–9, 11, 12, and 16–24 of U.S. Patent No. 7,296,121 B2 (Ex. 1001, "the '121 patent"). Memory Integrity, LLC ("Patent Owner") filed a Preliminary Response to the Petition. Paper 11 ("Prelim. Resp.").

Pursuant to 35 U.S.C. § 314(a), an *inter partes* review may not be instituted unless "the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." Having considered the Petition and the Preliminary Response, we determine that there is not a reasonable likelihood that Petitioner would prevail in establishing that the challenged claims of the '121 patent are unpatentable. Therefore, we deny institution of *inter partes* review.

I. BACKGROUND

A. THE '121 PATENT

The '121 patent relates to techniques to reduce memory transaction traffic and to improve data access and cache coherency in systems with multiple processors connected using point-to-point links. Ex. 1001, 1:22–25, 2:39–47. The '121 patent explains that cache coherency problems can arise in a system with multiple processors, each with an individual cache memory, because the system may contain multiple copies of the same data. *Id.* at 1:26–38. For example, if the caches of two different processors have a

[1] The Petition also lists Samsung Telecommunications America, LLC ("STA") as a petitioner. Paper 6 ("Pet."), 1. After the filing of the Petition, however, STA merged with and into Samsung Electronics America, Inc. Paper 10. Thus, STA no longer exists as a separate corporate entity. *Id.*

copy of the same data block and both processors "attempt to write new values into the data block at the same time," then the two caches may have different data values and the system may be "unable to determine what value to write through to system memory." *Id.* at 1:37–45.

The '121 patent discloses a computer system with processing nodes, each with a cache memory, connected by a point-to-point architecture. *Id.* at [57], 2:48–62. The system also includes a "probe filtering unit" that can receive a probe, "[a] mechanism for eliciting a response from a node to maintain cache coherency in a system," from a processing node. *Id.* at [57], 2:52–65, 5:45–47. The probe filtering unit then can evaluate the probe based on probe filtering information, specifically "[a]ny criterion that can be used to reduce the number of clusters or nodes probed," and can transmit the probe to selected processing nodes. *Id.* at [57], 2:52–3:5, 14:50–52; *see id.* at 28:29–58, 29:43–46. The probe filtering unit also may be operable to accumulate responses from the selected processing nodes and to respond to the node from which the probe originated. *Id.* at 3:5–8, 28:59–67, 29:46–51. Figure 18 of the patent is reproduced below.

Figure 18

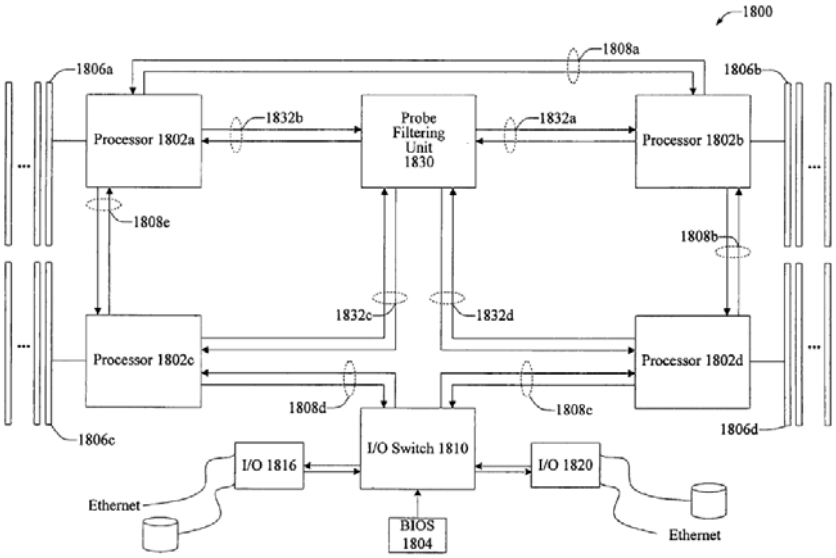

Figure 18 is a diagrammatic representation of a multiple processor system with a probe filtering unit. *Id.* at 3:61–63, 26:58–27:20, Fig. 18. Specifically, Figure 18 depicts multiple processor system 1800 with processing nodes 1802a–d interconnected by point-to-point communication links 1808a–e. *Id.* at 26:58–27:1. System 1800 also includes probe filtering unit 1830 as well as I/O switch 1810, one or more Basic I/O systems ("BIOS") 1804, I/O adapters 1816, 1820, and a memory subsystem with memory banks 1806a–d. *Id.* at 3:61–63, 26:58–27:20, Fig. 18.

B. Illustrative Claim

Claims 1 and 16 are the only independent claims challenged in the Petition. Claim 1 is illustrative of the claimed subject matter and recites:

> 1. A computer system comprising a plurality of processing nodes interconnected by a first point-to-point architecture,
>
> each processing node having a cache memory associated therewith,
>
> the computer system further comprising a probe filtering unit which is operable to receive probes corresponding to memory lines from the processing nodes and to transmit the probes only to selected ones of the processing nodes with reference to probe filtering information representative of states associated with selected ones of the cache memories.

Id. at 30:65–31:7 (line breaks added).

C. Asserted Prior Art

The Petition relies upon the following prior art references, as well as the supporting Declaration of Robert Horst, Ph.D. (Ex. 1014):

U.S. Patent No. 6,490,661 B2 (filed Dec. 21, 1998) (issued Dec. 3, 2002) (Ex. 1006, "Keller");

Daniel Lenoski et al., *The Directory-Based Cache Coherence Protocol for the DASH Multiprocessor*, *in* The 17th Annual

INTERNATIONAL SYMPOSIUM ON COMPUTER ARCHITECTURE 148 (1990) (Ex. 1005, "Stanford DASH");

JOSÉ DUATO ET AL., INTERCONNECTION NETWORKS (1997) (Corrected Ex. 1007, "Duato");

MICHAEL JOHN SEBASTIAN SMITH, APPLICATION-SPECIFIC INTEGRATED CIRCUITS (1997) (Ex. 1008, "Smith"); and

ADVANCED MICRO DEVICES, INC., HYPERTRANSPORT TECHNOLOGY I/O LINK (2001) (EX. 1018, "HYPERTRANSPORT").

D. ASSERTED GROUNDS OF UNPATENTABILITY

Petitioner asserts the following grounds of unpatentability. Pet. 3.

Challenged Claim[s]	Basis	Reference[s]
1–3, 8, 11, 12, 16, 19, 20, and 22	§ 102	Stanford DASH
4–6	§ 103	Stanford DASH and Keller
7	§ 103	Stanford DASH and HyperTransport
9	§ 103	Stanford DASH and Duato
17–24	§ 103	Stanford DASH and Smith

II. ANALYSIS

A. CLAIM INTERPRETATION

We begin our analysis by addressing the meaning of the claims. The Board interprets claims using the "broadest reasonable construction in light of the specification of the patent in which [they] appear[]." 37 C.F.R. § 42.100(b); *see In re Cuozzo Speed Techs., LLC*, 778 F.3d 1271, 1279–82 (Fed. Cir. 2015). We presume a claim term carries its "ordinary and customary meaning," which is "the meaning that the term would have to a person of ordinary skill in the art in question" at the time of the invention. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007) (citation and quotations omitted). This presumption, however, is rebutted when the

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