

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of: Morton et al.

Case Nos.: IPR2015-00159

U.S. Patent No.: 7,296,121

IPR2015-00163

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Title: REDUCING PROBE TRAFFIC IN MULTIPROCESSOR SYSTEMS

REPLY DECLARATION OF DR. ROBERT HORST

1. I have reviewed the “Patent Owner Response” in IPR2015-00159, the “Patent Owner Response” in IPR2015-00163 and the “Declaration of Vojin Oklobdzija, Ph.D. in Support of Patent Owner’s Responses,” each filed on August 11, 2015. I also considered the references cited herein, including, for example: U.S. Patent Application Publication Number 2002/0053004 to Pong (“Pong”) (Ex. 1003); U.S. Patent No. 7,698,509 to Koster *et al.* (“Koster”) (Ex. 1009); Deposition Transcript of Dr. Vojin G. Oklobdzija Vol. 1, November 23, 2015 (Ex. 1026); Deposition Transcript of Dr. Vojin G. Oklobdzija Vol. 2, November 24, 2015 (Ex. 1027); David E. Culler et al., Parallel Computer Architecture: A Hardware/software Approach (1st Ed.) (1998) (Ex. 1028); “InfiniBand Architecture Specification Volume 1 Release 1.0.a” (June 19, 2001) (Ex. 1029); James Laudon and Daniel Lenoski, Proceedings of the 24th Annual International Symposium on Computer Architecture, “The SGI Origin: A ccNUMA Highly Scalable Server” (1997) (Ex. 1030); Excerpts from Merriam-Webster’s Collegiate

Dictionary (10th ed. 1999) (Ex. 2014); Excerpts from Laughton et al., *Electrical Engineer's Reference Book*, pp. 15/3 (16th ed. 2003) (Ex. 2015); and Fong Pong *et al.*, *Design and Performance of SMPs With Asynchronous Caches* (Nov. 1999) (“the Pong whitepaper”) (Ex. 2024)¹. Moreover, I attended the deposition of Dr. Oklobdzija on November 23 and 24, 2015. In my declaration, I am applying the standards and legal principles that I applied when drafting the declaration entitled “Declaration of Dr. Robert Horst” dated October 28, 2014, which were outlined in paragraphs 8 and 40-61 of that document. Based on these principles and my expertise in the relevant technology, I disagree with several inaccurate and/or misleading statements in both the Patent Owner's Responses and Dr. Oklobdzija's August 11, 2015 Declaration. Below, I address some of these statements.

I. Proper Construction of the Term “Programmed”

2. Dr. Oklobdzija asserts that “the broadest reasonable interpretation of the term ‘programmed’ in the context of the ’121 patent refers to a device that has been configured by a sequence of instructions.” Ex. 2016, ¶ 33. Dr. Oklobdzija further asserts that “the broadest reasonable interpretation of ‘programmed’ would not include hardwired logic.” Ex. 2016, ¶ 38. I respectfully disagree, because the

¹ Throughout this declaration I refer to Ex. 1004 as “Pong” or the “Pong prior art reference.” I refer to Ex. 2024 as the “Pong whitepaper.”

term “programmed” is commonly used to describe the design and configuration of hardwired logic.

3. For example, a field programmable gate array (FPGA) is effectively an array of logic gates that can be inter-wired in different configurations according to a manufacturer’s programming. Contrary to Dr. Oklobdzija’s contention that the term “programmed” is limited to devices that execute a series of instructions, a field programmable gate array need not execute any instructions. Rather, a designer specifies a configuration of physical interconnections between the logic gates and transfers the configuration to a storage device. Depending on the type of FPGA, the configuration is either stored in non-volatile storage inside the FPGA, or the configuration is automatically transferred into the FPGA from a non-volatile memory when power is first applied. After initialization, the logic gates within the FPGA perform logical operations corresponding to the configuration and input signals.

4. During his deposition, Dr. Oklobdzija admitted that an FPGA “doesn’t use [a] sequence of instructions.” Ex. 1026, 123:12-20. Dr. Oklobdzija asserted that despite its use of the term “programmable” in the name, FPGAs are not “programmable in a sense of executing a sequence of instructions.” Ex. 1026, 123:21-23. He suggested that “the better, more accurate term would be field configurable logic because it's configured.” Ex. 1026, 123:24-124:1. I have not

heard of FPGAs referred to as “field configurable gate arrays” outside of this legal proceeding, and Dr. Oklobdzija stated he has not either. *See* Ex. 1026, 124:4-11.

5. Contrary to Dr. Oklobdzija’s assertions during the deposition, the ’121 Patent uses the term “programmable,” not “configurable,” when referring to devices that need not execute instructions, teaching that “the cache coherence controller 230 is a specially configured programmable chip such as a programmable logic device or a field programmable gate array.” Ex. 1001, 7:49-52. Moreover, the evidence cited in Dr. Oklobdzija’s declaration states that “in hardwired logic systems the physical interconnections of the elements govern the routes by which data flows between the processing elements and thus the sequence of processing operations performed on the data.” Ex. 2015 (Excerpts from Laughton et al., *Electrical Engineer’s Reference Book*, pp. 15/3 (16th ed. 2003)) at 15/3. This is entirely consistent with the operation of the aforementioned field programmable gate array.

6. Therefore, Dr. Oklobdzija’s definition of the term “programmed” to exclude hardwired systems is inconsistent with the use of the term “programmable” in the ’121 Patent, with the evidence Dr. Oklobdzija cites in his declaration, and with my experience with the term. The Merriam-Webster’s Collegiate Dictionary cited in Patent Owner’s Responses includes a definition for “program” that is “to work out a sequence of operations to be performed by (a

mechanism).” Ex. 2014, p. 931. I believe this definition is consistent with the usage of the term “programmed” in the ’121 Patent and the understanding of a person of ordinary skill in the art. Accordingly, I believe a reasonable interpretation of the term “programmed” is “designed to perform a sequence of operations,” regardless of whether this design is in hardware or software.

II. Reply to Statements Made With Regard to Pong

A. Pong Enables the Instituted Claims of the ’121 Patent

7. In his declaration, Dr. Oklobdzija asserts that “teachings of Pong are confusing, internally inconsistent, and omit key disclosures that would enable one of ordinary skill in the art to practice the limitations of any of the independent claims of the ’121 Patent.” Ex. 2016, ¶ 73. I disagree. The level of implementation detail provided by Pong is consistent with the level of implementation detail provided in similar prior art disclosures of cache coherent systems, such as Koster. A person of ordinary skill in the art would have known how to implement the Pong system without undue experimentation.

8. Pong’s disclosure is organized into a number of embodiments, which are generally demarked by easily identifiable headings. Pong describes various implementations for certain features, but a person of ordinary skill in the art would have been able to distinguish these implementations and understood how they relate to each of the embodiments.

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