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(54) **MAINTAINING CACHE COHERENCY DURING A MEMORY READ OPERATION IN A MULTIPROCESSING COMPUTER SYSTEM**

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(51) **Int. Cl.⁷** **G06F 13/14**

(52) **U.S. Cl.** **711/150; 711/141; 711/130**

(58) **Field of Search** **711/141, 144, 711/145, 146, 130, 119, 150; 709/213, 214, 216, 200, 238**

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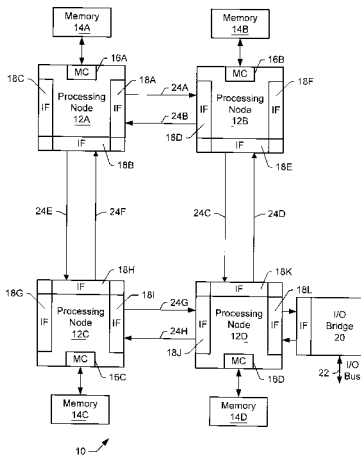
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(57) **ABSTRACT**

A messaging scheme that accomplishes cache-coherent data transfers during a memory read operation in a multiprocessing computer system is described. A source processing node sends a read command to a target processing node to read data from a designated memory location in a system memory associated with the target processing node. In response to the read command, the target processing node transmits a probe command to all the remaining processing nodes in the computer system regardless of whether one or more of the remaining nodes have a copy of the data cached in their respective cache memories. Probe command causes each node to maintain cache coherency by appropriately changing the state of the cache block containing the requested data and by causing the node having an updated copy of the cache block to send the cache block to the source node. Each processing node that receives a probe command sends, in return, a probe response indicating whether that processing node has a cached copy of the data and the state of the cached copy if the responding node has the cached copy. The target node sends a read response including the requested data to the source node. The source node waits for responses from the target node and from each of the remaining node in the system and acknowledges the receipt of requested data by sending a source done response to the target node.

35 Claims, 13 Drawing Sheets



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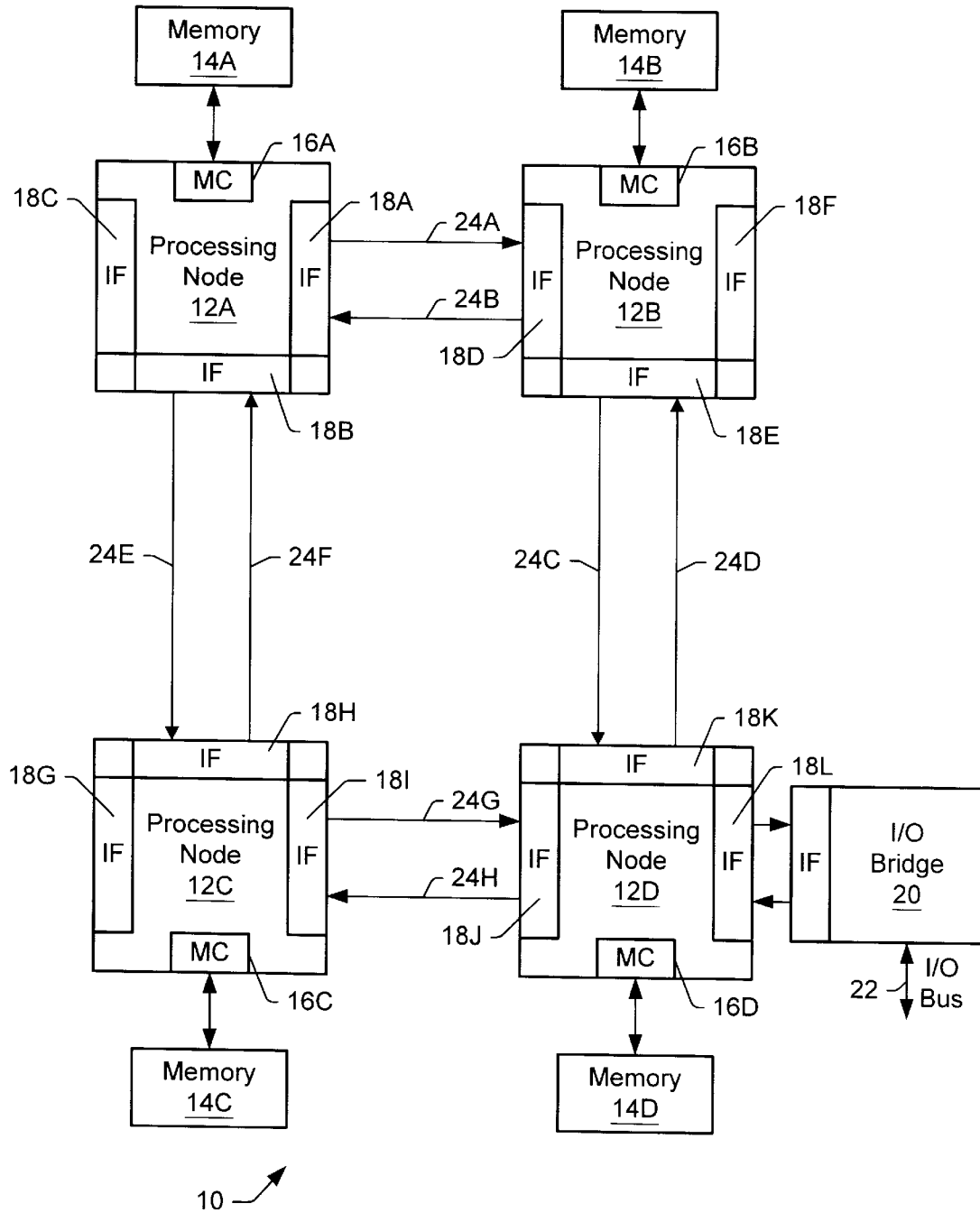


Fig. 1

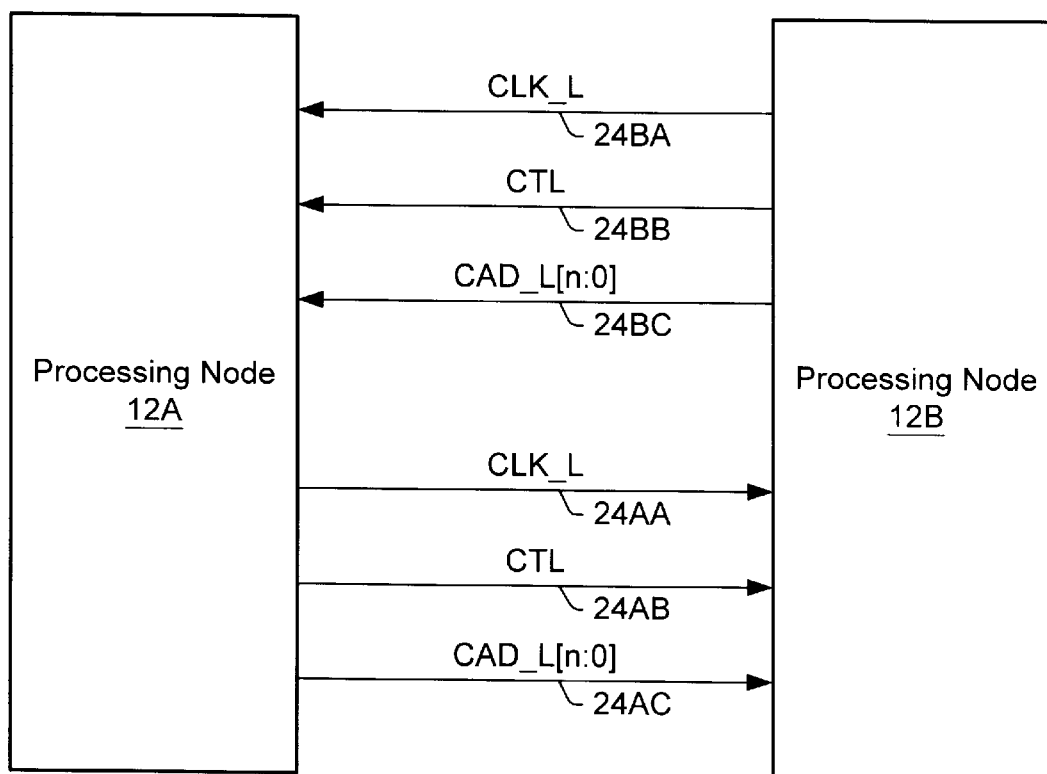


Fig. 2

Bit Time	7	6	5	4	3	2	1	0
1	Reserved or Packet-Specific		CMD[5:0]					
2	Reserved or Packet-Specific							

30 ↗

Fig. 3

Bit Time	7	6	5	4	3	2	1	0
1	DestNode [1:0]		CMD[5:0]					
2	SrcTag [1:0]		SrcNode[3:0]			DestNode [3:2]		
3	Reserved or Packet-Specific		SrcTag[6:2]					
4	Addr[7:0]							
5	Addr[15:8]							
6	Addr[23:16]							
7	Addr[31:24]							
8	Addr[39:32]							

32 ↗

Fig. 4

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