UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC., HTC CORPORATION, HTC AMERICA, INC., SAMSUNG ELECTRONICS CO. LTD, SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG TELECOMMUNICATIONS AMERICA, LLC AND AMAZON.COM, INC.
Petitioners

v.

MEMORY INTEGRITY, LLC
Patent Owner

U.S. Patent No. 7,296,121

Inter Partes Review Case No. 2015-00159

MEMORY INTEGRITY, LLC'S APPENDIX OF CLAIMS IN SUPPORT OF ITS MOTION TO AMEND [37 CFR § 42.121(b)]

LISTING OF PROPOSED SUBSTITUTE CLAIMS

26 (contingent proposed substitute claim for claim 16 if Board determines claim 16 is unpatentable):

A probe filtering unit for use in a computer system comprising a plurality of processing nodes interconnected by a first point-to-point architecture, each processing node having a cache memory associated therewith, the probe filtering unit being operable to receive probes corresponding to memory lines from the processing nodes and to transmit the probes only to selected ones of the processing nodes with reference to probe filtering information representative of states associated with selected ones of the cache memories, wherein said states comprise cache coherency states of a cache coherence protocol, and wherein said cache coherence protocol includes at least a modified state, an exclusive state, a shared state, and an invalid state, and wherein said probe filtering unit is coupled to a coherent protocol interface and a non-coherent protocol interface.

27 (contingent proposed substitute claim for claim 17 if Board determines claim 17 is unpatentable):

An integrated circuit comprising a probe filtering unit for use in a computer system comprising a plurality of processing nodes interconnected by a first point-to-point architecture, each processing node having a cache memory associated therewith, the probe filtering unit being operable to receive probes corresponding to memory lines from the processing nodes and to transmit the probes only to selected ones of the processing nodes with reference to probe filtering information representative of states associated with selected ones of the cache memories, wherein said states comprise cache coherency states of a cache coherence protocol, and wherein said cache coherence protocol includes at least a modified state, an exclusive state, a

shared state, and an invalid state, and wherein said probe filtering unit is coupled to a coherent protocol interface and a non-coherent protocol interface.

28 (contingent proposed substitute claim for claim 18 if Board determines claim 18 is unpatentable):

An integrated circuit comprising a probe filtering unit for use in a computer system comprising a plurality of processing nodes interconnected by a first point-to-point architecture, each processing node having a cache memory associated therewith, the probe filtering unit being operable to receive probes corresponding to memory lines from the processing nodes and to transmit the probes only to selected ones of the processing nodes with reference to probe filtering information representative of states associated with selected ones of the cache memories, wherein said integrated circuit comprises an application-specific integrated circuit, wherein said states comprise cache coherency states of a cache coherence protocol, and wherein said cache coherence protocol includes at least a modified state, an exclusive state, a shared state, and an invalid state, and wherein said probe filtering unit is coupled to a coherent protocol interface and a non-coherent protocol interface.

29 (contingent proposed substitute claim for claim 19 if Board determines claim 19 is unpatentable):

At least one computer-readable medium having data structures stored therein representative of a probe filtering unit for use in a computer system comprising a plurality of processing nodes interconnected by a first point-to-point architecture, each processing node having a cache memory associated therewith, the probe filtering unit being operable to receive probes corresponding to memory lines from the processing nodes and to transmit the probes only to selected ones of the processing nodes with reference to probe filtering information representative of

states associated with selected ones of the cache memories, wherein said states comprise cache coherency states of a cache coherence protocol, and wherein said cache coherence protocol includes at least a modified state, an exclusive state, a shared state, and an invalid state, and wherein said probe filtering unit is coupled to a coherent protocol interface and a non-coherent protocol interface.

30 (contingent proposed substitute claim for claim 20 if Board determines claim 20 is unpatentable):

At least one computer-readable medium having data structures stored therein representative of a probe filtering unit for use in a computer system comprising a plurality of processing nodes interconnected by a first point-to-point architecture, each processing node having a cache memory associated therewith, the probe filtering unit being operable to receive probes corresponding to memory lines from the processing nodes and to transmit the probes only to selected ones of the processing nodes with reference to probe filtering information representative of states associated with selected ones of the cache memories, wherein said data structures comprise a simulatable representation of the probe filtering unit, wherein said states comprise cache coherency states of a cache coherence protocol, and wherein said cache coherence protocol includes at least a modified state, an exclusive state, a shared state, and an invalid state, and wherein said probe filtering unit is coupled to a coherent protocol interface and a non-coherent protocol interface.

31 (contingent proposed substitute claim for claim 21 if Board determines claim 21 is unpatentable):

At least one computer-readable medium having data structures stored therein representative of a probe filtering unit for use in a computer system comprising a

plurality of processing nodes interconnected by a first point-to-point architecture, each processing node having a cache memory associated therewith, the probe filtering unit being operable to receive probes corresponding to memory lines from the processing nodes and to transmit the probes only to selected ones of the processing nodes with reference to probe filtering information representative of states associated with selected ones of the cache memories, wherein the data structures comprise a simulatable representation of the probe filtering unit, wherein said simulatable representation comprises a netlist, wherein said states comprise cache coherency states of a cache coherence protocol, and wherein said cache coherence protocol includes at least a modified state, an exclusive state, a shared state, and an invalid state, and wherein said probe filtering unit is coupled to a coherent protocol interface and a non-coherent protocol interface.

32 (contingent proposed substitute claim for claim 22 if Board determines claim 22 is unpatentable):

At least one computer-readable medium having data structures stored therein representative of a probe filtering unit for use in a computer system comprising a plurality of processing nodes interconnected by a first point-to-point architecture, each processing node having a cache memory associated therewith, the probe filtering unit being operable to receive probes corresponding to memory lines from the processing nodes and to transmit the probes only to selected ones of the processing nodes with reference to probe filtering information representative of states associated with selected ones of the cache memories, wherein the data structures comprise a code description of the probe filtering unit, wherein said states comprise cache coherency states of a cache coherence protocol, and wherein said cache coherence protocol includes at least a modified state, an exclusive state,

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