Consultant Curriculum Vitae

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(Phonetic spelling: Vo-in Oklob-j-a)

Contact:

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Expertise

- Computer System Design and Computer Architecture
- VLSI Circuits and Systems
- System Clocking and Clocked Storage Elements
- Logic Design and Machine Organization
- Low-Power Design and Technology
- Computer Arithmetic: VLSI adders, multipliers arithmetic, crypto processors
- Microprocessor Design
- Design for Testability and Fault-Tolerant Computer Design

Professional Summary

Employment History

From:	2013	**Silicon Analytics Inc.**
To:	Present	San Jose, California
	Position:	Founder and President
		Expertise and tool development for power optimization. Targeting low and ultra-low power design.

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From: 2013 **Skyera Inc.**
To: 2014 San Jose, California
Position: *Senior Director, Processor Development*

From: 1996 **Integration Corp.**
To: Present Berkeley, California
Position: President and CEO
Processor design services: Developed fastest encryption processor for Blue Steel Networks (sold to Broadcom for $150M). Designed and developed network encryption processor for Digital Archways. Design and developed Media and Floating-Point Processor for BOPS Inc.

From: 1992 **Advanced Computer Systems Engineering Laboratory**
To: Present Berkeley, California
Position: *Director*
Conducting research in: Low-Power systems and processor development with implementations in multi-media, cryptography and wireless communication.
Developed a comprehensive family of clocked storage elements and clocking strategies for high performance and low-power applications; optimization method for digital circuits and system design resulting in up to 50% energy savings; the fastest parallel multiplier, adder and method for generation, estimation and comparison of arithmetic structures.

From: 1991 **University of California Davis**
To: Present Davis, CA
Position: Professor Emeritus, 2007-Present
1991-2007: Full Professor, Electrical and Computer Engineering Department

From: 2007 **University of Texas at Dallas**
To: Present Dallas, TX
Position: *Visiting Professor;* Director of Systems and Circuits Group (2007-2010), *Adjunct Professor (2010 – on)*

From: 2005 **Sydney University**
To: 2007 Sydney, Australia
Position: *Computer Engineering Chair and Chair Professor, Department of Electrical and Information Engineering*
(ARC funding $1,900,000).

From: 03/2004 **Ecole Polytechnique Federale de Lausanne, EPFL**
To: 10/2004 Lausanne, Switzerland
Position: *Visiting Professor, Processor Architecture Laboratory*
Developed and taught a new doctoral course in computer arithmetic

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From: 07/2003 **Government of Korea**
To: 12/2003 Seoul, Korea
Position: *Distinguished Visiting Professor,* Korea Information Technology Assessment Program
Established research program in digital media and secured a three year grant in *"Power Minimization for Media Signal Processing"* from the Korean government (appx: $300,000). Established and taught the course titled: *"Digital System Engineering"*.

From: 1998 **University of California at Berkeley**
To: 1990 Berkeley, CA
Position: *Visiting IBM Faculty, Electrical Engineering and Computer Science Department*
Teaching: *Upper level courses:* CS150 Digital System Design, CS152: Computer System Design and Organization. *Graduate courses:* CS252 Computer System Architecture, CS292I VLSI Implementation of Fast Computer Arithmetic. Assisted in preliminary evaluation and preparation of Patterson-Hennessy book "Computer Architecture: A Quantitative Approach".

From: 1996 **Siemens Corporation**
To: 1998 San Jose, CA
Position: Architecture / Circuit Design Manager
Development of Full-Custom high-performance arithmetic units. Chief architect for Siemens / Infineon TriCore line of integrated RISC-DSP controller. Development of and embedded Logic-DRAM processor (32-bit, RISC + DSP). Managed a group of 15 engineers.

From: 1982 **IBM T.J. Watson Research Center**
To: 1991 Yorktown Heights, NY
Position: *Research Staff Member*
My work was in the areas of: *Systems and Architecture, CPU and Floating Point processor design, Circuit design, Design for Testability*
Development and implementation of VLSI RISC architectures:
1. High Performance 801 (first RISC microprocessor) for PC-RT (ROMP-E project).
2. Very high performance Super-Scalar RISC Architecture, RS/6000: floating point processor and system organization. (current PowerPC architecture)
3. Architectural definition and design of VLSI-RISC type processor to be used in a highly parallel super-computer. IBM SP-2.

From: 1979 **Xerox Corp.**
To: 1982 El Segundo, CA
Position: *Member of the Engineering Staff, Microelectronics Center*
Work on the VLSI microprocessors design and diagnostic. Chip set for

the first Workstation – Xerox Alto.

From: 1977 **UCLA**
To: 1982 Los Angeles, CA
Position: *Research Assistant & Senior Research Engineer, Computer Science Department*
Worked on VLSI Design and Testability, VLSI Design Methodology, Fault-Tolerant Computer Design and High Reliability, Computer Arithmetic and Design of Arithmetic Processor.

From: 1974 **University of Belgrade**
To: 1976 Belgrade, Yugoslavia
Position: *Assistant Professor, Electrical Engineering Department*
Research and teaching in Analog and Digital Electronics.

From: 1973 **Institute for Automation and Telecommunications**
To: 1974 Belgrade Yugoslavia
Position: *Research Engineer*
Design of non-standard analog circuitry for the analog part of the state of the art hybrid computer (project with USSR). Design of an Analog Multiplier based on Time Division Concept.

From: 1971 **Institute of Physics**
To: 1973 Belgrade Yugoslavia
Position: *Research Physicist*
Experimental work in plasma physics with extensive use of computer tools for simulation and data acquisition. Written software in Fortran on IBM 360/44 and CDC 6600.

Current and Past Professional Service:

- President, IEEE Circuits and Systems Society (2014 - on)
- President Elect, IEEE Circuits and Systems Society (2013).
- Vice President, Technical Activities, IEEE Circuits and Systems Society (2009-2013)
- General Chair: International Symposium on Low-Power Electronics, 2010.
- Technical Program Chair: International Symposium on Low-Power Electronics, 2008.
- General Chair: International Symposium on Computer Arithmetic, ARITH-20. (Tuebingen, Germany, 2011)
- General Chair: International Symposium on Computer Arithmetic, ARITH-13, Pacific Grove, California, 2007.
- Member of the Board of Governors, IEEE Circuits and Systems Society (2008-present)
- Editorial Board, IEEE MICRO.

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- Editor, Computer Engineering Series, Taylor & Francis.
- Editorial Board Taylor and Francis / CRC Press.
- Distinguished Lecturer of IEEE Solid-State Circuits Society: 2000-on.

Consulting History Industry

From:	10/2014	**Wave Semi, Inc.**
To:	current	Campbell, California
	Duties:	Developing high-speed low-power adders and multipliers, clocking strategy for a proprietary reconfigurable multi-processor.
From:	10/2003	**Samsung Electronics Co. System LSI Division Research Laboratories**
To:	01/2004	Suwon-City, Gyeonggi-Do, Korea
	Duties:	Provided lectures in the area of media processor architecture, clocking and clocked storage elements, power optimization of digital circuits.
From:	05/2002	**Intel Advanced Microprocessor Research Laboratories**
To:	09/2002	Hillsboro, OR
	Duties:	Developed Energy-Delay optimization methodology and tool for adders used in Itanium and P4 processors. Supervised two of my students in wireless 802.11 chip realization project.
From:	1997	**SONY, LSI Systems Laboratories**
To:	2001	San Jose, CA
	Duties:	Architect and project leader for new generation of media processors (reporting to the vice-president of SONY Corp.). Participated in strategic program planning as a member of the board.
From:	1996	**Hitachi Research and Development Laboratories**
To:	1999	San Jose, CA
	Duties:	Low-Power Design. Performed evaluation of clocked storage elements to be used in SH-5 processor. Work in low-power design.
From:	07/1994	**AT&T Bell Laboratories**
To:	09/1994	Holmdel, NJ
	Duties:	Development of new type of Low-Power circuits and logic based on energy-recovery principles.
From:	07/1992	**Sun Microsystems Laboratories**
To:	10/1992	Mountain View, CA
	Duties:	Worked on development of high-performance (1 GOP) super-scalar BiCMOS processor implementation and design.

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