

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC., HTC CORPORATION, HTC AMERICA, INC., SAMSUNG
ELECTRONICS CO. LTD, SAMSUNG ELECTRONICS AMERICA, INC., AND
AMAZON.COM, INC.,
Petitioners,

v.

MEMORY INTEGRITY, LLC,
Patent Owner.

Case IPR2015-00163
Patent 7,296,121

**PETITIONER'S REQUEST FOR REHEARING
PURSUANT TO 37 C.F.R. § 42.71**

I. Introduction

Apple Inc., HTC Corporation, HTC America, Inc., Samsung Electronics Co. Ltd, Samsung Electronics America, Inc., and Amazon.com, Inc. (“Petitioners”) hereby respectfully request rehearing of the May 8, 2015 Decision (“Decision”), granting-in-part and denying-in-part institution of trial. In particular, Petitioners request rehearing of the Board’s decision not to institute review with regard to claim 12. In rendering its Decision, the Board misapprehended the Petition’s application of Koster to the language of claim 12.

First, the Board misapprehended the Petitions’ argument with respect to claim 12, which focused solely on the exemplary *single response* memory transaction disclosed in FIG. 9 of Koster, where a requesting microprocessor 182 received one and only one response from the other microprocessors and, therefore, in this example, necessarily completed its memory transaction after receiving one and only one response. *See* Petition, pp. 34-37. While this example alone satisfies claim 12, as described in the Petition, the Board focused on the fact that Koster’s system additionally supports memory transactions that may involve *multiple responses*, where the “requesting processor 182 could potentially receive *one, two, or three responses* with copies of the requested data” (emphasis added). *See* Decision, p. 23. The ability of Koster’s system to support memory transactions that involve *multiple responses* does not undermine its disclosure of a processor

programmed to function as described in its Fig. 9, which clearly supports memory transactions that involve a *single response* and, as noted in the Petition, such *single response* transactions alone satisfy the features of claim 12.

Second, when explaining its denial of the Petition’s proposed ground for unpatentability of claim 12 based on Koster, the Board criticized the Petition for failing to demonstrate how Koster disclosed a node programmed to perform a “memory transaction ... before all the responses are in.” See Decision, p. 23 (“Petitioner does not point us to any disclosure in Koster that the memory transaction occurs before all the responses are in. See Pet. 23–37. Thus, we are not persuaded that Petitioner nodes is programmed to complete a memory transaction after receiving a first number of responses to a first probe” “and the first number is one,” as required by claim 12.”). It is evident from this portion of the Decision that the Board has misapprehended the plain meaning attributed by the Petition to claim 12, as the Decision introduces the allegedly unmet non-limitations (“before all the responses are in”) into claim 12. Specifically, contrary to the Petition, the Decision reads claim 12 as if that claim requires a node programmed to trigger transactions “before all the responses are in.” In fact, claim 11 merely requires a node programmed to trigger transactions “after receiving a first number of responses,” and claim 12 merely requires the first number to be “one.” Neither the Patent Owner Preliminary Response nor the Petition misapprehends the plain

meaning of claim 12 by introducing this new limitation. Rather, in applying Koster to claim 12, the Petition explains that claim 12 is given its plain meaning and that FIG. 9 of Koster meets claim 12 by disclosing a microprocessor (182) that is programmed to complete a memory transaction after receiving just “one” response to a first probe. *See* Petition, pp. 4-5 and 36. While the Decision embraces this description of Koster, it nevertheless refused to apply Koster to claim 12 based on Koster’s alleged failure to meet the “before all the responses are in” feature that was inappropriately introduced by the Decision into claim 12.

Accordingly, misapprehension and oversight led the Board to deny institution of the proposed ground for unpatentability of claim 12 based on Koster.

II. **Applicable Rules**

37 C.F.R. § 42.71 (d) states:

(d) Rehearing. A party dissatisfied with a decision may file a request for rehearing, without prior authorization from the Board. The burden of showing a decision should be modified lies with the party challenging the decision. The request must specifically identify all matters the party believes the Board misapprehended or overlooked, and the place where each matter was previously addressed in a motion, an opposition, or a reply. A request for rehearing does not toll times for taking action. Any request must be filed:

(1) Within 14 days of the entry of a non-final decision or a decision to institute a trial as to at least one ground of unpatentability asserted in the petition; or

(2) Within 30 days of the entry of a final decision or a decision not to institute a trial.

In accordance with 37 C.F.R. § 42.71 (d)(1), this request is being filed within 14 days of the entry of a decision to institute a trial as to at least one ground of unpatentability asserted in the petition.

III. Requested Relief

Petitioners respectfully request reconsideration of the Board's decision not to institute a review of claim 12 of U.S. Patent No. 7,296,121 as being anticipated by Koster. Petitioners submit that Koster anticipates claim 12 and respectfully request that the Board institute review of claim 12 as part of IPR2015-00163.

IV. Claim

Claim 12 is reproduced below—along with the language of claim 11 from which it depends—with the significant language highlighted:

11. The computer system of claim 1 wherein each of the processing nodes is programmed to complete a memory transaction after receiving a first number of responses to a first probe, the first number being fewer than the number of processing nodes.

12. The computer system of claim 11 wherein the probe filtering unit has temporary storage associated therewith for holding read response data from one of the cache memories, and the first number is one.

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