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Paper 18
Entered: May 8, 2015

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC., HTC CORPORATION, HTC AMERICA, INC.,
SAMSUNG ELECTRONICS CO. LTD,
SAMSUNG ELECTRONICS AMERICA, INC., and
AMAZON.COM, INC.,
Petitioner,

v.

MEMORY INTEGRITY, LLC,
Patent Owner.

Case IPR2015-00163
Patent 7,296,121 B2

Before JENNIFER S. BISK, NEIL T. POWELL, and
KERRY BEGLEY, *Administrative Patent Judges.*

BISK, *Administrative Patent Judge.*

DECISION
Institution of *Inter Partes* Review
37 C.F.R. § 42.108

INTRODUCTION

A. Background

The parties named above[1] ("Petitioner") filed a Petition requesting an *inter partes* review of claims 1–6, 8–12, and 15–25 (the "challenged claims") of U.S. Patent No. 7,296,121 B2 (Ex. 1001, "the '121 patent"). Patent Owner, Memory Integrity, LLC, filed a Preliminary Response. Paper 13 ("Prelim. Resp.").

We have authority to determine whether to institute an *inter partes* review. 35 U.S.C. § 314(b); 37 C.F.R. § 42.4(a). The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted "unless the Director determines . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition."

After considering the Petition and Preliminary Response, we determine that Petitioner has established a reasonable likelihood of prevailing in showing the unpatentability of claims 4–6, 11, and 19–24. Accordingly, we institute *inter partes* review of these challenged claims. We decline to institute an *inter partes* review of claims 1–3, 8–10, 12, 15–18, and 25.

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[1] The Petition also lists Samsung Telecommunications America, LLC ("STA") as a petitioner. Paper 1 ("Pet."), 1. After the filing of the Petition, however, STA merged with and into Samsung Electronics America, Inc. Paper 12. Thus, STA no longer exists as a separate corporate entity. *Id.*

B. Related Matters

The parties indicate that the '121 patent is the subject of several proceedings in the United States District Court for the District of Delaware. Pet. 1–2; Paper 11, 1–2. Petitioner also filed three other petitions seeking *inter partes* review of the '121 patent—IPR2015-00159, IPR2015-00161, and IPR2015-00172. In addition, another party filed a petition seeking *inter partes* review of the '121 patent—IPR2015-00158.

C. The Asserted Grounds of Unpatentability

Petitioner contends that claims 1–6, 8–12, and 15–25 of the '121 patent are unpatentable under 35 U.S.C. §§ 102 and/or 103 based on the following grounds (Pet. 3):[2]

Ground	References	Challenged Claims
§ 102	Koster[3]	1–6, 8, 11, 12, and 16
§ 103	Koster and Duato[4]	9 and 10
§ 103	Koster and O'Krafka[5]	15 and 25
§ 103	Koster and Smith[6]	17–24

D. The '121 Patent

The '121 patent relates to accessing data in computer systems that include more than one processor. Ex. 1001, 1:23–24. Specifically, the '121 patent discusses multiple processor systems with a point-to-point architecture—a cluster of individual processors (also referred to as processing nodes) that are directly connected to each other through point-to-

[2] Petitioner also provides a declaration from Dr. Robert Horst. Ex. 1014.
[3] U.S. Patent No. 7,698,509 B1 (Ex. 1009) ("Koster").
[4] JOSÉ DUATO ET AL., INTERCONNECTION NETWORKS (1997) (Corrected Ex. 1007, "Duato").
[5] U.S. Patent No. 7,315,919 B1 (Ex. 1010) ("O'Krafka").
[6] MICHAEL JOHN SEBASTIAN SMITH, APPLICATION-SPECIFIC INTEGRATED CIRCUITS (1997) (Ex. 1008, "Smith").

point links, each with an associated cache memory. *Id.* at 4:38–40. To increase the number of available processors, multiple clusters may be connected. *Id.* at 4:50–53. Figure 1A is reproduced below.

Figure 1A

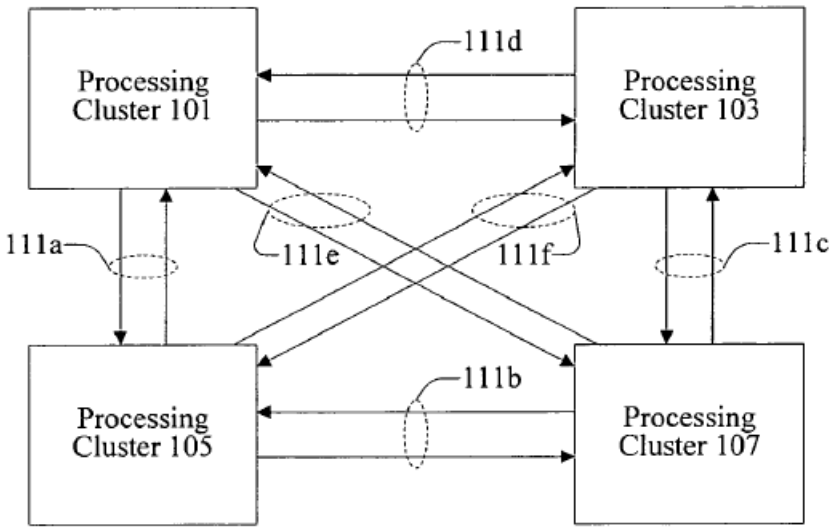

Figure 1A shows an example of a multiple cluster, multiple processor system described by the '121 patent. *Id.* at 6:10–12. Figure 1A includes four processing clusters: 101, 103, 105, and 107, each of which can, in turn, include multiple processors. *Id.* at 6:12–14. The clusters are connected through point-to-point links 111a–f. *Id.* at 6:14–16.

The '121 patent explains that cache coherency problems can arise in such a system, because it may contain multiple copies of the same data. *Id.* at 1:26–38. For example, if the caches of two different processors have a copy of the same data block and both processors "attempt to write new values into the data block at the same time," then the two caches may have different data values and the system may be "unable to determine what value to write through to system memory." *Id.* at 1:37–45. Solutions to cache

coherency problems often involve an increase in communication traffic and a resulting decrease in efficiency. *Id.* at 1:23–26, 2:46–48. The '121 patent discloses "techniques . . . for increasing data access efficiency in a multiple processor system," while also addressing cache coherency. *Id.* at 4:36–38.

The system disclosed by the '121 patent includes a probe filtering unit. *Id.* at 2:52–65. A probe is defined as "[a] mechanism for eliciting a response from a node to maintain cache coherency in a system." *Id.* at 5:45–47. As opposed to a traditional approach of broadcasting probes to all nodes, the probe filtering unit reduces traffic by intercepting the probes and transmitting them only to those nodes that require the information based on probe filtering information, i.e., "[a]ny criterion that can be used to reduce the number of clusters or nodes probed." *Id.* at 2:52–3:5, 14:50–52; *see id.* at 28:29–58, 29:43–46. The probe filtering unit may also accumulate responses from those nodes selected to receive the probes and respond to the node from which the probe originated. *Id.* at 3:5–8, 28:59–67, 29:46–51. Figure 18 of the '121 patent is reproduced below.

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