

Apple, Inc. et al. v. Memory Integrity, L
and
Sony Corp. et al. v. Memory Integrity, L

IPR2015-00158, -00159, -00163
U.S. Patent No. 7,296,121

Patent Owner's Demonstratives

Overview

- The references do not disclose the “states” limitation (cls. 1, 16, and 25)
- The references do not disclose the “programmed” limitation (cl. 11)
- The references do not disclose the “accumulating” limitation (cls. 13 and

The “states” term

- “a probe filtering unit which is operable to ... transmit the probe with reference to probe filtering information representative of states associated with selected ones of the cache memories”
 - ‘121 Pat. cl. 1
- “ the probe filtering unit being operable to ... transmit the probe with reference to probe filtering information representative of states associated with selected ones of the cache memories”
 - ‘121 Pat. cl. 16
- “evaluating the probe with the probe filtering unit ..., the evaluation being done with reference to probe filtering information associated with the probe filtering unit and representative of states associated with selected ones of the cache memories”
 - ‘121 Pat. cl. 25

Construction of “states” term

- ‘121 Patent is directed to the field of cache coherency

BACKGROUND OF THE INVENTION

The present invention generally relates to accessing data in a multiple processor system. More specifically, the present invention provides techniques for reducing memory transaction traffic in a multiple processor system.

Data access in multiple processor systems can raise issues relating to cache coherency. Conventional multiple proces-

‘121 Pat. at 1:26-27 (cited by PO Resp. at 3)

Consequently, it is desirable to provide techniques for improving data access and cache coherency in systems having multiple processors connected using point-to-point links.

‘121 Pat. at 2:39-42 (cited by PO Resp. at 3)

Construction of “states” term

- In the field of cache coherency, “states” refers to cache coherency states

15. Although the term “state” may have many broad and different meanings in general English usage, as well as in the specific field of computer architecture, the term “state” connotes a specific meaning in the context of the field of cache coherency. In the field of cache coherency, the term “state” is understood to a “cache coherency state.” For example, in Sorin et al., *A Primer on Memory Consistency and Cache Coherency*, 2009, at 10.

Oklobdzija PO Resp. Decl. ¶ 15 (-00159, Ex. 2016)

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