

(12) United States Patent Gaither

(54) CACHE SYSTEM WITH GROUPS OF LINES AND WITH COHERENCY FOR BOTH SINGLE LINES AND GROUPS OF LINES

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- (73) Assignce: Hewlett-Packard Development Company, L.P., Houston, TX (US)
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- (52) U.S. Cl. 711/145; 711/141; 711/144;
- 711/146; 711/147; 711/148 (58) Field of Search 711/141, 145, 711/146, 147, 148

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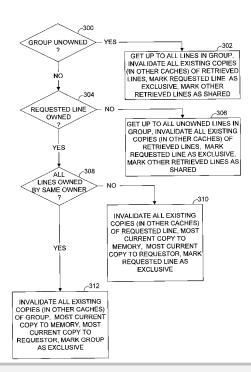
(45) Date of Patent:

Primary Examiner—Donald Sparks Assistant Examiner—Ngoc Dinh (74) Attorney, Agent, or Firm—Augustus W. Winfield

(57) ABSTRACT

In a computer system with caching, memory transactions can retrieve and store groups of lines. Coherency states are maintained for groups of lines, and for individual lines. A single coherency transaction, and a single address transaction, can then result in the transfer of multiple lines of data, reducing overall latency. Even though lines may be transferred as a group, the lines can subsequently be treated separately. This avoids many of the problems caused by long lines, such as increased cache-to-cache copy activity. In one alternative, when a cache memory requests a group of lines, and when the group of lines is partially owned by another cache memory, then the requesting cache receives fewer than all the lines in the requested group.

9 Claims, 5 Drawing Sheets



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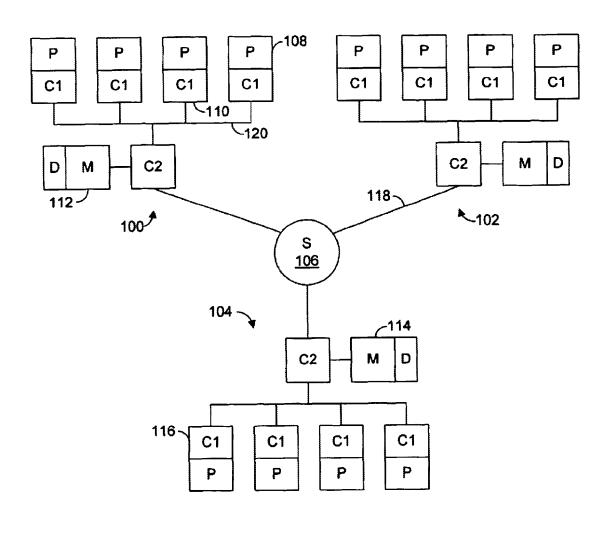


FIG. 1

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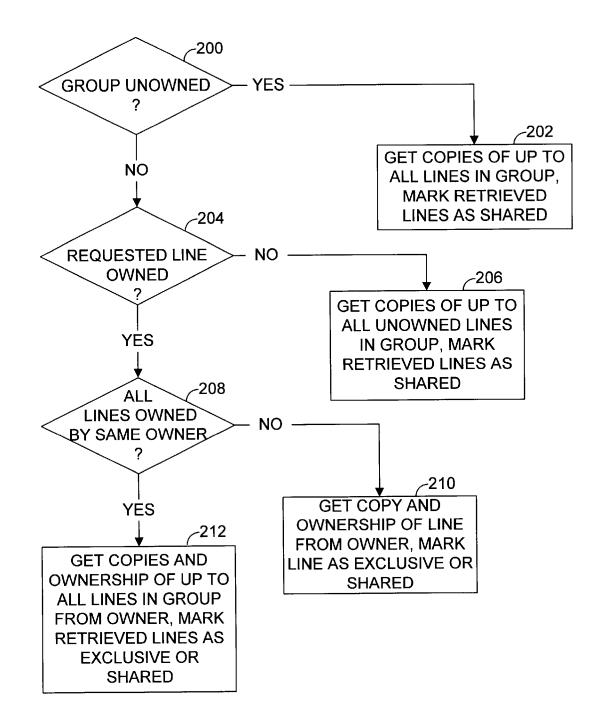


FIG. 2

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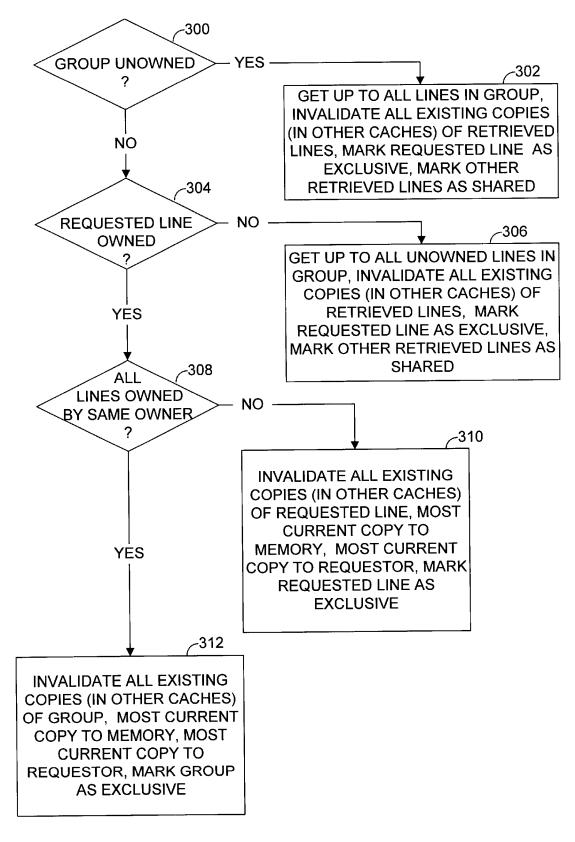


FIG. 3

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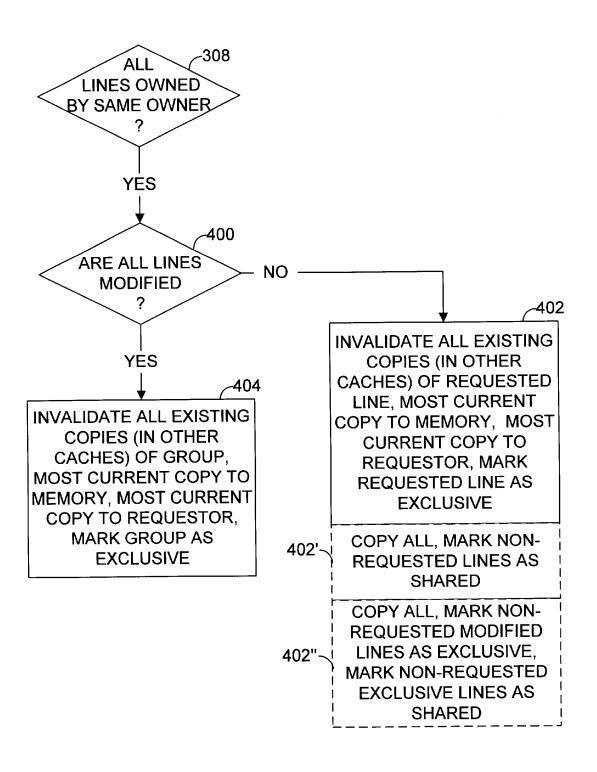


FIG. 4

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