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**Morton et al.**

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- (54) **REDUCING PROBE TRAFFIC IN MULTIPROCESSOR SYSTEMS** 5,524,212 A 6/1996 Somani et al.
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- (75) Inventors: **Eric Morton**, Austin, TX (US); **Rajesh Kota**, Austin, TX (US); **Adnan Khaleel**, Austin, TX (US); **David B. Glasco**, Austin, TX (US) 5,829,032 A 10/1998 Komuro et al.
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- (73) Assignee: **Newisys, Inc.**, Austin, TX (US) 6,073,210 A 6/2000 Palanca et al.
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- (\* ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 250 days. 6,108,737 A 8/2000 Sharma et al.
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(Under 37 CFR 1.47)

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(65) **Prior Publication Data**  
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**Related U.S. Application Data**

(63) Continuation-in-part of application No. 10/288,347, filed on Nov. 4, 2002, now Pat. No. 7,003,633.

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- (51) **Int. Cl.**  
**G06F 12/00** (2006.01)
  - (52) **U.S. Cl.** ..... **711/148**; 711/141
  - (58) **Field of Classification Search** ..... 711/141,  
711/148, 131, 144, 145, 146; 709/206, 213,  
709/216, 217, 218, 219
- See application file for complete search history.

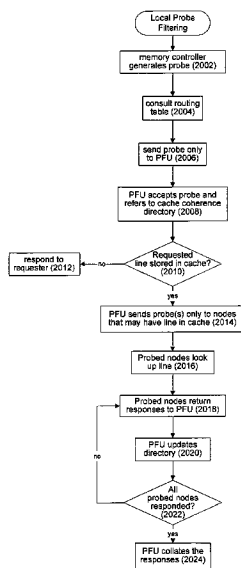
(57) **ABSTRACT**

A computer system having a plurality of processing nodes interconnected by a first point-to-point architecture is described. Each processing node has a cache memory associated therewith. A probe filtering unit is operable to receive probes corresponding to memory lines from the processing nodes and to transmit the probes only to selected ones of the processing nodes with reference to probe filtering information. The probe filtering information is representative of states associated with selected ones of the cache memories.

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**25 Claims, 25 Drawing Sheets**

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Figure 1A

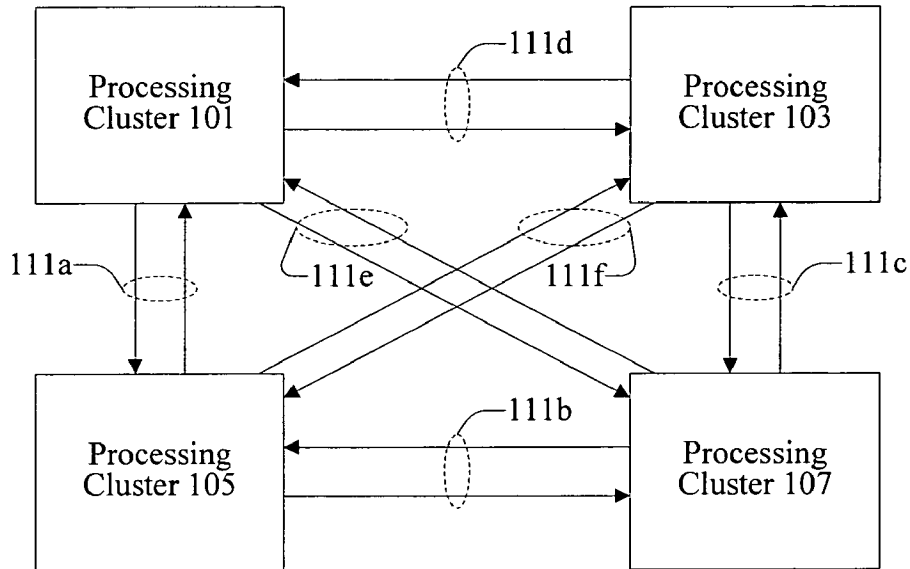


Figure 1B

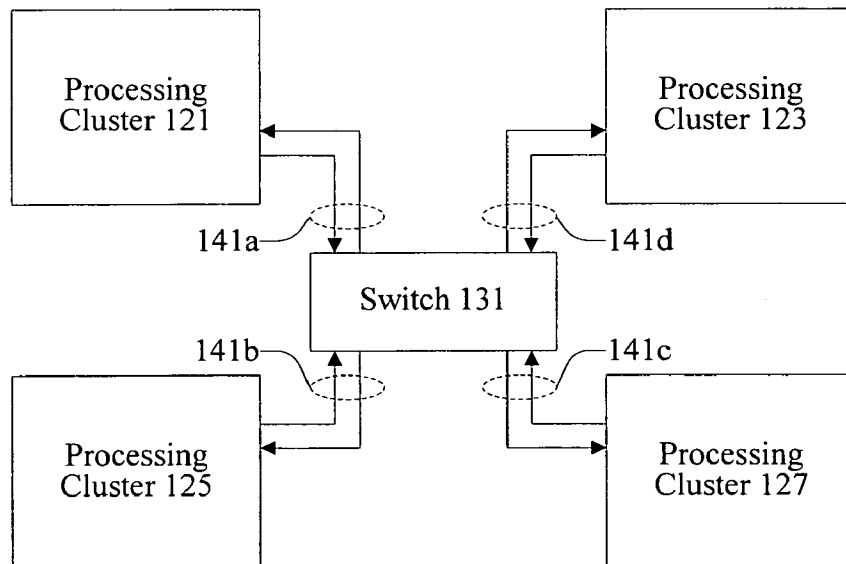


Figure 2

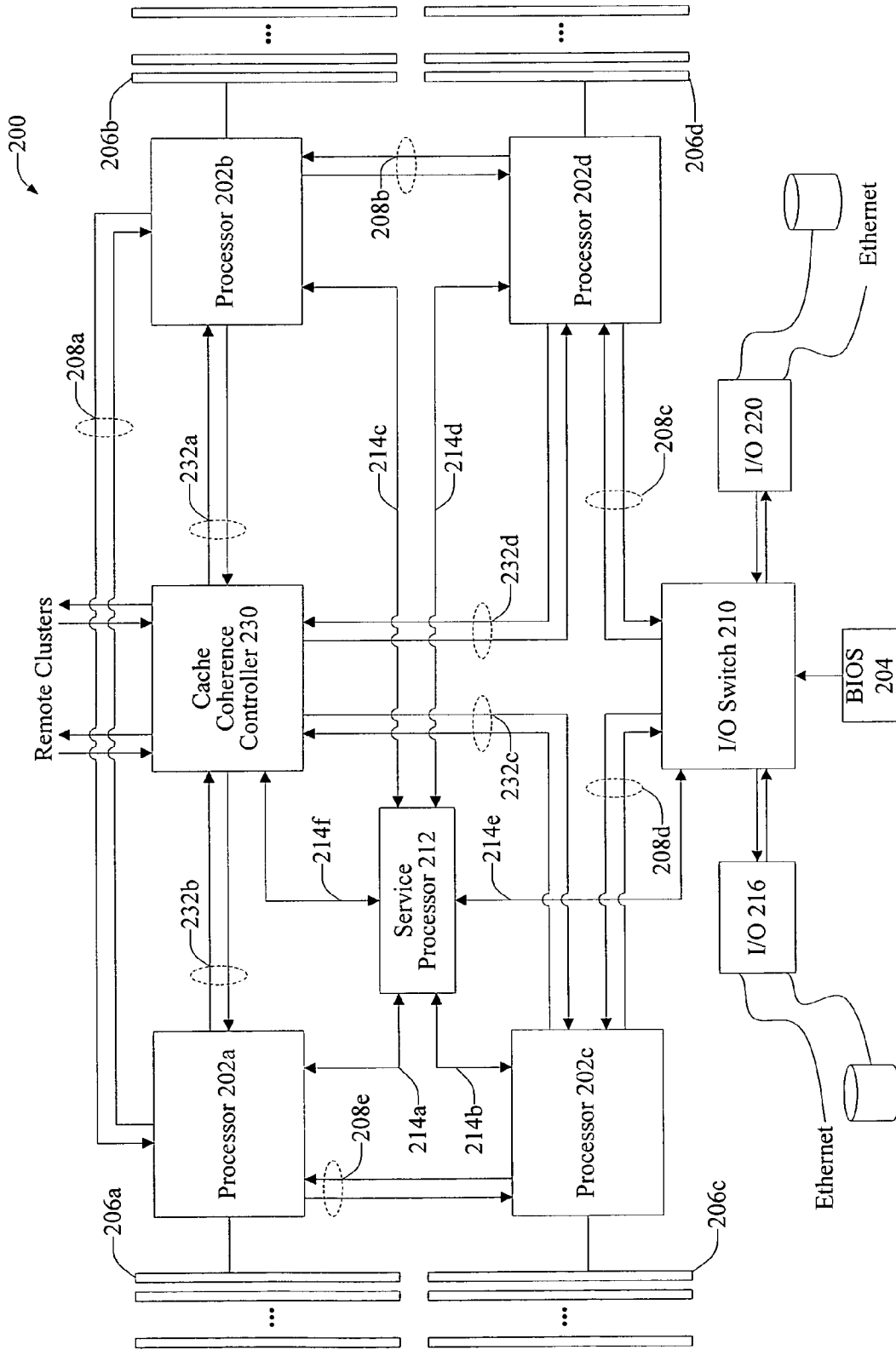
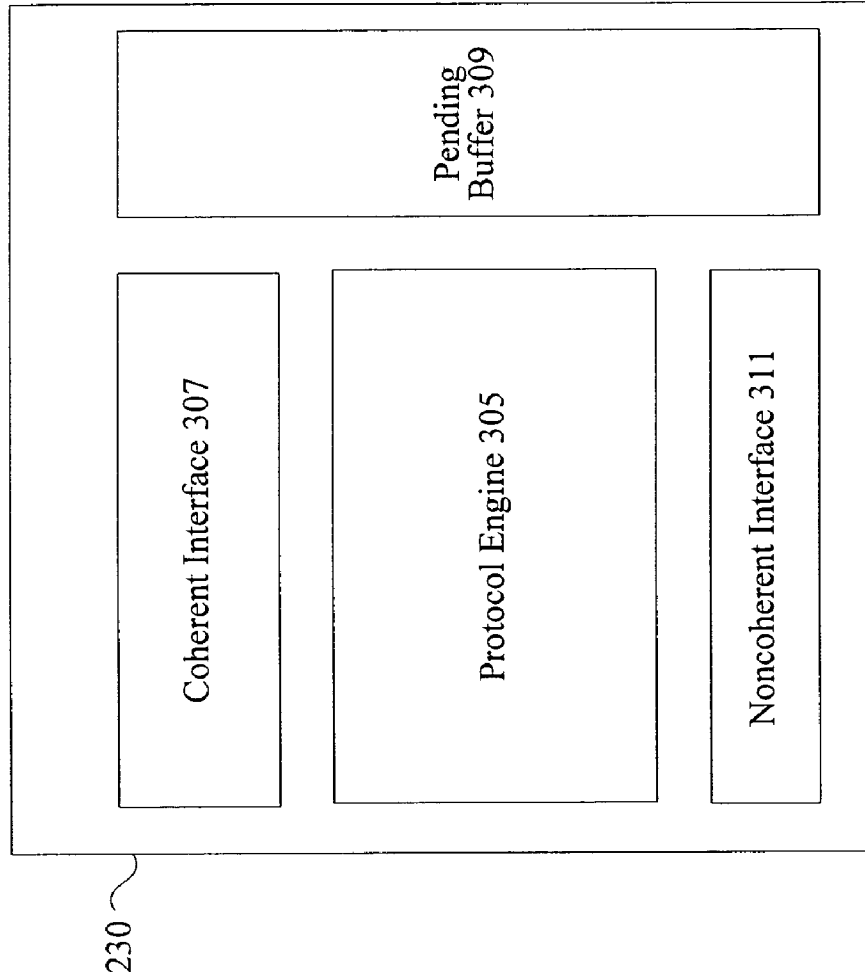


Figure 3



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