UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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APPLE INC., HTC CORPORATION, HTC AMERICA, INC., SAMSUNG ELECTRONICS CO. LTD, SAMSUNG ELECTRONICS AMERICA, INC., AND AMAZON.COM, INC.,
Petitioners,

v.

MEMORY INTEGRITY, LLC,
Patent Owner.

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Case IPR2015-00159
Patent 7,296,121

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PETITIONERS' REPLY TO PATENT OWNER RESPONSE PURSUANT TO 37 C.F.R. § 42.23

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EXHIBITS

APPL-1025	Reply Declaration of Dr. Robert Horst
APPL-1026	Deposition Transcript of Dr. Vojin G. Oklobdzija Vol. 1, November 23, 2015
APPL-1027	Deposition Transcript of Dr. Vojin G. Oklobdzija Vol. 2, November 24, 2015
APPL-1028	David E. Culler et al., Parallel Computer Architecture: A Hardware/software Approach (1st Ed.) (1998)
APPL-1029	"InfiniBand Architecture Specification Volume 1 Release 1.0.a" (June 19, 2001)
APPL-1030	James Laudon and Daniel Lenoski, Proceedings of the 24th Annual International Symposium on Computer Architecture, "The SGI Origin: A ccNUMA Highly Scalable Server" (1997)

I. Introduction

Petitioners submit this Reply to Memory Integrity's ("MI") Response (Paper 25) ("POR"). MI relies upon improper claim construction proposals that have already been considered and rejected in the Board's Institution Decision (Paper 12). MI's proposals ignore the actual claim language and improperly seek to narrow the broadest reasonable construction of the terms without support. Moreover, MI's validity arguments are highly attenuated and reflect a flawed understanding of the Pong reference. As explained in greater detail herein, MI's arguments should be dismissed.

II. Claim Constructions

In an effort to avoid Pong's anticipating disclosure, MI "engages in a *post hoc* attempt to redefine the claimed invention by impermissibly incorporating language appearing in the specification into the claims." *In re Paulson*, 30 F.3d 1475, 1480 (Fed. Cir. 1994). MI's proposals should be rejected as there is no clear definition, in the '121 Patent or elsewhere, that warrants narrowing the terms.

A. "States"

MI's proposed construction improperly seeks to add the very limitation that MI is trying to add with its Motion to Amend. Motion to Amend, p. 1 (seeking to add "wherein said states comprise cache coherency states of a cache coherence protocol" to substitute claims). This attempt by MI belies its argument that "states" is already limited to "cache coherence protocol states." MI should not be

allowed to use claim construction to add claim limitations without amendment.

Further, the Board has already considered intrinsic and extrinsic evidence and found that the term "states … is not limited to cache coherence protocol states and is broad enough to include the condition of presence—i.e., what is stored in cache memory." Institution Decision, pp. 9-10. MI effectively repeats its earlier arguments, essentially citing to the same disclosure within the '121 specification, and has presented no new evidence to diminish the Board's preliminary findings. Additionally, MI's proposal contains the word "state" that it seeks to define, exposing MI's attempt to narrow the broadest reasonable interpretation of this term.

"[T]he PTO should only limit the claim based on the specification or prosecution history when those sources expressly disclaim the broader definition." *In re Bigio*, 381 F.3d 1320, 1325 (Fed. Cir. 2004). Here, none of the passages cited by MI amount to an express disclaimer. To the contrary, as noted in the Institution Decision, all of the examples in the specification to which MI (again) points are couched in broad language stating that "particular implementations may use a different set of states" and "[t]he techniques of the present invention can be used with a variety of different possible memory line states." Institution Decision, p. 9.

Moreover, the claims at issue recite "states associated with selected ones of the cache memories." This recital is broader than the individual "memory line" states described in each of the '121 Patent passages quoted by MI. POR, pp. 5-6

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