AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Delaware on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
	11/26/2013	Delaware

PLAINTIFF	DEFENDANT
MEMORY INTEGRITY, LLC	ARCHOS S.A., AND ARCHOS, INC.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	7,296,121 B2	11/13/2007	MEMORY INTEGRITY, LLC
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In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

Dismissed - See Attached

CLERK	(BY) DEPUTY CLERK	DATE
John A Cerino, Clerk United States District Court 844 N. King Street, Unit 18 Wilmington, DE 19801		9/2/14

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

MEMORY INTEGRITY, LLC,

Plaintiff,

v.

ARCHOS, INC.,

Defendant.

Civil Action No. 1:13-cv-01981-GMS

STIPULATION AND ORDER TO DISMISS WITHOUT PREJUDICE

IT IS HEREBY STIPULATED AND AGREED that all claims and counterclaims between Plaintiff Memory Integrity, LLC and Defendant Archos, Inc. in the above-captioned action are hereby dismissed without prejudice by agreement of the parties pursuant to Rule 41(a)(1)(A)(ii) of the Federal Rules of Civil Procedure, with each party to bear its own costs, expenses, and attorneys' fees.

Dated: August 6, 2014

Respectfully submitted,

DEVLIN LAW FIRM

/s/ Timothy Devlin
Timothy Devlin (#4241)
DEVLIN LAW FIRM
1220 Market Street, Suite 850
Wilmington, DE 19806
(302) 449-9010
tdevlin@devlinlawfirm.com

Attorneys for Plaintiff Memory Integrity, LLC

POTTER ANDERSON & CORROON LLP

By: */s/ Richard L. Horwitz*
Richard L. Horwitz (#2246)
David E. Moore (#3983)
Bindu A. Palapura (#5370)
Hercules Plaza, 6th Floor
1313 N. Market Street
Wilmington, DE 19801
Tel: (302) 984-6000
rhorwitz@potteranderson.com
dmoore@potteranderson.com
bpalapura@potteranderson.com

Attorneys for Defendant Archos, Inc.

IT IS SO ORDERED this 26th day of August, 2014.

United States District Judge

AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 **Director of the U.S. Patent and Trademark Office** **P.O. Box 1450** **Alexandria, VA 22313-1450**	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Delaware on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
	11/26/2013	Delaware

PLAINTIFF	DEFENDANT
MEMORY INTEGRITY, LLC	ARCHOS S.A., AND ARCHOS, INC.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	7,296,121 B2	11/13/2007	MEMORY INTEGRITY, LLC
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In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director **Copy 3—Upon termination of action, mail this copy to Director**
Copy 2—Upon filing document adding patent(s), mail this copy to Director **Copy 4—Case file copy**

AO 120 (Rev. 08/10)

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☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
	11/26/2013	Delaware

PLAINTIFF	DEFENDANT
MEMORY INTEGRITY, LLC	BARNES & NOBLE, INC., NOOK MEDIA, LLC, AND NOOK MEDIA INC

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	7,296,121 B2	11/13/2007	MEMORY INTEGRITY, LLC
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DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
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TO:	Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK

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☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
	11/26/2013	Delaware

PLAINTIFF	DEFENDANT
MEMORY INTEGRITY, LLC	HISENSE INTERNATIONAL CO, LTD. AND HISENSE USA CORPORATION,

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	7,296,121 B2	11/13/2007	MEMORY INTEGRITY, LLC
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☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
	11/26/2013	Delaware

PLAINTIFF	DEFENDANT
MEMORY INTEGRITY, LLC	MICROSOFT CORPORATION

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	7,296,121 B2	11/13/2007	MEMORY INTEGRITY, LLC
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☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT Delaware
PLAINTIFF MEMORY INTEGRITY, LLC		DEFENDANT FUJITSU LIMITED AND FUJITSU AMERICA, INC.,

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	US 7,296,121 B2	11/13/2007	MEMORY INTEGRITY, LLC
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☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT Delaware
PLAINTIFF MEMORY INTEGRITY, LLC		DEFENDANT MOTOROLA SOLUTIONS, INC.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	US 7,296,121 B2	11/13/2007	MEMORY INTEGRITY, LLC
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☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT Delaware
PLAINTIFF MEMORY INTEGRITY, LLC		DEFENDANT GOOGLE INC. AND MOTOROLA MOBILITY, LLC,

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	US 7,296,121 B2	11/13/2007	MEMORY INTEGRITY, LLC
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In the above—entitled case, the following patent(s)/ trademark(s) have been included:

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☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT Delaware
PLAINTIFF MEMORY INTEGRITY, LLC		DEFENDANT SAMSUNG ELECTRONICS CO. LTD.; SAMSUNG ELECTRONICS AMERICA, LLC; AND SAMSUNG TELECOMMUNICATIONS AMERICA, LLC,

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	US 7,296,121 B2	11/13/2007	MEMORY INTEGRITY, LLC
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In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

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☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT Delaware
PLAINTIFF MEMORY INTEGRITY, LLC		DEFENDANT HTC CORPORATION AND HTC AMERICA, INC.,

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	US 7,296,121 B2	11/13/2007	MEMORY INTEGRITY, LLC
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In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
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CLERK	(BY) DEPUTY CLERK	DATE

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☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT Delaware
PLAINTIFF MEMORY INTEGRITY, LLC		DEFENDANT HUAWEI DEVICE USA, INC. AND FUTUREWEI TECHNOLOGIES, INC.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	US 7,296,121 B2	11/13/2007	MEMORY INTEGRITY, LLC
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In the above—entitled case, the following patent(s)/ trademark(s) have been included:

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DOCKET NO.	DATE FILED	U.S. DISTRICT COURT Delaware
PLAINTIFF MEMORY INTEGRITY, LLC		DEFENDANT SONY CORPORATION; SONY ELECTRONICS, INC.; SONY MOBILE COMMUNICATIONS (USA) INC.; AND SONY MOBILE COMMUNICATIONS AB

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	US 7,296,121 B2	11/13/2007	MEMORY INTEGRITY, LLC
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☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT Delaware
PLAINTIFF MEMORY INTEGRITY, LLC		DEFENDANT TOSHIBA CORPORATION; TOSHIBA AMERICA, INC.; TOSHIBA; AMERICA INFORMATION SYSTEMS, INC.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	US 7,296,121 B2	11/13/2007	MEMORY INTEGRITY, LLC
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DOCKET NO.	DATE FILED	U.S. DISTRICT COURT Delaware
PLAINTIFF MEMORY INTEGRITY, LLC		DEFENDANT ZTE CORPORATION AND ZTE (USA) INC.,

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	US 7,296,121 B2	11/13/2007	MEMORY INTEGRITY, LLC
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☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
	11/11/2013	for the District of Delaware

PLAINTIFF	DEFENDANT
MESSAGE NOTIFICATION TECHNOLOGIES LLC	UNIFY INC., F/K/A SIEMENS ENTERPRISE COMMUNICATIONS

PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 5,944,786	8/31/1999	MESSAGE NOTIFICATION TECHNOLOGIES LLC
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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Delaware on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT Delaware
PLAINTIFF MEMORY INTEGRITY, LLC		DEFENDANT AMAZON.COM, INC.

PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 7,296,121	11/13/2007	MEMORY INTEGRITY, LLC
2		
3		
4		
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Delaware on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT Delaware
PLAINTIFF MEMORY INTEGRITY, LLC		DEFENDANT LG ELECTRONICS, INC.; LG ELECTRONICS USA, INC., LG ELECTRONICS MOBILECOMM USA, INC.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	US 7,296,121 B2	11/13/2007	MEMORY INTEGRITY, LLC
2			
3			
4			
5			

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
Mr. David B. Glasco	06/04/2013

RECEIVING PARTY DATA

Name:	Sanmina Corporation
Street Address:	2700 North First Street
City:	San Jose
State/Country:	CALIFORNIA
Postal Code:	95134

PROPERTY NUMBERS Total: 1

Property Type	Number
Patent Number:	7296121

OP $40.00 7296121

CORRESPONDENCE DATA

Fax Number:
Correspondence will be sent via US Mail when the fax attempt is unsuccessful.
Email: swood@farneydaniels.com
Correspondent Name: Stephanie Wood
Address Line 1: 800 S. Austin Ave., Unit 200
Address Line 4: Georgetown, TEXAS 78626

NAME OF SUBMITTER:	Stephanie R. Wood
Signature:	/s/ Stephanie R. Wood
Date:	06/13/2013
	This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 2
source=Glasco to Sanmina Assignment Agreement re '121 Patent (fully executed) (ID 97270)#page1.tif
source=Glasco to Sanmina Assignment Agreement re '121 Patent (fully executed) (ID 97270)#page2.tif

ASSIGNMENT OF PATENT AND PATENT APPLICATION

WHEREAS, I, David B. Glasco, have invented certain new and useful improvements as set forth in U.S. Patent Number 7,296,121 which is entitled "REDUCING PROBE TRAFFIC IN MULTIPROCESSOR SYSTEMS" and which issued from U.S. Patent Application No. 10/966,161 (collectively, the "Patent");

WHEREAS, I have previously assigned any and all of my rights in the Patent to Newisys, Inc. ("Newisys") pursuant to my Proprietary Information and Inventions Agreement dated July 17, 2003, and my Confidentiality, Proprietary Information and Inventions Agreement dated November 6, 2000 (collectively, the "PIIA Agreements");

WHEREAS, I have appointed Newisys and its officers as my agents and attorney-in-fact to execute any documents on my behalf to further the purposes set forth in the PIIA Agreements;

WHEREAS, Newisys has been merged into Sanmina Corporation, a Delaware corporation having a principal place of business at 2700 North First Street, San Jose, California 95134 ("Sanmina") and Sanmina is therefore the successor-in-interest to Newisys;

WHEREAS, Sanmina Corporation desires to obtain a confirmatory assignment confirming that any and all of my rights in the Patent have been assigned to Sanmina as the successor-in-interest to Newisys.

NOW, THEREFORE, for good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, and as a confirmation of my prior assignment of the Patent pursuant to the PIIA Agreements, to the extent that any of the following rights have not already been assigned to Newisys pursuant to the PIIA Agreements, I hereby:

1) Sell, assign and transfer to Sanmina the entire right, title and interest in the Patent and the inventions disclosed in, applications based upon, and patents granted upon (including foreign patents and the right to claim priority), the above-referenced Patent, including all rights to sue for past, present and future infringement of the Patent, the right to collect and receive any damages, royalties, or settlements for such past, present and future infringements, all rights to seek and obtain injunctive or other equitable relief, and any and all causes of action relating to any of the inventions or discoveries claimed in the Patent.

2) Agree that the terms, covenants and conditions of this assignment shall inure to the benefit of Sanmina, its successors, assigns and other legal representatives, and shall be binding upon me, as well as my heirs, legal representatives and assigns.

[Remainder of Page Left Blank Intentionally]

IN TESTIMONY WHEREOF, I hereunto set my hand this 4th day of ~~May~~ June 2013. RKE

David B. Glasco, by Sanmina Corporation, as Agent and Attorney-In-Fact

Robert Eulau
Executive Vice President and Chief Financial Officer
Sanmina Corporation

STATE OF)

COUNTY OF)

On 4 June 2013, before me Melissa K Ritchie,
Notary Public, personally appeared Robert Eulau
proved to me on the basis of satisfactory evidence to be the person whose name is subscribed to the within instrument and acknowledged to me that he executed the same in his authorized capacity, and that by his signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

Signature of Notary

MELISSA K. RITCHIE
Commission # 1981111
Notary Public - California
Santa Clara County
My Comm. Expires Jul 2, 2016

PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
Sanmina Corporation	06/04/2013

RECEIVING PARTY DATA

Name:	Memory Integrity, LLC
Street Address:	1220 N. Market Street, Suite 806
City:	Wilmington
State/Country:	DELAWARE
Postal Code:	19801

PROPERTY NUMBERS Total: 55

Property Type	Number
Patent Number:	7921188
Patent Number:	7107409
Patent Number:	7103725
Patent Number:	7107408
Patent Number:	6986069
Patent Number:	6865595
Patent Number:	7395379
Patent Number:	7653790
Patent Number:	7103636
Patent Number:	7039740
Patent Number:	7155525
Patent Number:	7281055
Patent Number:	7251698
Patent Number:	7577755
Patent Number:	7418517

OP $2200.00 7921188

Patent Number:	8185602
Patent Number:	6934814
Patent Number:	6920532
Patent Number:	6925536
Patent Number:	7162589
Patent Number:	6950913
Patent Number:	7003633
Patent Number:	7103726
Patent Number:	7047372
Patent Number:	7222262
Patent Number:	7337279
Patent Number:	7024521
Patent Number:	7272688
Patent Number:	7346744
Patent Number:	7249224
Patent Number:	7334089
Patent Number:	7103823
Patent Number:	7069392
Patent Number:	7159137
Patent Number:	7395347
Patent Number:	7117419
Patent Number:	7386626
Patent Number:	7577727
Patent Number:	7194660
Patent Number:	7719964
Patent Number:	7296121
Patent Number:	7080284
Patent Number:	7386796
Patent Number:	7225327
Patent Number:	7512971
Patent Number:	7908648
Patent Number:	7561572
Patent Number:	7877629
Patent Number:	7647596
Patent Number:	7694309

	7492716
Patent Number:	8411591
Application Number:	13327483
Application Number:	11258228
Application Number:	13783190

CORRESPONDENCE DATA

Fax Number:

Correspondence will be sent via US Mail when the fax attempt is unsuccessful.

Email: swood@farneydaniels.com
Correspondent Name: Stephanie Wood
Address Line 1: 800 S. Austin Ave., Unit 200
Address Line 4: Georgetown, TEXAS 78626

NAME OF SUBMITTER:	Stephanie R. Wood
Signature:	/s/ Stephanie R. Wood
Date:	06/11/2013
	This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 7
source=2013-06-04 Non-Confidential Version of Sanmina Assignment to Memory Integrity (ID 98283)#page1.tif
source=2013-06-04 Non-Confidential Version of Sanmina Assignment to Memory Integrity (ID 98283)#page2.tif
source=2013-06-04 Non-Confidential Version of Sanmina Assignment to Memory Integrity (ID 98283)#page3.tif
source=2013-06-04 Non-Confidential Version of Sanmina Assignment to Memory Integrity (ID 98283)#page4.tif
source=2013-06-04 Non-Confidential Version of Sanmina Assignment to Memory Integrity (ID 98283)#page5.tif
source=2013-06-04 Non-Confidential Version of Sanmina Assignment to Memory Integrity (ID 98283)#page6.tif
source=2013-06-04 Non-Confidential Version of Sanmina Assignment to Memory Integrity (ID 98283)#page7.tif

ASSIGNMENT

WHEREAS, Sanmina Corporation, with an office at 2700 North First Street, San Jose, California 95134, together with any successors, legal representatives or assigns thereof, called "Assignor") is the owner of and desires to assign the entire right, title, and interest in the Patents listed in the Patent List attached hereto (the "Patents");

AND WHEREAS, Memory Integrity, LLC, having a principal place of business at 4101 County Road 253, Stephenville, Texas 76401 (hereafter, together with any successors, legal representatives or assigns thereof, called "ASSIGNEE") wants to acquire the entire right, title and interest in and to said Patents and all the inventions therein, and Assignor is willing to enter into such assignment.

NOW, THEREFORE, effective on Jan 4, 2013 and in consideration of the sum of One Dollar ($1.00) in hand paid and other good and valuable consideration the receipt of which from ASSIGNEE is hereby acknowledged, Assignor has sold, assigned, transferred and set over, and does hereby sell, assign, transfer and set over to ASSIGNEE the entire right, title and interest in and to the Patents, and any patents, patent applications, foreign patents, foreign patent applications, continuations, continuations–in-part, divisionals, extensions, renewals, reissues and re-examinations claiming priority directly from the Patents, including without limitation, all rights to claim priority directly therefrom, all rights to sue for past, present and future infringement, including the right to collect and receive any damages, royalties, or settlements for such infringements, and all rights to sue for injunctive or other equitable relief.

[Remainder of Page Left Blank Intentionally]

IN TESTIMONY WHEREOF, I hereunto set my hand this 4th day of June, 2013.

Sanmina Corporation
(Assignor)

By _____

Name Robert K Ewin

Title CFO

STATE OF)

COUNTY OF)

On 4 June 2013, before me Melissa K Ritchie, Notary Public, personally appeared Robert Ewin proved to me on the basis of satisfactory evidence to be the person whose name is subscribed to the within instrument and acknowledged to me that he executed the same in his authorized capacity, and that by his signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

Signature of Notary
Melissa K Ritchie

MELISSA K. RITCHIE
Commission # 1961111
Notary Public - California
Santa Clara County
My Comm. Expires Jul 2, 2016

PATENT LIST

Patent	Patent Title	Filing Date
US		
7,921,188	COMPUTER SYSTEM PARTITIONING USING DATA TRANSFER ROUTING MECHANISM	8/16/2001
7,107,409	METHODS AND APPARATUS FOR SPECULATIVE PROBING AT A REQUEST CLUSTER	3/22/2002
7,103,725	METHODS AND APPARATUS FOR SPECULATIVE PROBING WITH EARLY COMPLETION AND DELAYED REQUEST	3/22/2002
7,107,408	METHODS AND APPARATUS FOR SPECULATIVE PROBING WITH EARLY COMPLETION AND EARLY REQUEST	3/22/2002
6,986,069	METHODS AND APPARATUS FOR STATIC AND DYNAMIC POWER MANAGEMENT OF COMPUTER SYSTEMS	7/1/2002
6,865,595	METHODS AND APPARATUS FOR SPECULATIVE PROBING OF A REMOTE CLUSTER	5/28/2002
7,395,379	METHODS AND APPARATUS FOR RESPONDING TO A REQUEST CLUSTER	5/13/2002
7,653,790	METHODS AND APPARATUS FOR RESPONDING TO A REQUEST CLUSTER	5/13/2002
7,103,636	METHODS AND APPARATUS FOR SPECULATIVE PROBING OF A REMOTE CLUSTER	5/28/2002
7,039,740	INTERRUPT HANDLING IN SYSTEMS HAVING MULTIPLE MULTI-PROCESSOR CLUSTERS	7/19/2002
7,155,525	TRANSACTION MANAGEMENT IN SYSTEMS HAVING MULTIPLE MULTI-PROCESSOR CLUSTERS	5/28/2002
7,281,055	ROUTING MECHANISMS IN SYSTEMS HAVING MULTIPLE MULTI-PROCESSOR CLUSTERS	5/28/2002
7,251,698	ADDRESS SPACE MANAGEMENT IN SYSTEMS HAVING MULTIPLE MULTI-PROCESSOR CLUSTERS	5/28/2002
7,577,755	METHODS AND APPARATUS FOR DISTRIBUTING SYSTEM MANAGEMENT SIGNALS	11/19/2002
7,418,517	METHODS AND APPARATUS FOR DISTRIBUTING SYSTEM MANAGEMENT SIGNALS	1/30/2003

8,185,602	TRANSACTION PROCESSING USING MULTIPLE PROTOCOL ENGINES IN SYSTEMS HAVING MULTIPLE MULTI-PROCESSOR CLUSTERS	11/5/2002
6,934,814	CACHE COHERENCE DIRECTORY EVICTION MECHANISMS IN MULTIPROCESSOR SYSTEMS WHICH MAINTAIN TRANSACTION ORDERING	11/5/2002
6,920,532	CACHE COHERENCE DIRECTORY EVICTION MECHANISMS FOR MODIFIED COPIES OF MEMORY LINES IN MULTIPROCESSOR SYSTEMS	11/5/2002
6,925,536	CACHE COHERENCE DIRECTORY EVICTION MECHANISMS FOR UNMODIFIED COPIES OF MEMORY LINES IN MULTIPROCESSOR SYSTEMS	11/5/2002
7,162,589	METHODS AND APPARATUS FOR CANCELING A MEMORY DATA FETCH	12/16/2002
6,950,913	METHODS AND APPARATUS FOR MULTIPLE CLUSTER LOCKING	11/8/2002
7,003,633	METHODS AND APPARATUS FOR MANAGING PROBE REQUESTS	11/4/2002
7,103,726	METHODS AND APPARATUS FOR MANAGING PROBE REQUESTS	11/4/2002
7,047,372	MANAGING I/O ACCESSES IN MULTIPROCESSOR SYSTEMS	4/15/2003
7,222,262	METHODS AND DEVICES FOR INJECTING COMMANDS IN SYSTEMS HAVING MULTIPLE MULTI-PROCESSOR CLUSTERS	8/5/2003
7,337,279	METHODS AND APPARATUS FOR SENDING TARGETED PROBES	6/27/2003
7,024,521	MANAGING SPARSE DIRECTORY EVICTIONS IN MULTIPROCESSOR SYSTEMS VIA MEMORY LOCKING	4/24/2003
7,272,688	METHODS AND APPARATUS FOR PROVIDING CACHE STATE INFORMATION	4/28/2003
7,346,744	METHODS AND APPARATUS FOR MAINTAINING REMOTE CLUSTER STATE INFORMATION	5/9/2003
7,249,224	METHODS AND APPARATUS FOR PROVIDING EARLY RESPONSES FROM A REMOTE DATA CACHE	8/5/2003

7,334,089	METHODS AND APPARATUS FOR PROVIDING CACHE STATE INFORMATION	5/20/2003
7,103,823	COMMUNICATION BETWEEN MULTI-PROCESSOR CLUSTERS OF MULTI-CLUSTER COMPUTER SYSTEMS	8/5/2003
7,069,392	METHODS AND APPARATUS FOR EXTENDED PACKET COMMUNICATIONS BETWEEN MULTIPROCESSOR CLUSTERS	6/12/2003
7,159,137	SYNCHRONIZED COMMUNICATION BETWEEN MULTI-PROCESSOR CLUSTERS OF MULTI-CLUSTER COMPUTER SYSTEMS	8/5/2003
7,395,347	COMMUNICATION BETWEEN AND WITHIN MULTI-PROCESSOR CLUSTERS OF MULTI-CLUSTER COMPUTER SYSTEMS	8/5/2003
7,117,419	RELIABLE COMMUNICATION BETWEEN MULTI-PROCESSOR CLUSTERS OF MULTI-CLUSTER COMPUTER SYSTEMS	8/5/2003
7,386,626	BANDWIDTH, FRAMING AND ERROR DETECTION IN COMMUNICATIONS BETWEEN MULTI-PROCESSOR CLUSTERS OF MULTI-CLUSTER COMPUTER SYSTEMS	6/23/2003
7,577,727	DYNAMIC MULTIPLE CLUSTER SYSTEM RECONFIGURATION	6/27/2003
7,194,660	MULTI-PROCESSING IN A BIOS ENVIRONMENT	6/23/2003
7,719,964	DATA CREDIT POOLING FOR POINT-TO-POINT LINKS	8/12/2004
7,296,121	REDUCING PROBE TRAFFIC IN MULTIPROCESSOR SYSTEMS	10/15/2004
7,080,284	COMPUTER SERVER ARCHITECTURE AND DIAGNOSTIC FRAMEWORK FOR TESTING SAME	7/19/2002
7,386,796	METHOD AND EQUIPMENT ADAPTED FOR MONITORING SYSTEM COMPONENTS OF A DATA PROCESSING SYSTEM	4/1/2003
7,225,327	METHOD, SYSTEM, SOFTWARE AND PROCESSOR FOR INITIALIZING INFORMATION SYSTEMS OPERATING IN HEADLESS AND NON-HEADLESS ENVIRONMENTS	4/11/2003
7,512,971	METHOD AND SYSTEM FOR ENABLING REMOTE ACCESS TO A COMPUTER SYSTEM	1/29/2004

7,908,648	METHOD AND SYSTEM FOR ENABLING REMOTE ACCESS TO A COMPUTER SYSTEM	2/17/2009
7,561,572	SYNTHESIS OF GLOBAL TRANSACTION TAGS	7/20/2005
7,877,629	FACILITATING HANDLING OF EXCEPTIONS IN A PROGRAM IMPLEMENTING A M-ON-N THREADING MODEL	6/1//2005
7,647,596	METHOD FOR SHARING A DATA STORE ACROSS EVENT MANAGEMENT FRAMEWORKS AND SYSTEM COMPRISING SAME	12/8/2005
7,694,309	METHOD FOR FACILITATING UNIFICATION OF EVENT FRAMEWORK VIEWS AND SYSTEM COMPRISING SAME	2/14/2006
7,492,716	METHOD FOR EFFICIENTLY RETRIEVING TOPOLOGY-SPECIFIC DATA FOR POINT-TO-POINT NETWORKS	10/26/2005
8,411,591	METHOD FOR EFFICIENTLY RETRIEVING TOPOLOGY-SPECIFIC DATA FOR POINT-TO-POINT NETWORKS	2/4/2009
Foreign		
Australia 2002324671	COMPUTER SYSTEM PARTITIONING USING DATA TRANSFER ROUTING MECHANISM	8/9/2002
Germany 1561162	METHODS AND APPARATUS FOR MULTIPLE CLUSTER LOCKING	11/4/2003
France 1561162	METHODS AND APPARATUS FOR MULTIPLE CLUSTER LOCKING	11/4/2003
United Kingdom 1561162	METHODS AND APPARATUS FOR MULTIPLE CLUSTER LOCKING	11/4/2003
Italy 1561162	METHODS AND APPARATUS FOR MULTIPLE CLUSTER LOCKING	11/4/2003
United Kingdom 1652091	METHODS AND APPARATUS FOR PROVIDING EARLY RESPONSES FROM A REMOTE DATA CACHE	7/29/2004
China 200480020505.9	METHODS AND APPARATUS FOR PROVIDING CACHE STATE INFORMATION	5/20/2004
China 200480024015.6	DYNAMIC MULTIPLE CLUSTER SYSTEM RECONFIGURATION	6/18/2004

Pending Patent Applications Application/ Serial Number	Patent Application Title	Filing Date
EP 02759329.2	COMPUTER SYSTEM PARTITIONING USING DATA TRANSFER ROUTING MECHANISM	8/9/2002
13/327,483	TRANSACTION PROCESSING USING MULTIPLE PROTOCOL ENGINES IN SYSTEMS HAVING MULTIPLE MULTI-PROCESSOR CLUSTERS	12/15/2011
11/258,228	METHOD FOR EFFICIENTLY CALCULATING DEADLOCK-FREE OPTIMAL ROUTING MATRICES FOR N-NODE POINT TO POINT NETWORKS	10/24/2005
13/783,190	METHOD FOR EFFICIENTLY RETRIEVING TOPOLOGY-SPECIFIC DATA FOR POINT-TO-POINT NETWORKS	3/1/2013

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/966,161	11/13/2007	7296121	NWISP052	6289

22434 7590 10/24/2007

BEYER WEAVER LLP
P.O. BOX 70250
OAKLAND, CA 94612-0250

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 250 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Eric Morton, Austin, TX;
Rajesh Kota, Austin, TX;
Adnan Khaleel, Austin, TX;
David B. Glasco, Austin, TX;

IR103 (Rev. 11/05)

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

22434 7590 07/16/2007

BEYER WEAVER LLP
P.O. BOX 70250
OAKLAND, CA 94612-0250

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Mia Mitchell-Haynes (Depositor's name)
(Signature)
8.7.07 (Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/966,161	10/15/2004	Eric Morton	NWISP052	6289

TITLE OF INVENTION: REDUCING PROBE TRAFFIC IN MULTIPROCESSOR SYSTEMS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$0	$1700	10/16/2007

EXAMINER	ART UNIT	CLASS-SUBCLASS
PEUGH, BRIAN R	2187	711-148000

08/10/2007 CNEGA2 00000001 10966161
01 FC:1501 1400.00 OP
02 FC:1504 300.00 OP
03 FC:1001 30.00 OP

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 Beyer Weaver LLP
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: NEWISYS, INC.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): AUSTIN, TEXAS

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☒ Advance Order - # of Copies 10

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
☒ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge ~~xxxxxxxxx~~(s), any deficiency, or credit any overpayment, to Deposit Account Number 50-0388 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature Joseph M. Villeneuve Date 8/7/2007
Typed or printed name Joseph M. Villeneuve Registration No. 37,460

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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NOTICE OF ALLOWANCE AND FEE(S) DUE

22434 7590 07/16/2007

BEYER WEAVER LLP
P.O. BOX 70250
OAKLAND, CA 94612-0250

EXAMINER	
PEUGH, BRIAN R	
ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 07/16/2007

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/966,161	10/15/2004	Eric Morton	NWISP052	6289

TITLE OF INVENTION: REDUCING PROBE TRAFFIC IN MULTIPROCESSOR SYSTEMS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$0	$1700	10/16/2007

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 07/07) Approved for use through 07/31/2007.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
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or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

22434 7590 07/16/2007

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Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/966,161	10/15/2004	Eric Morton	NWISP052	6289

TITLE OF INVENTION: REDUCING PROBE TRAFFIC IN MULTIPROCESSOR SYSTEMS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$0	$1700	10/16/2007

EXAMINER	ART UNIT	CLASS-SUBCLASS
PEUGH, BRIAN R	2187	711-148000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☐ Issue Fee

☐ Publication Fee (No small entity discount permitted)

☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

☐ A check is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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22434 7590 07/16/2007

BEYER WEAVER LLP
P.O. BOX 70250
OAKLAND, CA 94612-0250

EXAMINER	
PEUGH, BRIAN R	
ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 07/16/2007

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 250 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 250 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 07/07) Approved for use through 07/31/2007.

Notice of Allowability	Application No.	Applicant(s)	
	10/966,161	MORTON ET AL.	
	Examiner	Art Unit	
	Brian R. Peugh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the filing of 10/15/04*.

2. ☒ The allowed claim(s) is/are *1-7 & 9-26, now renumbered as 1-25*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 6/18/07
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on June 18, 2007 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

Specification page 1, line 10: Insert --, now U.S. Patent No. 7,003,633,-- before "for".

Specification page 1, line 14: Insert --, now U.S. Patent No. 7,103,726,-- before "for".

The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

Misnumbered claims 9-26 been renumbered as 8-25 as seen below:

Claim 9, line 1: Replace "9" with –8--.

Claim 10, line 1: Replace "10" with –9--.

Claim 10, line 1: Replace " claim 9" with –claim 8--.

Claim 11, line 1: Replace "11" with –10--.

Claim 11, line 1: Replace "claim 10" with –claim 9--.

Claim 12, line 1: Replace "12" with –11--.

Claim 13, line 1: Replace "13" with –12--.

Claim 13, line 1: Replace "claim 12" with –claim 11--.

Claim 14, line 1: Replace "14" with –13--.

Claim 14, line 1: Replace "claim 12" with –claim 11--.

Claim 15, line 1: Replace "15" with –14--.

Claim 16, line 1: Replace "16" with –15--.

Claim 17, line 1: Replace "17" with –16--.

Claim 18, line 1: Replace "18" with –17--.

Claim 18, line 1: Replace "claim 17" with –claim 16--.

Claim 19, line 1: Replace "19" with –18--.

Claim 19, line 1: Replace "claim 18" with –claim 17--.

Claim 20, line 1: Replace "20" with –19--.

Claim 20, line 2: Replace "claim 17" with –claim 16--.

Claim 21, line 1: Replace "21" with –20--.

Claim 21, line 1: Replace "claim 20" with –claim 19--.

Claim 22, line 1: Replace "22" with –21--.

Claim 22, line 1: Replace "claim 21" with –claim 20--.

Claim 23, line 1: Replace "23" with –22--.

Claim 23, line 1: Replace "claim 20" with –claim 19--.

Claim 24, line 1: Replace "24" with –23--.

Claim 24, line 1: Replace "claim 23" with –claim 22--.

Claim 25, line 1: Replace "25" with –24--.

Claim 25, line 2: Replace "claim 17" with –claim 16--.

Claim 26, line 1: Replace "26" with –25--.**REASONS FOR ALLOWANCE**

The following is an examiner's statement of reasons for allowance: The prior art, including that of Mudgett et al., Razdan et al., Keller et al., and Guo et al. teach related probing systems but fail to teach the combination including the limitation of:

(Claim 1) "...a probe filtering unit which is operable to receive probes corresponding to memory lines from the processing nodes and to transmit the probes only to selected ones of the processing nodes with reference to probe filtering information representative of states associated with selected ones of the cache memories";

(Filed Claim 17, new claim 16) "...the probe filtering unit being operable to receive probes corresponding to memory lines from the processing nodes and to transmit the probes only to selected ones of the processing nodes with reference to probe filtering information representative of states associated with selected ones of the cache memories";

(Filed Claim 26, new claim 25) "...evaluating the probe with the probe filtering unit to determine whether a valid copy of the memory line is in any of the cache

memories, the evaluating being done with reference to probe filtering information associated with the probe filtering unit and representative of states associated with selected ones of the cache memories; transmitting the probe from the probe filtering unit only to selected ones of the processing nodes identified by the evaluating; accumulating probe responses from the selected processing nodes with the probe filtering unit; and responding to the probe from the first processing node only with the probe filtering unit".

The dependent claims are allowable as being dependent upon, and thus incorporating therein, the allowable subject matter of the respective parent claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian R. Peugh whose telephone number is (571) 272-4199. The examiner can normally be reached on Monday-Thursday from 7:00am to 4:30pm. The examiner can also be reached on alternate Friday's from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks, can be reached on (571) 272-4201. The fax phone number

for the organization where this application or proceeding is assigned is (703) 872-9306872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian R. Peugh
Primary Examiner
Art Unit 2187
June 26, 2007

PTO/SB/08a (08-03)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	10966161
	Filing Date	2004-10-15
	First Named Inventor	Morton et al.
	Art Unit	2187
	Examiner Name	PEUGH, BRIAN R.
	Attorney Docket Number	NWISP052

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/BP/	1	6292906		2001-09-18	Fu et al.	
	2	6209055		2001-03-27	Van Doren et al.	
	3	6052769		2000-04-18	Huff et al.	
	4	6073210		2000-06-06	Palanca et al.	
	5	6122715		2000-09-19	Palanca et al.	
	6	6173393		2001-01-09	Palanca et al.	
	7	6205520		2001-03-20	Palanca et al.	
	8	6343347		2002-01-29	Arimilli et al.	

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/BP/	9	6665767		2003-12-16	Comisky et al.	
/BP/	10	6751721		2004-06-15	Webb et al.	

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/BP/	1	20040255002		2004-12-16	Kota et al.	
/BP/	2	20040088494		2004-05-06	Glasco	
/BP/	3	20020083149		2002-06-27	Van Huben et al.	
/BP/	4	20030210655		2003-11-13	Glasco	

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	Attorney Docket Number	NWISP052

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1		☐

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EXAMINER SIGNATURE

Examiner Signature	/Brian Peugh/	Date Considered	06/25/2007

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

PTO/SB/08a (08-03)
Approved for use through 07/31/2006. OMB 0651-0031
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	Attorney Docket Number	NWISP052

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/BP/	1	6760809		2004-07-06	Arimilli et al.	
	2	6148378		2000-11-14	Bordaz et al.	
	3	5829032		1998-10-27	Komuro et al.	
	4	6633945		2003-10-14	Fu et al.	
	5	5394555		1995-02-28	Hunter et al.	
	6	6018791		2000-01-25	Arimilli et al.	
	7	6038652		2000-03-14	Van Huben et al.	
	8	6192451		2001-02-20	Arimilli et al.	

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	Attorney Docket Number	NWISP052

/BP/	9	6330643		2001-12-11	Arimilli et al.	
	10	6334172		2001-12-25	Arimilli et al.	
	11	6405289		2002-06-11	Arimilli et al.	
	12	6542926		2003-04-01	Zalewski et al.	
	13	6631447		2003-10-07	Morioka et al.	
	14	6738870		2004-05-18	Van Huben et al.	
	15	6738871		2004-05-18	Van Huben et al.	
	16	6892282		2005-05-10	Hass et al.	
	17	6189078		2001-02-13	Bauman et al.	
	18	6338122		2002-01-08	Baumgartner et al.	
	19	6760819		2004-07-06	Dhong et al.	

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/BP/	20	6292705		2001-09-18	Wang et al.	
	21	6615319		2003-09-02	Khare et al.	
	22	5195089		1993-03-16	Sindhu	
	23	6865595		2005-03-08	Glasco	
	24	6754782		2004-06-22	Arimilli et al.	
	25	6067603		2000-05-23	Carpenter et al.	
	26	6751698		2004-06-15	Deneroff et al.	
	27	6704842		2004-03-09	Janakiraman et al.	
	28	6633960		2003-10-14	Kessler et al.	
	29	5692123		1997-11-25	Logghe	
	30	6467007		2002-10-15	Armstrong et al.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	10966161
	Filing Date	2004-10-15
	First Named Inventor	Morton et al.
	Art Unit	2187
	Examiner Name	PEUGH, BRIAN R.
	Attorney Docket Number	NWISP052

/BP/	31	6463529		2002-10-08	Miller et al.	
/BP/	32	7003633		2006-02-21	Glasco	

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/BP/	1	20030195939		2003-10-16	Edirisooriya et al.	
	2	20030009623		2003-01-09	Arimilli et al.	
	3	20020052914		2002-05-02	Zalewski et al.	
	4	20020083243		2002-06-27	Van Huben	
	5	20040073755		2004-04-15	Webb et al.	
	6	20030212741		2003-11-13	Glasco	
	7	20030233388		2003-12-18	Glasco et al.	

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/BP/	8	20030182509		2003-09-25	Glasco	
	9	20030182514		2003-09-25	Glasco	
	10	20030182508		2003-09-25	Glasco	
	11	20020007463		2002-01-17	Fung	
	12	20010037435		2001-11-01	Van Doren	
	13	20030196047		2003-10-16	Kessler et al.	
	14	20020087811		2002-07-04	Khare et al.	

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
/BP/	1	WO 0239242	WO		2002-05-16	SOKWOO et al.		☐

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	First Named Inventor	Morton et al.
	Art Unit	2187
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	Attorney Docket Number	NWISP052

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T5
/BP/	1	Application No: 10/288,347 (Now US Patent No. 7,003,633), Notice of Allowance, dated September 12, 2005 (Atty Dkt: NWISP024)	☐
	2	Application No: 10/288,347 (Now US Patent No. 7,003,633), First Office Action, dated November 18, 2004 (Atty Dkt: NWISP024)	☐
	3	KIM et al., "Power-aware Partitioned Cache Architectures", 2001 ACM p. 6467	☐
	4	POWELL et al., "Reducing Set-Associative Cache Energy via Way-Prediction and Selective Direct-Mapping" 2001 IEEE, p. 54-65	☐
	5	CULLER, D.E. , J. P. Singh, A. Gupta, "Parallel Computer Architecture", 1999 Morgan Kaufmann, San Francisco, CA USA XP002277658	☐
	6	TANENBAUM, Andrew, "Computer Networks", Computer Networks, London: Prentice Hall International, GB, 1996, pp. 345-403, XP002155220	☐
	7	Application No: 10/288,347 (Now US Patent No. 7,003,633), Final Office Action, dated May 12, 2005 (Atty Dkt: NWISP024)	☐
	8	U.S. Office Action mailed September 22, 2004, from Application No. 10/106,426 [NWISP002].	☐
	9	U.S. Office Action mailed March 7, 2005, from Application No. 10/106,426 [NWISP002].	☐
	10	U.S. Office Action mailed July 21, 2005, from Application No. 10/106,426 [NWISP002].	☐

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/BP/	11	U.S. Office Action mailed September 23, 2004, from Application No. 10/106,430 [NWISP003].	☐
	12	U.S. Office Action mailed March 10, 2005, from Application No. 10/106,430 [NWISP003].	☐
	13	U.S. Office Action mailed July 21, 2005, from Application No. 10/106,430 [NWISP003].	☐
	14	U.S. Office Action mailed September 22, 2004, from Application No. 10/106,299 [NWISP004].	☐
	15	U.S. Office Action mailed March 10, 2005, from Application No. 10/106,299 [NWISP004].	☐
	16	U.S. Office Action mailed July 21, 2005, from Application No. 10/106,299 [NWISP004].	☐
	17	U.S. Office Action mailed July 20, 2005, from Application No. 10/608,846 [NWISP030].	☐
	18	U.S. Office Action mailed September 9, 2005, from Application No. 10/462,015 [NWISP040].	☐
	19	U.S. Office Action mailed September 9, 2005, from Application No. 10/426,084 [NWISP033].	☐
	20	U.S. Office Action mailed November 2, 2005, from Application No. 10/106/430 [NWISP003].	☐
	21	U.S. Office Action mailed October 5, 2005, from Application No. 10/635,703 [NWISP036].	☐

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	Attorney Docket Number	NWISP052

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Bib Data Sheet

CONFIRMATION NO. 6289

SERIAL NUMBER	FILING OR 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/966,161	10/15/2004 RULE 1.47	711	2187	NWISP052

APPLICANTS

Eric Morton, Austin, TX;
Rajesh Kota, Austin, TX;
Adnan Khaleel, Austin, TX;
David B. Glasco, Austin, TX;

**** CONTINUING DATA ***************************

This application is a CIP of 10/288,347 11/04/2002 PAT 7,003,633

**** FOREIGN APPLICATIONS *********************

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 11/23/2004

Foreign Priority claimed	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
☐ yes ☑ no	TX	25	25	3
35 USC 119 (a-d) conditions met ☐ yes ☑ no ☐ Met after Allowance				
Verified and Acknowledged Examiner's Signature Initials				

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TITLE

REDUCING PROBE TRAFFIC IN MULTIPROCESSOR SYSTEMS

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- ☐ 1.17 Fees (Processing Ext. of time)
- ☐ 1.18 Fees (Issue)
- ☐ Other _____
- ☐ Credit

Issue Classification	Application/Control No. 10/966,161	Applicant(s)/Patent under Reexamination MORTON ET AL.
	Examiner Brian R. Peugh	Art Unit 2187

ISSUE CLASSIFICATION

ORIGINAL		INTERNATIONAL CLASSIFICATION											
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED						
711	148	G	06	F	12	/00					/		
CROSS REFERENCES						/					/		
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)												
711	141					/					/		
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						/					/		
						/					/		
						/					/		

(Assistant Examiner) (Date)

(Legal Instruments Examiner) 7/3/07 (Date)

Brian R. Peugh
Primary Examiner
(Primary Examiner) 6/23/07 (Date)

Total Claims Allowed: 25

O.G. Print Claim(s)	O.G. Print Fig.
1	20

☐ **Claims renumbered in the same order as presented by applicant** ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1		31		61		91		121		151		181
2	2		32		62		92		122		152		182
3	3		33		63		93		123		153		183
4	4		34		64		94		124		154		184
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11	12		42		72		102		132		162		192
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18	19		49		79		109		139		169		199
19	20		50		80		110		140		170		200
20	21		51		81		111		141		171		201
21	22		52		82		112		142		172		202
22	23		53		83		113		143		173		203
23	24		54		84		114		144		174		204
24	25		55		85		115		145		175		205
25	26		56		86		116		146		176		206
	27		57		87		117		147		177		207
	28		58		88		118		148		178		208
	29		59		89		119		149		179		209
	30		60		90		120		150		180		210

Search Notes

Application/Control No.	Applicant(s)/Patent under Reexamination	
10/966,161	MORTON ET AL.	
Examiner	**Art Unit**	
Brian R. Peugh	2187	

SEARCHED			
Class	Subclass	Date	Examiner
711	141,148, 131,144, 145,146	3/21/2007	BRP
709	206,213	3/21/2007	BRP
709	216,217	3/21/2007	BRP
709	218,219	3/21/2007	BRP

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner
711	**148,141**	3/28/2007	**BRP**

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
WEST search (text)	3/21/2007	BRP
Updated WEST search (text)	3/22/2007	BRP
Consulted Kevin Ellis	3/27/2007	BRP
Updated WEST search (text) IEEE search	3/28/2007	BRP

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REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	10966161	Filing Date	2004-10-15	Docket Number (if applicable)	NWISP052	Art Unit	2187
First Named Inventor	Morton et al.			Examiner Name	PEUGH, BRIAN R.		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

☐ Other _____

☒ Enclosed

☐ Amendment/Reply

☒ Information Disclosure Statement (IDS)

☐ Affidavit(s)/ Declaration(s)

☒ Other
Two (2) EFS Web 2.0 Forms with 82 cited references.

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.

☒ The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 500388

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

☐ Applicant Signature

Signature of Registered U.S. Patent Practitioner			
Signature	/Joseph M. Villeneuve/	Date (YYYY-MM-DD)	6/18/07
Name	Joseph M. Villeneuve	Registration Number	37460

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

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	Art Unit	2187
	Examiner Name	PEUGH, BRIAN R.
	Attorney Docket Number	NWISP052

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	1	6760809		2004-07-06	Arimilli et al.	
	2	6148378		2000-11-14	Bordaz et al.	
	3	5829032		1998-10-27	Komuro et al.	
	4	6633945		2003-10-14	Fu et al.	
	5	5394555		1995-02-28	Hunter et al.	
	6	6018791		2000-01-25	Arimilli et al.	
	7	6038652		2000-03-14	Van Huben et al.	
	8	6192451		2001-02-20	Arimilli et al.	

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	9	6330643		2001-12-11	Arimilli et al.	
	10	6334172		2001-12-25	Arimilli et al.	
	11	6405289		2002-06-11	Arimilli et al.	
	12	6542926		2003-04-01	Zalewski et al.	
	13	6631447		2003-10-07	Morioka et al.	
	14	6738870		2004-05-18	Van Huben et al.	
	15	6738871		2004-05-18	Van Huben et al.	
	16	6892282		2005-05-10	Hass et al.	
	17	6189078		2001-02-13	Bauman et al.	
	18	6338122		2002-01-08	Baumgartner et al.	
	19	6760819		2004-07-06	Dhong et al.	

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	20	6292705		2001-09-18	Wang et al.	
	21	6615319		2003-09-02	Khare et al.	
	22	5195089		1993-03-16	Sindhu	
	23	6865595		2005-03-08	Glasco	
	24	6754782		2004-06-22	Arimilli et al.	
	25	6067603		2000-05-23	Carpenter et al.	
	26	6751698		2004-06-15	Deneroff et al.	
	27	6704842		2004-03-09	Janakiraman et al.	
	28	6633960		2003-10-14	Kessler et al.	
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	31	6463529		2002-10-08	Miller et al.	
	32	7003633		2006-02-21	Glasco	

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	1	20030195939		2003-10-16	Edirisooriya et al.	
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	4	20020083243		2002-06-27	Van Huben	
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	6	20030212741		2003-11-13	Glasco	
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	8	20030182509		2003-09-25	Glasco	
	9	20030182514		2003-09-25	Glasco	
	10	20030182508		2003-09-25	Glasco	
	11	20020007463		2002-01-17	Fung	
	12	20010037435		2001-11-01	Van Doren	
	13	20030196047		2003-10-16	Kessler et al.	
	14	20020087811		2002-07-04	Khare et al.	

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	1	WO 0239242	WO		2002-05-16	SOKWOO et al.		☐

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	Attorney Docket Number	NWISP052

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	Application No: 10/288,347 (Now US Patent No. 7,003,633), Notice of Allowance, dated September 12, 2005 (Atty Dkt: NWISP024)	☐
	2	Application No: 10/288,347 (Now US Patent No. 7,003,633), First Office Action, dated November 18, 2004 (Atty Dkt: NWISP024)	☐
	3	KIM et al., "Power-aware Partitioned Cache Architectures", 2001 ACM p. 6467	☐
	4	POWELL et al., "Reducing Set-Associative Cache Energy via Way-Prediction and Selective Direct-Mapping" 2001 IEEE, p. 54-65	☐
	5	CULLER, D.E. , J. P. Singh, A. Gupta, "Parallel Computer Architecture", 1999 Morgan Kaufmann, San Francisco, CA USA XP002277658	☐
	6	TANENBAUM, Andrew, "Computer Networks", Computer Networks, London: Prentice Hall International, GB, 1996, pp. 345-403, XP002155220	☐
	7	Application No: 10/288,347 (Now US Patent No. 7,003,633), Final Office Action, dated May 12, 2005 (Atty Dkt: NWISP024)	☐
	8	U.S. Office Action mailed September 22, 2004, from Application No. 10/106,426 [NWISP002].	☐
	9	U.S. Office Action mailed March 7, 2005, from Application No. 10/106,426 [NWISP002].	☐
	10	U.S. Office Action mailed July 21, 2005, from Application No. 10/106,426 [NWISP002].	☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	10966161
	Filing Date	2004-10-15
	First Named Inventor	Morton et al.
	Art Unit	2187
	Examiner Name	PEUGH, BRIAN R.
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	11	U.S. Office Action mailed September 23, 2004, from Application No. 10/106,430 [NWISP003].	☐
	12	U.S. Office Action mailed March 10, 2005, from Application No. 10/106,430 [NWISP003].	☐
	13	U.S. Office Action mailed July 21, 2005, from Application No. 10/106,430 [NWISP003].	☐
	14	U.S. Office Action mailed September 22, 2004, from Application No. 10/106,299 [NWISP004].	☐
	15	U.S. Office Action mailed March 10, 2005, from Application No. 10/106,299 [NWISP004].	☐
	16	U.S. Office Action mailed July 21, 2005, from Application No. 10/106,299 [NWISP004].	☐
	17	U.S. Office Action mailed July 20, 2005, from Application No. 10/608,846 [NWISP030].	☐
	18	U.S. Office Action mailed September 9, 2005, from Application No. 10/462,015 [NWISP040].	☐
	19	U.S. Office Action mailed September 9, 2005, from Application No. 10/426,084 [NWISP033].	☐
	20	U.S. Office Action mailed November 2, 2005, from Application No. 10/106/430 [NWISP003].	☐
	21	U.S. Office Action mailed October 5, 2005, from Application No. 10/635,703 [NWISP036].	☐

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Signature	/Joseph M. Villeneuve/	Date (YYYY-MM-DD)	2007-06-18
Name/Print	Joseph M. Villeneuve	Registration Number	37460

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	9	6665767		2003-12-16	Comisky et al.	
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(71) Applicant: **MILLENNIAL NET, INC.** [US/US]; One Canal Park, Cambridge, MA 02141 (US).

(72) Inventors: **SOKWOO, Rhee**; 25 Webster Avenue, #305, Sommerville, MA 02143 (US). **SHENG, Liu**; 615 Green Street, Cambridge, MA 02139 (US).

(74) Agents: **KAMERER, Bruce, E.** et al.; Iandiorio & Teska, 260 Bear Hill Road, Waltham, MA 02451-1018 (US).

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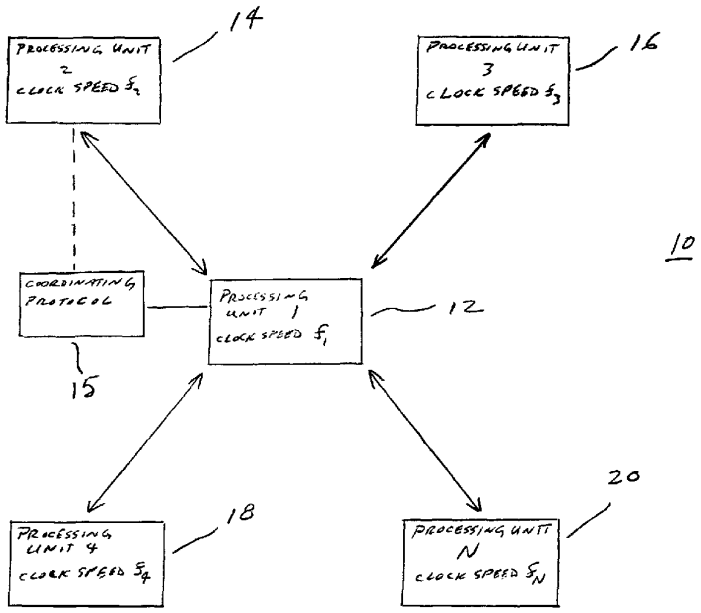
(54) Title: NETWORKED PROCESSING SYSTEM WITH OPTIMIZED POWER EFFICIENCY



(57) Abstract: A multi-processor computing system (10) including a plurality of processing units (12, 14, 16, 18, 20) is provided in which each of the plurality of processing units operates at a clock frequency and a coordinating protocol (15) is used to assign tasks and operations to any of the plurality of processing units in a manner such that the power efficiency of the system is optimized.

WO 02/39242 A1

NETWORKED PROCESSING SYSTEM WITH OPTIMIZED POWER EFFICIENCY

FIELD OF THE INVENTION

This invention relates to a networked processing system with an optimized power efficiency.

RELATED APPLICATIONS

This application claims benefit of U.S. Provisional Application Serial No. 60/244,502 filed October 31, 2000 and entitled I-BEAN: AN INTEGRATED WIRELESS COMMUNICATION AND COMPUTING DEVICE USING NOVEL POWER SAVING ALGORIGHMS FOR MINIMAL ENERGY OPERATIONS.

BACKGROUND OF THE INVENTION

Power efficiency and minimizing power usage are important issues in networked systems, such as communications systems and computing systems. Programs which monitor the usage of various components of a computer system and shut down or minimize some of those components have been used in the past.

However, one area in which such power conservation has not been utilized is with respect to processing units. Whether in networked computer systems or communications systems, optimizing the power efficiency of processing units has not been previously addressed. For example, computer systems with multiple processors operate all processors in parallel at the same time to improve overall system performance without consideration to the power usage involved.

In multiple processor systems, specific tasks such as disk operations, display operations and keyboard input may be assigned to each processor. Another method of improving performance is to assign specific programs, such as word processing and spreadsheet programs, to separate processors. What these systems fail to address is the power used when the processor units are idling. Even when idling, processors are using power with every tick of the processor clock. For high speed processors, this can result in a substantial power usage.

This problem is particularly evident in portable units where the power is limited to that which is available from batteries. One solution used in laptop computers is to slow the processor speed when the laptop computer is running on battery. For example, a processor chip may operate at 1GHz when the computer is connected to an AC power outlet and at 500MHz when running on the internal battery. This results in a significant impact on the performance of the system.

Likewise, communications systems such as cellular phones experience considerable idle time during which power continues to be used in order to keep the system ready to transmit or receive signals. This use of power even when idling causes portable, battery-powered units to require frequent recharging.

SUMMARY OF THE INVENTION

It is therefore an object of this invention to provide a networked processing system in which power usage is minimized.

It is a further object of this invention to provide a networked processing system in which performance is optimized.

It is a further object of this invention to provide a multi-tasking, multiple

processor system in which the power efficiency is optimized.

It is a further object of this invention to provide a self-contained, miniaturized computer with a built in power source, flash memory, digital I/O interface and radio frequency (RF) transceiver for bi-directional communication.

The invention results from the realization that, in a multi-tasking, multi-processor environment, the power efficiency of the system can be optimized by coordinating the usage of processing units such that tasks are run on the appropriate speed processing unit and unused processing units are placed in sleep mode.

This invention features a networked computing system with improved power consumption comprising a plurality of processing units including at least first and second processing units. A coordinating protocol is operative on the first and second processing units and controls the operation of the system such that the power consumption of the system is minimized.

In a preferred embodiment, the first and second processing units are interconnected. The first processing unit operates at a first clock frequency, and the second processing unit operates at a second clock frequency. The first clock frequency may be lower than the second clock frequency.

The first processing unit assigns a task to the first or second processing units based on the clock frequency required to run the task such that the minimum power is used. The first processing unit may instruct the second processing unit to enter a minimum power usage mode. The first processing may activate the second processing unit from the minimum power usage mode when a task is to performed by the second processing unit. The first processing unit may transfer the coordinating protocol to the second processing unit.

The processing units may be communications device which may be bi-directional communications devices. The first processing unit may instruct the second processing unit to enter a minimum power usage mode for a preprogrammed time. The second processing unit may poll the first processing unit after the preprogrammed time. The preprogrammed time may be variable.

This inventions also provides a multiple processor computer system comprising a plurality of processing units, each of the plurality of processing units operating at a clock frequency. A first processing unit operates at a clock frequency lower than the remaining processing units. A coordinating protocol is operable on the first processing unit and coordinates the operation of the system such that the power efficiency is optimized.

In a preferred embodiment, each of the plurality of processing units operates at a different clock frequency. The first processing unit may transfer the coordinating protocol to a second processing unit of the plurality of processing units. The second processing unit may transfer the coordinating protocol to any of the plurality of processing units.

This invention also features a wireless communication system comprising a base unit and a plurality of terminal units in communication with the base unit. Each of the plurality of terminal units has a duty cycle. The base unit controls the duty cycle of each of the plurality of terminal units to optimize the power efficiency of the system.

In a preferred embodiment, the base unit may instruct at least one of the terminal units to enter a minimum power consumption mode for a preprogrammed time. The base unit and the plurality of terminal units may be bi-directional. The

terminal unit may poll the base unit after the preprogrammed time.

This invention also features a method for optimizing the power efficiency of a multi-processor computer system including the steps of providing a plurality of processing units including at least first and second processing units, each processing unit operating at a clock frequency, and operating a coordinating protocol on the first processing unit. The coordinating protocol is operative to receive a request to perform a task, determine to which of the processing units to assign the task, and assign the task to one of the plurality of processing units. The coordinating protocol determines which processing unit to which a task is to be assigned based on optimizing the power efficiency of the system.

The method may also include the steps of transferring the coordinating protocol from the first processing unit to the second processing unit based on the speed required to run the coordinating protocol. The coordinating protocol may be further transferred from the second processing unit to any of the plurality of processing units based on the speed required to run the coordinating protocol.

This invention also features a self-contained, miniaturized computer system including first and second processing units, the first processing unit including a coordinating protocol operable to coordinate the operation of the first and second processing units, a power source, a flash memory module and a RF transceiver, wherein the coordinating protocol assigns tasks to the first and second processing units to optimize the power efficiency of the system.

In a preferred embodiment, the first processing unit operates at a clock frequency of 32 kHz and the second processing unit operates at a clock frequency of 4 MHz. The power source may be a battery.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects, features and advantages will occur to those skilled in the art from the following description of a preferred embodiment and the accompanying drawings, in which:

Fig. 1 is a schematic diagram of a networked processing system according to the subject invention;

Fig. 2 is a block diagram of a bi-directional wireless communication system according to the subject invention;

Fig. 3 is a timing diagram illustrating the transfer of the coordinating protocol among processing units according to the subject invention;

Fig. 4 is a block diagram of the method of the subject invention; and

Figs. 5A, 5B and 5C are block schematic diagrams of a self-contained computer according to the subject invention.

PREFERRED EMBODIMENT

Networked processing system 10, Fig. 1, includes a number of interconnected processing units 12, 14, 16, 18, and 20. There should be at least two interconnected processing units, and there may be any number N of these processing units in system 10. Each processing unit operates at a given clock frequency, f_1, f_2, f_3, f_4,...f_N, respectively. The clock frequencies may all be the same, one or more of the clock frequencies may be the same, or all of the clock frequencies may be different. In a preferred embodiment, each processing unit operates at a different clock frequency, with $f_1<f_2<f_3<f_4<...f_N$.

Processing units 12, 14, 16, 18 and 20 may be central processing units (CPUs) used in many desktop and portable computers today. These processing units may be networked externally, i.e., one or more processing unit may be located in a separate enclosure, or they may be networked internally, i.e., the processing units may be located on a single circuit board or interconnected via an internal data bus in the same computer enclosure.

In operation, processing unit 12 includes a coordinating protocol 15 which is used to control the operation of system 10 by assigning tasks and operations to various processing units based upon the speed required to perform a given task of function. Coordinating protocol 15 is designed to assign tasks to the various processing units with the result being the optimization of the power efficiency of system 10.

For example, the coordinating protocol will allow processing unit 12 to assign a given task or operation to itself or to any other processing unit 14, 16, 18 or 20 based upon the speed requirements of the task or operation and the clock frequencies of the various processing units. Tasks and operations which require lower clock frequencies, which may include such tasks as refreshing a display or operations such as processing keyboard entries, will be assigned to processing units with lower clock frequencies. Because those processing units operate at lower clock frequencies, the power efficiency of the system as a whole will be optimized. When the task load of the system is low enough, processing units may even be shut off or placed into a "sleep" mode to further optimize the power efficiency of the system. One processing unit will always need to remain active to run the coordinating protocol so it may reactivate any processing units which have been shut down.

In a preferred embodiment, the coordinating protocol may be transferred from one processing unit to another processing unit. As shown in Fig. 3, there are N processing units 50, 52, 54, each operating at a respective clock frequency of f_1, f_2,...f_N, with $f_1 < f_s < ... f_N$. Processing unit 50 is the "watchdog", i.e., the processing unit that runs the coordinating protocol, from time T_0 to time T_4. During that period, processing unit 50 activates processing unit 52 at time T_1, deactivates processing unit 52 at time T_2, and activates processing unit 54 at time T_3. At time T_4, processing unit 50 activates processing unit 52 and transfers the coordinating protocol to processing unit 52 which then becomes the "watchdog." Processing unit 52 deactivates processing units 50 and 54 at time T_5, reactivates processing unit 54 at time T_6, and reactivates processing unit 50 at time T_7. Processing unit 52 transfers the coordinating protocol back to processing unit 50 time at T_7, whereby processing unit 50 resumes the "watchdog" responsibility. Finally, processing unit 50 deactivates processing units 52 and 54 at time T_8.

Transferring the coordinating protocol between processing units is useful when the coordinating protocol itself requires a higher clock frequency than that of the lowest clock frequency available. For example, if the number of tasks requested is high enough, the coordinating protocol may require a clock frequency higher than that of the lowest clock frequency available to efficiently and effectively handle the assignment of the tasks to various processing units. Normally, the power efficiency is generally optimized when the coordinating protocol is run by the processing unit with the lowest clock frequency as this processing unit uses the minimum power when idling due to the low clock frequency.

One application of a computing system where this invention is particularly

useful is laptop, or other portable, computers. By using multiple processing units in a laptop combined with the coordinating protocol of this invention, it is possible to optimize the power consumption of the laptop computer such that the battery life is maximized.

In another embodiment, communications system 30, Fig. 2, includes base station 32 and at least one portable communications device 34. System 30 may include a plurality of M portable communications devices 34, 36, 38, 40, 42, and 44. Base station 32 is usually connected to a continuous power supply (not shown) such that the power efficiency of base station 32 is not relevant. However, portable communications device 34 (and 36, 38, 40, 42, and 44 in a multi-point system) are usually powered by batteries which have a finite amount of power. Therefore, optimizing the power efficiency of the system, and particularly of the portable communications device(s), is important. Even so, such optimization must also allow for the communications system to operate effectively, i.e., to be able to send and/or receive signals without significant delay.

In one embodiment, base station 32 is bi-directional and portable communications devices 34, 36, 38, 40, 42 and 44 are receive only devices. Base station 32 includes a coordinating protocol which controls the operation of the portable communications devices. For example, base station 32 controls the duty cycle of the portable communications devices by placing one or more of the portable communications devices in a minimum power usage mode for a preprogrammed time. After the preprogrammed time, the portable communications device automatically returns to the standby mode awaiting another signal. The minimum power usage mode uses less power than the standby mode. By placing a portable communications

devices into the minimum power usage mode, the power efficiency of that portable communications device is optimized.

The preprogrammed time may be variable. For example, if a particular portable communications device is required to be active very infrequently, the preprogrammed time is longer than for a portable communications device that is required to be used more frequently. This allows for the maximum efficiency in the power consumption of the system as a whole. Also, if a particular task is run less frequently, the preprogrammed time for a portable communications device on which that task is to be run may be longer than for a portable communications device on which a task that is run more frequently.

In another embodiment, portable communications devices 34, 36, 38, 40, 42, and 44 are also bi-directional. In this embodiment, base station 32 may put a portable communications device into minimum power mode for a preprogrammed time. However, because the portable communications device is bi-directional, after the preprogrammed time, the portable communications device may poll base station 32 to notify the base station that the portable communications device is once again in the standby mode. This allows base station 32 to transmit any signals which may have been queued up during the preprogrammed time.

In another embodiment, computer 60, Figs. 5A-5C, is a self-contained, miniaturized computer. Computer 60 includes first processing unit 62, RF transceiver 64, second processing unit 66 (Fig. 5B), low clock frequency crystal 68, high clock frequency crystal 70 and I/O connector 72 all mounted on circuit board 74. Power source 76, Fig. 5C, for example a battery, may be attached to circuit board 74.

The small size and low power consumption of computer 60 allows computer

60 to operate from battery 70 for its entire life span. In a preferred embodiment, first processing unit 62 operates at a clock frequency of 32 kHz, and second processing unit 66 operates at a clock frequency of 4 MHz. A coordinating protocol operates so that computer 60 may perform signal processing and RF transmission with optimum power efficiency. Such self-contained, miniaturized computers are useful in communications systems and locally networked computer systems.

A method for optimizing the power efficiency of a multi-processor computer system is also provided. Step 80 of providing a plurality of processing units, Fig. 4, includes providing at least first and second processing units. Each of the processing units operates at a clock frequency. In a preferred embodiment, the clock frequencies of each of the plurality of processing units is different, although this is not a necessary limitation. Step 82 of operating a coordinating protocol on the first processing unit includes receiving a request to perform a task, determining to which processing unit to assign the task, and assigning the task to a processing unit. In a preferred embodiment, step 84 of transferring the coordinating protocol from the first processing unit to the second processing unit may be included. In a further embodiment, step 86 of transferring the coordinating protocol from the second processing unit to any of the plurality of processing units may be included. Optional steps 84 and 86 provide for transferring the coordinating protocol based on the speed required to operate the coordinating protocol. For example, if the number of task requested is high, a higher clock speed processing unit may be required to run the coordinating protocol.

Although specific features of the invention are shown in some drawings and not in others, this is for convenience only as each feature may be combined with any

or all of the other features in accordance with the invention. The words "including", "comprising", "having", and "with" as used herein are to be interpreted broadly and comprehensively and are not limited to any physical interconnection. Moreover, any embodiments disclosed in the subject application are not to be taken as the only possible embodiments.

Other embodiments will occur to those skilled in the art and are within the following claims:

What is claimed is:

CLAIMS

1. A networked computing system with improved power consumption comprising:

a plurality of processing units including at least first and second processing units, said first processing unit including a coordinating protocol,

wherein the first processing unit utilizes the coordinating protocol to control the operation of the system such that the power consumption of the system is minimized.

2. The networked computing system of claim 1 wherein the first and second processing units are physically interconnected.

3. The networked computing system of claim 2 wherein the first processing unit operates at a first clock frequency and the second processing unit operates at a second clock frequency, the second clock frequency being higher than the first clock frequency.

4. The networked computing system of claim 3 wherein the first processing unit assigns a task to the first processing unit or the second processing unit based on the processing speed required by the task such that the minimum power is used to process the task.

5. The networked computing system of claim 3 wherein the first processing unit instructs the second processing unit to enter a minimum power usage

mode.

6. The networked computing system of claim 5 wherein the first processing unit activates the second processing unit from the minimum power usage mode when a task is to be performed by the second processing unit.

7. The networked computing system of claim 4 wherein the first processing unit switches the coordinating protocol from the first processing unit to the second processing unit.

8. The networked computing system of claim 1 wherein the first and second processing units are communications devices.

9. The networked computing system of claim 7 wherein the first processing unit coordinates the operation of the second processing unit to minimize power consumption of the system.

10. The networked computing system of claim 8 wherein the first processing unit instructs the second processing unit to enter a minimum power usage mode.

11. The networked computing system of claim 8 wherein the first and second processing units are bi-directional communications devices.

12. The networked computing system of claim 12 wherein the first processing unit coordinates the operation of the second processing unit to minimize the power consumption of the system.

13. The networked computing system of claim 13 wherein the first processing unit instructs the second processing unit to enter a minimum power consumption mode for a preprogrammed time.

14. The networked computing system of claim 14 wherein the second processing unit polls the first processing unit after the preprogrammed time.

15. The networked computing system of claim 13 wherein the preprogrammed time is variable.

16. A multiple processor computer system comprising:

a plurality of processing units, each of the plurality of processing units operating at a clock frequency, with at least a first processing unit operating at a clock frequency lower than the remaining processing units; and

a coordinating protocol operable on the first processing unit, wherein the first processing unit coordinates the operation of the processing units such that the power efficiency of the computer system is optimized.

17. The multiple processor computer system of claim 16 wherein each of

the plurality of processing units operates at a different clock frequency.

18. The multiple processor computer system of claim 16 wherein the first processing unit transfers the coordinating function to a second processing unit of the plurality of processing units.

19. The multiple processor computer system of claim 18 wherein the second processing unit transfers the coordinating function to any of the plurality of processing units.

20. A wireless communication system comprising:

a base unit; and

a plurality of terminal units in communication with the base unit, each of the plurality of terminal units having a duty cycle,

wherein the base unit controls the duty cycle of the plurality of terminal units to optimize the power efficiency of the system.

21. The wireless communication system of claim 20 wherein the base unit instructs at least one of the terminal units to enter a minimum power consumption mode for a preprogrammed time.

22. The wireless communication system of claim 20 wherein the base unit and the terminal units are bi-directional.

23. The wireless communication system of claim 22 wherein the base unit instructs at least one of the terminal units to enter a minimum power consumption mode for a preprogrammed time.

24. The wireless communication system of claim 23 wherein at least one of the plurality of terminal unit polls the base unit after the preprogrammed time.

25. A method for optimizing the power efficiency of a multi-processor computing system comprising:

providing a plurality of processing units including at least a first and second processing unit, each of the plurality of processing units operating at a clock frequency; and

operating a coordinating protocol on the first processing unit, the first processing unit:

receiving a request to perform a task;

determining to which of the plurality of processing units to assign the task; and

assigning the task to one of the plurality of processing units.

26. The method of claim 25 wherein the first processing unit determines which processing unit to which a task is to be assigned based on optimizing the power efficiency.

27. The method of claim 25 further comprising the step of transferring the

coordinating protocol from the first processing unit to the second processing unit based on the speed required for the coordinating protocol.

28. The method of claim 27 further comprising the step of further transferring the coordinating protocol from the second processing unit to any of the plurality of processing units based on the speed required for the coordinating function.

29. A self-contained, miniaturized computer system comprising:

first and second processing units, the first processing unit including a coordinating protocol operable to coordinate the operation of the first and second processing units;

a power source;

a flash memory module; and

a RF transceiver,

wherein the first processing unit assigns tasks to the first and second processing units to optimize the power efficiency of the system.

30. The self-contained, miniaturized system of claim 29 wherein the first processing unit operates at a clock frequency of 32 kHz and the second processing unit operates at a clock frequency of 4 MHz.

31. The self-contained, miniaturized computer system of claim 30 wherein the power source is a battery.

32. The self-contained, miniaturized computer system of claim 30 wherein the first processing unit transfers the coordinating protocol from the first processing unit to the second processing unit.

33. The self-contained, miniaturized computer system of claim 32 wherein the second processing unit transfers the coordinating protocol from the second processing unit to the first processing unit.

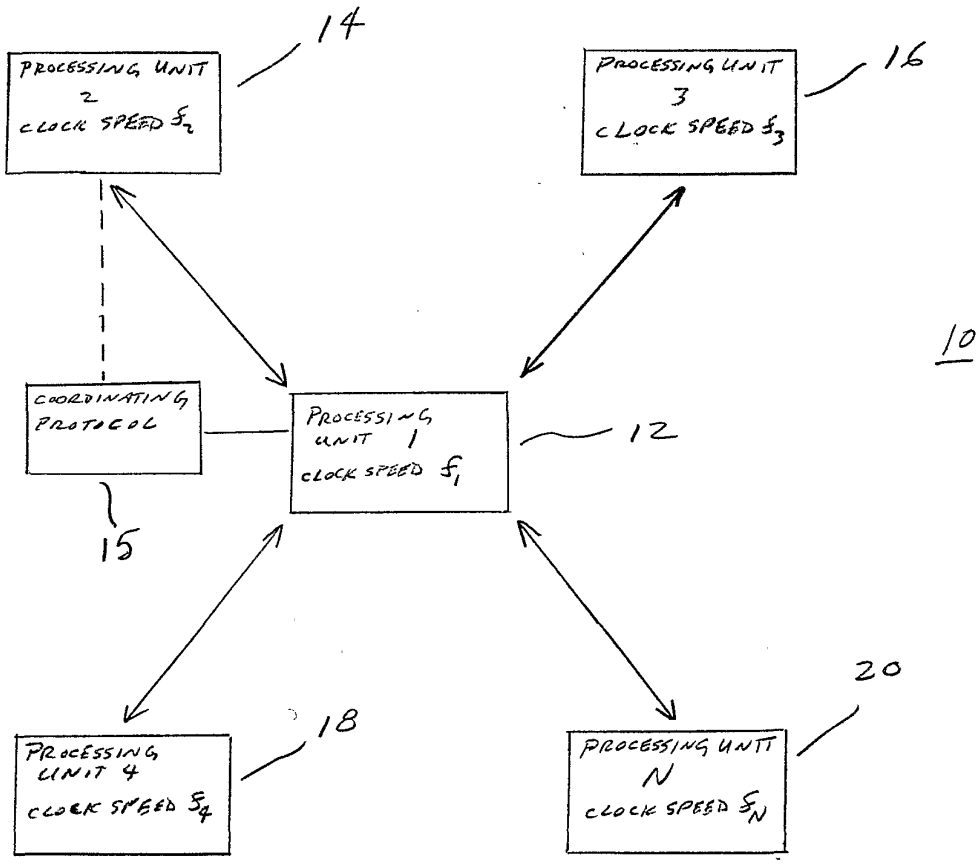

14
PROCESSING UNIT 2
CLOCK SPEED f_2
16
PROCESSING UNIT 3
CLOCK SPEED f_3
10
COORDINATING PROTOCOL
15
PROCESSING UNIT 1
CLOCK SPEED f_1
12
18
PROCESSING UNIT 4
CLOCK SPEED f_4
20
PROCESSING UNIT N
CLOCK SPEED f_N

FIG. 1

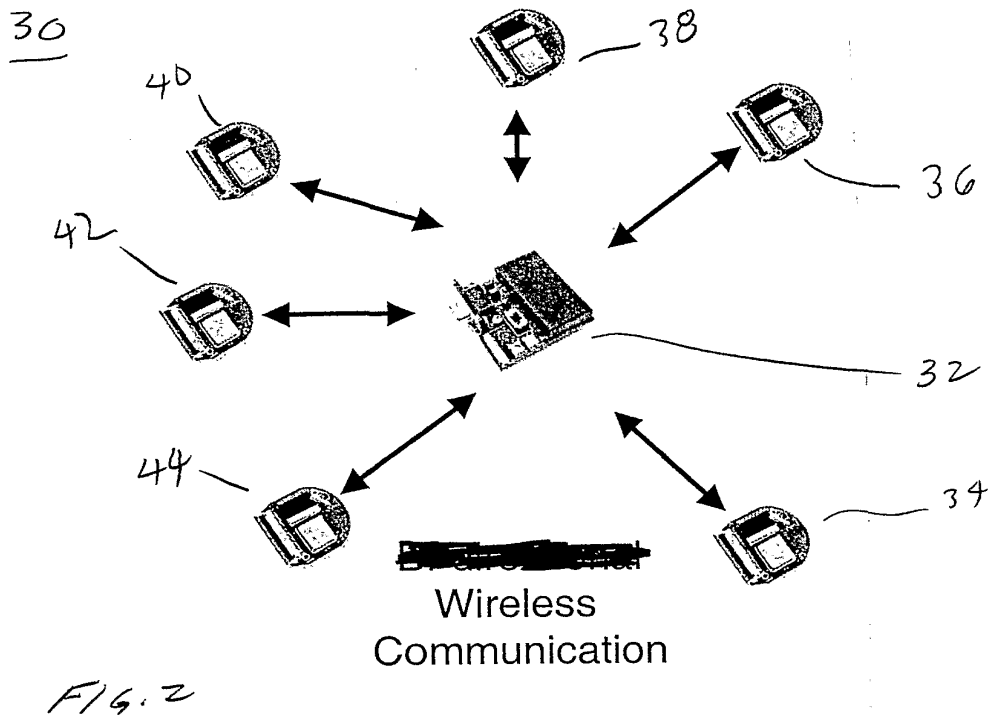
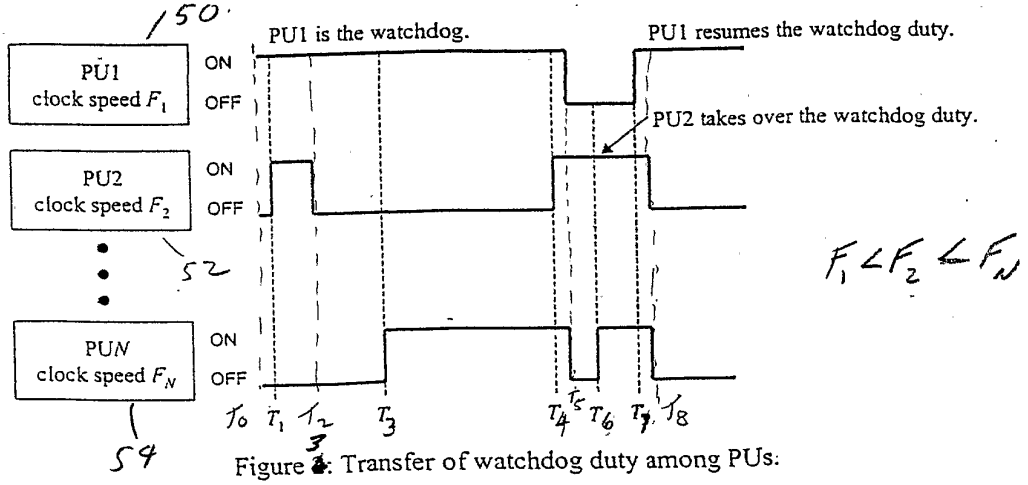


FIG. 2



$F_1 < F_2 < F_N$

Figure 3: Transfer of watchdog duty among PUs.

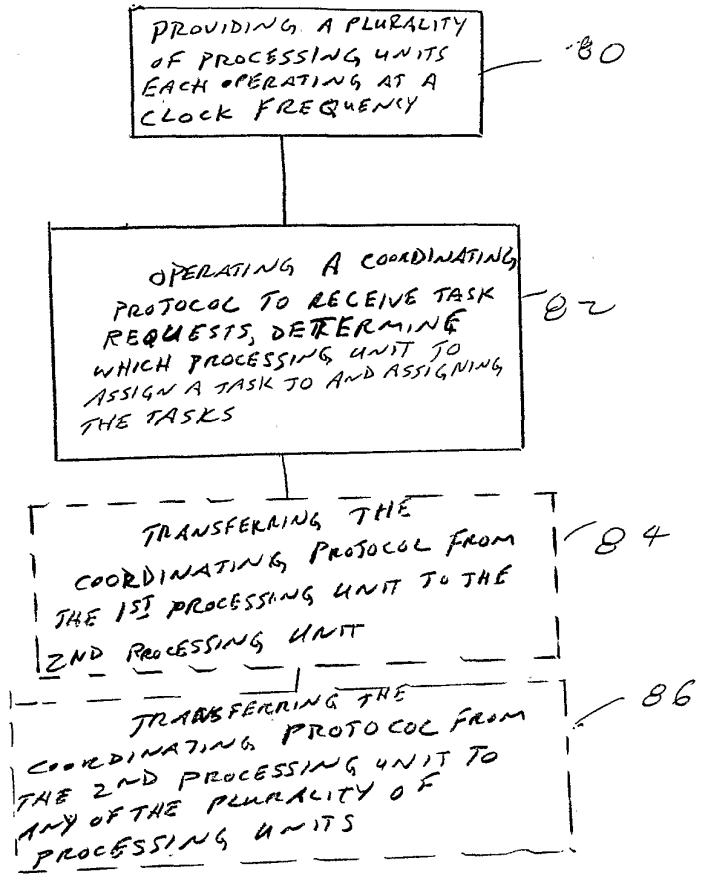

PROVIDING A PLURALITY OF PROCESSING UNITS EACH OPERATING AT A CLOCK FREQUENCY
80
OPERATING A COORDINATING PROTOCOL TO RECEIVE TASK REQUESTS, DETERMINE WHICH PROCESSING UNIT TO ASSIGN A TASK TO AND ASSIGNING THE TASKS
82
TRANSFERRING THE COORDINATING PROTOCOL FROM THE 1ST PROCESSING UNIT TO THE 2ND PROCESSING UNIT
84
TRANSFERRING THE COORDINATING PROTOCOL FROM THE 2ND PROCESSING UNIT TO ANY OF THE PLURALITY OF PROCESSING UNITS
86

FIG. 4

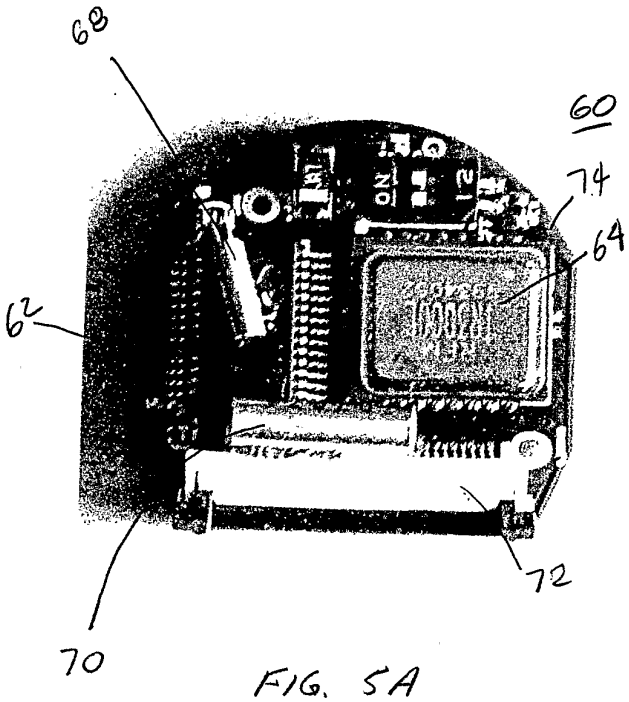


FIG. 5A

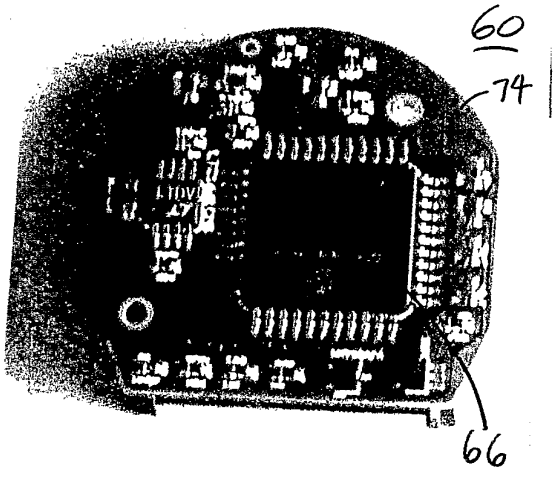


FIG. 5B

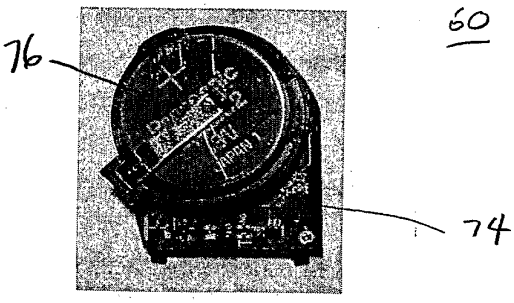


FIG. 5C

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US01/50648

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) : G06F 1/26, 1/32
US CL : 713/300, 320, 322, 323, 324
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 713/300, 320, 322, 323, 324

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EAST

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,790,817 A (ASGHAR et al.) 4 August 1998 (04.08.1998), see the entire document especially column 5, line 56 through column 6, line 17.	1-33
Y,P	US 6,272,537 B1 (KEKIC et al.) 7 August 2001 (07.08.2001), column 82 line 51 through column 83 line 52	13, 14, 15, 23, and 24
Y	US 4,358,823 A (MCDONALD et al.) 9 November 1982 (09.09.1982), the entire document.	1-33
Y	US 5,194,860 A (JONES et al) 16 March 1993 (16.03.1993), column 3 line 59 through column 4 line 35.	5, 10 and 21
Y	US 5,257,372 A (FURTNEY et al) 26 October 1993 (26.10.1993), the entire document, especially column 4 line 50 through column 5 line 37.	6

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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Date of the actual completion of the international search
20 March 2002 (20.03.2002)

Date of mailing of the international search report
18 APR 2002

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Authorized officer
Thomas Lee
Telephone No. (703) 305-3900

Form PCT/ISA/210 (second sheet) (July 1998)

Electronic Patent Application Fee Transmittal

Application Number:	10966161
Filing Date:	15-Oct-2004
Title of Invention:	REDUCING PROBE TRAFFIC IN MULTIPROCESSOR SYSTEMS
First Named Inventor/Applicant Name:	Eric Morton
Filer:	Joseph Michael Villeneuve/Mia Mitchell-Haynes
Attorney Docket Number:	NWISP052
Filed as Large Entity	

Utility Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Request for continued examination	1801	1	790	790
		Total in USD ($)		**790**

Electronic Acknowledgement Receipt	
EFS ID:	1884751
Application Number:	10966161
International Application Number:	
Confirmation Number:	6289
Title of Invention:	REDUCING PROBE TRAFFIC IN MULTIPROCESSOR SYSTEMS
First Named Inventor/Applicant Name:	Eric Morton
Customer Number:	22434
Filer:	Joseph Michael Villeneuve/Mia Mitchell-Haynes
Filer Authorized By:	Joseph Michael Villeneuve
Attorney Docket Number:	NWISP052
Receipt Date:	18-JUN-2007
Filing Date:	15-OCT-2004
Time Stamp:	21:07:55
Application Type:	Utility

Payment information:

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Payment was successfully received in RAM	$790
RAM confirmation Number	3374
Deposit Account	500388
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 and 1.17	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part /.zip	Pages (if appl.)
1	Request for Continued Examination (RCE)	NWISP052_RCE_sb0030e_fill.pdf	666989	no	3
Warnings:					
Information:					
2	Information Disclosure Statement (IDS) Filed	NWISP052_USPTO_IDS_FORM.pdf	1192777	no	10
Warnings:					
Information:					
3	Information Disclosure Statement (IDS) Filed	NWISP052_USPTO_IDS_FORM-2.pdf	768782	no	5
Warnings:					
Information:					
4	Foreign Reference	02039242.pdf	909473	no	25
Warnings:					
Information:					
5	NPL Documents	10288347_NOA.pdf	333806	no	7
Warnings:					
Information:					
6	NPL Documents	OA_mailed_11_18_04_NWISP024.pdf	1746295	no	53
Warnings:					
Information:					
7	NPL Documents	NPL_3_KIM.pdf	375101	no	4
Warnings:					
Information:					
8	NPL Documents	NPL_4_POWELL.pdf	1022832	no	12
Warnings:					
Information:					
9	NPL Documents	NPL_5_CULLER.pdf	589683	no	11
Warnings:					

Information:					
10	NPL Documents	NPL_6_TANENBAUM.pdf	3778291	no	60
Warnings:					
Information:					
11	NPL Documents	OA_mailed_5_12_05_NWISP024.pdf	1654122	no	51
Warnings:					
Information:					
12	NPL Documents	OA_mailed_9_22_04_NWISP002.pdf	819333	no	21
Warnings:					
Information:					
13	NPL Documents	OA_mailed_3_7_05_NWISP002.pdf	754691	no	20
Warnings:					
Information:					
14	NPL Documents	OA_mailed_7_21_05_NWISP002.pdf	726587	no	19
Warnings:					
Information:					
15	NPL Documents	OA_mailed_9_23_04_NWISP003.pdf	731916	no	19
Warnings:					
Information:					
16	NPL Documents	OA_mailed_3_10_05_NWISP003.pdf	723803	no	19
Warnings:					
Information:					
17	NPL Documents	OA_mailed_7_21_05_NWISP003.pdf	648137	no	17
Warnings:					
Information:					
18	NPL Documents	OA_mailed_9_22_04_NWISP004.pdf	649879	no	17
Warnings:					

Information:					
19	NPL Documents	OA_mailed_3_10_05_NWISP004.pdf	629146	no	17
Warnings:					
Information:					
20	NPL Documents	OA_mailed_7_21_05_NWISP004.pdf	638040	no	17
Warnings:					
Information:					
21	NPL Documents	OA_mailed_7_20_05_NWISP030.pdf	501652	no	15
Warnings:					
Information:					
22	NPL Documents	OA_mailed_9_9_05_NWISP040.pdf	258936	no	8
Warnings:					
Information:					
23	NPL Documents	OA_mailed_9_9_05_NWISP033.pdf	225227	no	7
Warnings:					
Information:					
24	NPL Documents	OA_mailed_11_2_05_NWISP003.pdf	794697	no	20
Warnings:					
Information:					
25	NPL Documents	OA_mailed_10_5_05_NWISP036.pdf	625694	no	17
Warnings:					
Information:					
26	Fee Worksheet (PTO-06)	fee-info.pdf	8191	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	21774080		

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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EXAMINER	
PEUGH, BRIAN R	
ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 04/12/2007

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/966,161	10/15/2004	Eric Morton	NWISP052	6289

TITLE OF INVENTION: REDUCING PROBE TRAFFIC IN MULTIPROCESSOR SYSTEMS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$0	$1700	07/12/2007

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 07/06) Approved for use through 04/30/2007.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

22434 7590 04/12/2007

BEYER WEAVER LLP
P.O. BOX 70250
OAKLAND, CA 94612-0250

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/966,161	10/15/2004	Eric Morton	NWISP052	6289

TITLE OF INVENTION: REDUCING PROBE TRAFFIC IN MULTIPROCESSOR SYSTEMS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$0	$1700	07/12/2007

EXAMINER	ART UNIT	CLASS-SUBCLASS
PEUGH, BRIAN R	2187	711-148000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/966,161	10/15/2004	Eric Morton	NWISP052	6289

22434 7590 04/12/2007

BEYER WEAVER LLP
P.O. BOX 70250
OAKLAND, CA 94612-0250

EXAMINER	
PEUGH, BRIAN R	
ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 04/12/2007

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 250 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 250 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 07/06) Approved for use through 04/30/2007.

Notice of Allowability	Application No.	Applicant(s)	
	10/966,161	MORTON ET AL.	
	Examiner	Art Unit	
	Brian R. Peugh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the filing of 10/15/04*.

2. ☒ The allowed claim(s) is/are *1-7 & 9-26, now renumbered as 1-25*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 4/4/05
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on April 4, 2005 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

Specification page 1, line 10: Insert --, now U.S. Patent No. 7,003,633,-- before "for".

Specification page 1, line 14: Insert --, now U.S. Patent No. 7,103,726,-- before "for".

The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

Misnumbered claims 9-26 been renumbered as 8-25 as seen below:

Claim 9, line 1: Replace "9" with –8--.

Claim 10, line 1: Replace "10" with –9--.

Claim 10, line 1: Replace " claim 9" with –claim 8--.

Claim 11, line 1: Replace "11" with –10--.

Claim 11, line 1: Replace "claim 10" with –claim 9--.

Claim 12, line 1: Replace "12" with –11--.

Claim 13, line 1: Replace "13" with –12--.

Claim 13, line 1: Replace "claim 12" with –claim 11--.

Claim 14, line 1: Replace "14" with –13--.

Claim 14, line 1: Replace "claim 12" with –claim 11--.

Claim 15, line 1: Replace "15" with –14--.

Claim 16, line 1: Replace "16" with –15--.

Claim 17, line 1: Replace "17" with –16--.

Claim 18, line 1: Replace "18" with –17--.

Claim 18, line 1: Replace "claim 17" with –claim 16--.

Claim 19, line 1: Replace "19" with –18--.

Claim 19, line 1: Replace "claim 18" with –claim 17--.

Claim 20, line 1: Replace "20" with –19--.

Claim 20, line 2: Replace "claim 17" with –claim 16--.

Claim 21, line 1: Replace "21" with –20--.

Claim 21, line 1: Replace "claim 20" with –claim 19--.

Claim 22, line 1: Replace "22" with –21--.

Claim 22, line 1: Replace "claim 21" with –claim 20--.

Claim 23, line 1: Replace "23" with –22--.

Claim 23, line 1: Replace "claim 20" with –claim 19--.

Claim 24, line 1: Replace "24" with –23--.

Claim 24, line 1: Replace "claim 23" with –claim 22--.

Claim 25, line 1: Replace "25" with –24--.

Claim 25, line 2: Replace "claim 17" with –claim 16--.

Claim 26, line 1: Replace "26" with –25--.**REASONS FOR ALLOWANCE**

The following is an examiner's statement of reasons for allowance: The prior art, including that of Mudgett et al., Razdan et al., Keller et al., and Guo et al. teach related probing systems but fail to teach the combination including the limitation of:

(Claim 1) "...a probe filtering unit which is operable to receive probes corresponding to memory lines from the processing nodes and to transmit the probes only to selected ones of the processing nodes with reference to probe filtering information representative of states associated with selected ones of the cache memories";

(Filed Claim 17, new claim 16) "...the probe filtering unit being operable to receive probes corresponding to memory lines from the processing nodes and to transmit the probes only to selected ones of the processing nodes with reference to probe filtering information representative of states associated with selected ones of the cache memories";

(Filed Claim 26, new claim 25) "...evaluating the probe with the probe filtering unit to determine whether a valid copy of the memory line is in any of the cache

memories, the evaluating being done with reference to probe filtering information associated with the probe filtering unit and representative of states associated with selected ones of the cache memories; transmitting the probe from the probe filtering unit only to selected ones of the processing nodes identified by the evaluating; accumulating probe responses from the selected processing nodes with the probe filtering unit; and responding to the probe from the first processing node only with the probe filtering unit".

The dependent claims are allowable as being dependent upon, and thus incorporating therein, the allowable subject matter of the respective parent claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian R. Peugh whose telephone number is (571) 272-4199. The examiner can normally be reached on Monday-Thursday from 7:00am to 4:30pm. The examiner can also be reached on alternate Friday's from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks, can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian R. Peugh
Primary Examiner
Art Unit 2187
March 28, 2007

Form 1449 (Modified)	Atty Docket No.	Application No.:
	NWISP052	10/966,161
Information Disclosure Statement By Applicant	Applicant: Morton et al.	
	Filing Date	Group
(Use Several Sheets if Necessary)	10/15/04	2187

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
/BP/	A1	6,167,492	12/26/00	Keller et al.			12/23/98
	A2	6,385,705 B1	5/7/02	Keller et al.			10/30/00
	A3	6,490,661	12/3/02	Keller et al.			12/21/98
	A4	2001/0013089	08/09/01	Weber, Wolf-Dietrich			3/12/98
	A5	6,640,287	10/28/03	Gharachorloo, et al.			1/7/02
	A6	6,658,526	12/02/03	Nguyen, et al.			10/20/99
	A7	6,085,295	07/04/00	Ekanadham et al.			10/20/97
	A8	20020046327	04/18/02	Gharachorloo et al.			06/11/01
	A9	6,108,737	08/22/00	Sharma et al.			10/24/97

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation Yes	Translation No

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
/BP/	B1	*HyperTransport ™ I/O Link Specification Revision 1.03,* HyperTransport ™ Consortium, October 10, 2001, Copyright © 2001 HyperTransport Technology Consortium
/BP/	B2	PCT Search Report PCT/US03/34756, Int'l filing date 10/30/03, Search report Mailed December 16, 2004.
/BP/	B3	Bilir et al., "Multicast Snooping: A New Coherence Method Using a Multicast Address Network", Computer Architecture, 1999. Proceedings of the 26th International Symposium on, May 2-4, 1999.

Examiner	/Brian Peugh/	Date Considered	03/28/2007

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Pg. 1 of 2

Form 1449 (Modified)	Atty Docket No.	Application No.:
	NWISP052	10/966,161
Information Disclosure Statement By Applicant	Applicant: Morton et al.	
	Filing Date	Group
(Use Several Sheets if Necessary)	10/15/04	2187

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
/BP/	A10	6,799,252 B1	9/28/04	Bauman			
	A11	6,636,906 B1	10/21/03	Sharma et al.			
	A12	5,524,212	6/4/96	Somani et al.			
	A13	5,751,995	5/12/98	Sarangdar			
	A14	5,893,151	4/6/99	Merchant			
	A15	US 2002/0087807 A1	7/4/02	Gharachorloo et al.			
	A16	US 20040088492 A1	5/6/04	Glasco			
	A17	US 20040088493 A1	5/6/04	Glasco			
	A18	US 20040117559 A1	6/17/04	Glasco			

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation Yes	Translation No

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
/BP/	B4	Martin et al., "Bandwidth Adaptive Snooping", Proceedings of the Eighth International Symposium on High-Performance Computer Architecture on February 2-6, 2002; pp. 251-262.
/BP/	B5	Sorin et al., "Specifying and Verifying a Broadcast and a Multicast Snooping Cache Coherence Protocol", IEEE Transactions on Parallel and Distributed Systems, Vol. 13, No. 6, June 2002.

Examiner	/Brian Peugh/	Date Considered	03/28/2007

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

DECLARATION FOR ORIGINAL U.S. PATENT APPLICATION

Attorney's Docket No. NWISP052

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: REDUCING PROBE TRAFFIC IN MULTIPROCESSOR SYSTEMS, the specification of which,

(check one)

1. ☐ is attached hereto.

2. ☒ was filed on October 15, 2004 as
U.S. Application No. 10/966,161
and was amended on _____.

3. ☐ was filed on _____ as
International PCT Application Serial No. _____
and was amended on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, CFR §1.56.

Prior Foreign Application(s)

I hereby claim foreign priority benefits under Title 35, United States code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

			Priority Benefits Claimed?
_____ (Appl. No.)	_____ (Country)	_____ (Date Filed- Day/Month/Year)	__Yes __No
_____ (Appl. No.)	_____ (Country)	_____ (Date Filed- Day/Month/Year)	__Yes __No

Provisional Application(s)

I hereby claim the benefit under 35 U.S.C. §119(e) of any United States provisional application(s) listed below:

_____ (Application No.)	_____ (Filing Date)
_____ (Application No.)	_____ (Filing Date)

Prior U.S. Application(s)

I hereby claim the benefit under Title 35, United Sates Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this applications is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

10/288,347 (Application No.)	11/4/2002 (Filing Date)	Pending (Status - patented, pending, abandoned)
_____ (Application No.)	_____ (Filing Date)	_____ (Status - patented, pending, abandoned)

Send Correspondence To: **Customer Number: 022434**

022434

Direct Telephone Calls To: **Joseph M. Villeneuve at telephone number (510) 843-6200**

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Typewritten Full Name of Sole or First Inventor: **Eric Morton** Citizenship: **United States**

Inventor's signature: [signature] **Date of Signature:** 1/13/05

Residence: (City) **Austin** (State/Country) **Texas/U.S.**

Post Office Address: **12901 Majestic Oaks Drive, Austin, TX 78732**

Typewritten Full Name of Sole or Second Inventor: **Rajesh Kota** Citizenship: **India**

Inventor's signature: [signature] **Date of Signature:** 1/13/05

Residence: (City) **Austin** (State/Country) **Texas/U.S.**

Post Office Address: **5817 Miramonte Drive, Austin, TX 78759**

Typewritten Full Name of Sole or Third Inventor: **Adnan Khaleel** Citizenship: **India**

Inventor's signature: [signature] **Date of Signature:** 1/13/05

Residence: (City) **Austin** (State/Country) **Texas/U.S.**

Post Office Address: **10430 Morado Circle, Apt. #2111, Austin, TX**

Typewritten Full Name of Sole or Fourth Inventor: **David B. Glasco** Citizenship: **United States**

Inventor's signature: **Date of Signature:**

Residence: (City) **Austin** (State/Country) **Texas/U.S.**

Post Office Address: **10337 Ember Glen Drive, Austin, TX 78726**

Notice of References Cited	Application/Control No. 10/966,161	Applicant(s)/Patent Under Reexamination MORTON ET AL.	
	Examiner Brian R. Peugh	Art Unit 2187	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2001/0029574	10-2001	RAZDAN et al.	711/130
*	B	US-2004/0024836	02-2004	Keller et al.	709/213
*	C	US-6,775,749	08-2004	Mudgett et al.	711/146
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Guo, et al., "A Probe-Based Server Selection Protocol for Differentiated Service Networks", © 2002 IEEE, p. 2353-2357.
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/966,161	MORTON ET AL.	
	Examiner	Art Unit	
	Brian R. Peugh	2187	

SEARCHED			
Class	Subclass	Date	Examiner
711	141,148, 131,144, 145,146	3/21/2007	BRP
709	206,213	3/21/2007	BRP
709	216,217	3/21/2007	BRP
709	218,219	3/21/2007	BRP

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner
711	**148,141**	3/28/2007	**BRP**

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
WEST search (text)	3/21/2007	BRP
Updated WEST search (text)	3/22/2007	BRP
Consulted Kevin Ellis	3/27/2007	BRP
Updated WEST search (text) IEEE search	3/28/2007	BRP

Issue Classification	Application/Control No. 10/966,161	Applicant(s)/Patent under Reexamination MORTON ET AL.
	Examiner Brian R. Peugh	Art Unit 2187

ISSUE CLASSIFICATION

ORIGINAL		INTERNATIONAL CLASSIFICATION									
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED				
711	148	G	06	F	12	/00					/
CROSS REFERENCES						/					/
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)										
711	141					/					/
						/					/
						/					/
						/					/
						/					/

(Assistant Examiner) (Date)

(Legal Instruments Examiner) 4/11/07 (Date)

Brian R. Peugh 3/30/07
Primary Examiner
(Primary Examiner) (Date)

Total Claims Allowed: 25

O.G. Print Claim(s)	O.G. Print Fig.
1	20

☐ **Claims renumbered in the same order as presented by applicant** ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1		31		61		91		121		151		181
2	2		32		62		92		122		152		182
3	3		33		63		93		123		153		183
4	4		34		64		94		124		154		184
5	5		35		65		95		125		155		185
6	6		36		66		96		126		156		186
7	7		37		67		97		127		157		187
	8		38		68		98		128		158		188
8	9		39		69		99		129		159		189
9	10		40		70		100		130		160		190
10	11		41		71		101		131		161		191
11	12		42		72		102		132		162		192
12	13		43		73		103		133		163		193
13	14		44		74		104		134		164		194
14	15		45		75		105		135		165		195
15	16		46		76		106		136		166		196
16	17		47		77		107		137		167		197
17	18		48		78		108		138		168		198
18	19		49		79		109		139		169		199
19	20		50		80		110		140		170		200
20	21		51		81		111		141		171		201
21	22		52		82		112		142		172		202
22	23		53		83		113		143		173		203
23	24		54		84		114		144		174		204
24	25		55		85		115		145		175		205
25	26		56		86		116		146		176		206
	27		57		87		117		147		177		207
	28		58		88		118		148		178		208
	29		59		89		119		149		179		209
	30		60		90		120		150		180		210

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Bib Data Sheet

CONFIRMATION NO. 6289

SERIAL NUMBER	FILING OR 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/966,161	10/15/2004 RULE 1.47	711	2187	NWISP052

APPLICANTS

Eric Morton, Austin, TX;
Rajesh Kota, Austin, TX;
Adnan Khaleel, Austin, TX;
David B. Glasco, Austin, TX;

3/28/07

3/28/07

**** CONTINUING DATA *************************

This application is a CIP of 10/288,347 11/04/2002 PAT 7,003,633

**** FOREIGN APPLICATIONS ********************

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 11/23/2004

Foreign Priority claimed	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
☐ yes ☐ no 35 USC 119 (a-d) conditions met ☐ yes ☐ no ☐ Met after Allowance Verified and Acknowledged Examiner's Signature Initials	TX	25	25	3

ADDRESS
22434

TITLE

Reducing probe traffic in multiprocessor systems

FILING FEE RECEIVED	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit
1170		

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Wed, 28 Mar 2007, 9:49:06 AM EST

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Recent Search Queries

#1 (((probe) <sentence> (filter <or> filtering))<in>metadata)

#2 (((probe) <near/2> (filter <or> filtering))<in>metadata)

#3 (((probe) <near/2> (route <or> routing))<in>metadata)

#4 (((probe) <sentence> (route <or> routing) <sentence> cache) <in>metadata)

#5 (((probe) <sentence> (cache <or> caching) <sentence> cache) <in>metadata)

[redacted]

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Term: 7003633.pn. or 7103726.pn.

Display: 10 **Documents in Display Format:** TI **Starting with Number** 1

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Search Clear Interrupt

Search History

DATE: Wednesday, March 28, 2007 Purge Queries Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L1	7003633.pn. or 7103726.pn.	2	L1

END OF SEARCH HISTORY

Freeform Search

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Term: l27 and ((prob$3 or filter$3) with (state or coherenc$4))

Display: 10 **Documents in Display Format:** - **Starting with Number** 1

Generate: ○ **Hit List** ◉ **Hit Count** ○ **Side by Side** ○ **Image**

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DATE: Thursday, March 22, 2007 **Purge Queries** Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT; PLUR=YES; OP=OR			
L29	l27 and ((prob$3 or filter$3) with (state or coherenc$4))	35	L29
L28	l10 and (probe near2 (rout$3 or filter$3))	44	L28
L27	l10 and (probe near4 (rout$3 or filter$3))	49	L27
L26	L12 and mask$3	0	L26
L25	L12 and asic	1	L25
L24	L12 and (hdl or language)	0	L24
L23	L12 and code	0	L23
L22	L12 and netlist	0	L22
L21	l12 and (simulat$4)	0	L21
L20	l12 and (simulatable)	0	L20
L19	l12 and (strsimulatable)	0	L19
L18	l12 and (structure$1)	0	L18
L17	l12 and (medium)	0	L17
L16	l12 and (integrated)	1	L16
L15	l12 and (data near2 structures)	0	L15
L14	l10 and (probe with filter$3 with (unit or controller or node))	22	L14

L13	L12 and (state$1 with cache)	1	L13
L12	7003633.pn.	1	L12
L11	L10 and (prob$3 with (filter$3))	181	L11
L10	L9 or l8	16943	L10
L9	709/206,213,216,217,218,219.ccls.	14752	L9
L8	711/131,146,144,145.ccls.	2261	L8
L7	L6 and (prob$3 with (filter$3))	21	L7
L6	l1 or l2 or l4 or L5	93	L6
L5	(glasco with david).in.	72	L5
L4	(khaleel with adnan).in.	2	L4
L3	(rajkhaleel with adnan).in.	0	L3
L2	(rajesh with kota).in.	36	L2
L1	(eric with morton).in.	15	L1

END OF SEARCH HISTORY

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APPLICATION NUMBER	FILING OR 371(c) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
10/966,161	10/15/2004	Eric Morton	NWISP052

CONFIRMATION NO. 6289

22434
BEYER WEAVER LLP
P.O. BOX 70250
OAKLAND, CA94612-0250

Title: Reducing probe traffic in multiprocessor systems

Publication No. US-2007-0055826-A1
Publication Date: 03/08/2007

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	DRAWINGS	TOT CLAIMS	IND CLAIMS
10/966,161	10/15/2004	2187	1170	NWISP052	25	25	3

CONFIRMATION NO. 6289

022434
BEYER WEAVER & THOMAS, LLP
P.O. BOX 70250
OAKLAND, CA94612-0250

UPDATED FILING RECEIPT

Date Mailed: 11/29/2006

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please mail to the Commissioner for Patents P.O. Box 1450 Alexandria Va 22313-1450. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).**

Applicant(s)

Eric Morton, Austin, TX;
Rajesh Kota, Austin, TX;
Adnan Khaleel, Austin, TX;
David B. Glasco, Austin, TX;

Assignment For Published Patent Application

Newisys, Inc., A Delaware corporation

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CIP of 10/288,347 11/04/2002 PAT 7,003,633

Foreign Applications

If Required, Foreign Filing License Granted: 11/23/2004

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US10/966,161**

Projected Publication Date: 03/08/2007

Non-Publication Request: No

Early Publication Request: No

Title

Reducing probe traffic in multiprocessor systems

Preliminary Class

711

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Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

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For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

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Adnan Khaleel, Austin, TX;
David B. Glasco, Austin, TX;

Assignment For Published Patent Application

Newisys, Inc., A Delaware corporation

Power of Attorney: The patent practitioners associated with Customer Number 022434

Domestic Priority data as claimed by applicant

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Early Publication Request: No

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Paper No. None

BEYER WEAVER & THOMAS LLP
P.O. BOX 70250
OAKLAND CA 94612-0250

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MAY 23 2005

OFFICE OF PETITIONS

In re Application of :
Eric Morton, Rajesh Kota, Adnan Khaleel, and David B,. Glasco :
Application No. 10/966,161 :
Filed: October 15, 2004 :
Attorney Docket No. NWISP052 :
Title: REDUCING PROBE TRAFFIC IN MULTIPROCESSOR SYSTEMS :

DECISION ON PETITION
UNDER 37 C.F.R. §1.47(a)

This is in response to the petition under 37 C.F.R. §1.47(a)[1], filed February 11, 2005.

On October 15, 2004, the application was deposited, identifying Eric Morton, Rajesh Kota, Adnan Khaleel, and David B,. Glasco as joint inventors. No oath or declaration was included on filing. On November 24, 2004, a "Notice to File Missing Parts of Nonprovisional Application – Filing Date Granted" (Notice) was mailed, indicating that a fully executed oath or declaration and the associated surcharge were required, along with a the basic filing fee and additional claim fees. This Notice set a two-month period for reply.

With the instant petition, Petitioner has also submitted the petition fee, the associated surcharge, the basic filing fee and additional claim fees, a declaration which has been executed by each of

1A grantable petition under 37 C.F.R. §1.47(a) requires:
(1) the petition fee of $130;
(2) a surcharge of either $65 or $130 if the petition is not filed at the time of filing the application, as set forth in 37 CFR § 1.16(e);
(3) a statement of the last known address of the non-signing inventors;
(4) either
a) proof that a copy of the entire application (specification, claims, drawings, and the oath or declaration) was sent or given to the non-signing inventor for review and proof that the non-signing inventor refuses to join in the application or
b) proof that the non-signing inventor cannot be found or reached after diligent effort;
(5) a declaration which complies with 37 CFR §1.63.

the inventors save Mr. Glasco, copies of various e-mails, and a statement of facts. Petitioner has further included a one-month extension of time to make timely this response.

Petitioner has failed to supply the last known address of the non-signing inventor. The Office will presume that the last known address is that which has been listed on the declaration, and Petitioner must notify the Office if this assumption is not correct.

Petitioner has met each of the 5 requirements above.

The petition is **GRANTED** and this application is hereby accorded Rule §1.47(a) status.

As provided in Rule 1.47(a), this Office will forward notice of this application's filing to the non-signing inventor at the address given in the petition. Notice of the filing of this application will also be published in the Official Gazette.

After this decision is mailed, the application will be forwarded to Technology Center 2100 for further processing.

The general phone number for the Office of Petitions which should be used for status requests is (571) 272-3282. Telephone inquiries regarding *this decision* should be directed to the undersigned at (571) 272-3225.

Paul Shanoski
Senior Attorney
Office of Petitions
United States Patent and Trademark Office

UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
P.O. BOX 1450
ALEXANDRIA, VA 22313-1450
WWW.USPTO.GOV

David B,. Glasco
10337 Ember Glen Drive
Austin, TX 78726

In re Application of :
Eric Morton, Rajesh Kota, Adnan Khaleel, and David B,. Glasco :
Application No. 10/966,161 :
Filed: October 15, 2004 :
Attorney Docket No. NWISP052 :
Title: REDUCING PROBE TRAFFIC IN MULTIPROCESSOR SYSTEMS :

COPY MAILED

MAY 23 2005

LETTER OFFICE OF PETITIONS

Dear Mr. Glasco

You are named as a joint inventor in the above-identified United States patent application filed under the provisions of 35 U.S.C. 116 (United States Code) and 37 CFR 1.47(a), Rules of Practice in Patent Cases. Should a patent be granted on the application you will be designated therein as a joint inventor.

As a named inventor you are entitled to inspect any paper in the file wrapper of the application, order copies of all or any part thereof (at a prepaid cost per 37 CFR 1.19) or make your position of record in the application. Alternatively, you may arrange to do any of the preceding through a registered patent attorney or agent presenting written authorization from you. If you care to join the application, the attorney of record below would presumably assist you. Joining in the application would entail the filing of an appropriate oath or declaration by you pursuant to 37 CFR 1.63.

Telephone inquiries regarding this communication should be directed to the undersigned at (571) 272-3225. Requests for information regarding your application should be directed to the File Information Unit at (703) 308-2733. Information regarding how to pay for and order a copy of the application, or a specific paper in the application, should be directed to the Certification Division at (703) 308-9726 or 1-800-972-6382 (outside the Washington D.C. area).

Paul Shanoski
Senior Attorney
Office of Petitions
United States Patent and Trademark Office

cc: BEYER WEAVER & THOMAS LLP
P.O. BOX 70250
OAKLAND CA 94612-0250

IPW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Morton et al.

Attorney Docket No.: NWISP052

Application No.: 10/966,161

Examiner: Not yet assigned

Filed: October 15, 2004

Group: 2187

Title: REDUCING PROBE TRAFFIC IN MULTIPROCESSOR SYSTEMS

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first-class mail on March 31, 2005 in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Signed: _____
Mia Mitchell-Haynes

INFORMATION DISCLOSURE STATEMENT
37 CFR §§1.56 AND 1.97(b)

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

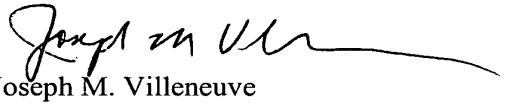
The references listed in the attached PTO Form 1449, copies of which are attached, may be material to examination of the above-identified patent application. Applicants submit these references in compliance with their duty of disclosure pursuant to 37 CFR §§1.56 and 1.97. The Examiner is requested to make these references of official record in this application.

This Information Disclosure Statement is not to be construed as a representation that a search has been made, that additional information material to the examination of this application does not exist, or that these references indeed constitute prior art.

This Information Disclosure Statement is: (i) filed within three (3) months of the filing date of the above-referenced application, (ii) believed to be filed before the mailing date of a first Office Action on the merits, or (iii) believed to be filed before the mailing of a first Office Action after the filing of a Request for Continued Examination under §1.114. Accordingly, it is believed that no fees are due in connection with the filing of this Information Disclosure

Statement. However, if it is determined that any fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 500388 (Order No. NWISP052).

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP



Joseph M. Villeneuve
Registration No. 37,460

P.O. Box 70250
Oakland, CA 94612-0250
(510) 663-1100

Form 1449 (Modified)	Atty Docket No.	Application No.:
	NWISP052	10/966,161
Information Disclosure Statement By Applicant	Applicant: Morton et al.	
	Filing Date	Group
(Use Several Sheets if Necessary)	10/15/04	2187

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A1	6,167,492	12/26/00	Keller et al.			12/23/98
	A2	6,385,705 B1	5/7/02	Keller et al.			10/30/00
	A3	6,490,661	12/3/02	Keller et al.			12/21/98
	A4	2001/0013089	08/09/01	Weber, Wolf-Dietrich			3/12/98
	A5	6,640,287	10/28/03	Gharachorloo, et al.			1/7/02
	A6	6,658,526	12/02/03	Nguyen, et al.			10/20/99
	A7	6,085,295	07/04/00	Ekanadham et al.			10/20/97
	A8	20020046327	04/18/02	Gharachorloo et al.			06/11/01
	A9	6,108,737	08/22/00	Sharma et al.			10/24/97

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation Yes	Translation No

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	B1	*HyperTransport ™ I/O Link Specification Revision 1.03*, HyperTransport ™ Consortium, October 10, 2001, Copyright © 2001 HyperTransport Technology Consortium
	B2	PCT Search Report PCT/US03/34756, Int'l filing date 10/30/03, Search report Mailed December 16, 2004.
	B3	Bilir et al., "Multicast Snooping: A New Coherence Method Using a Multicast Address Network", Computer Architecture, 1999. Proceedings of the 26th International Symposium on, May 2-4, 1999.

Examiner	Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form 1449 (Modified)	Atty Docket No.	Application No.:
	NWISP052	10/966,161
Information Disclosure Statement By Applicant	Applicant: Morton et al.	
	Filing Date	Group
(Use Several Sheets if Necessary)	10/15/04	2187

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A10	6,799,252 B1	9/28/04	Bauman			
	A11	6,636,906 B1	10/21/03	Sharma et al.			
	A12	5,524,212	6/4/96	Somani et al.			
	A13	5,751,995	5/12/98	Sarangdar			
	A14	5,893,151	4/6/99	Merchant			
	A15	US 2002/0087807 A1	7/4/02	Gharachorloo et al.			
	A16	US 20040088492 A1	5/6/04	Glasco			
	A17	US 20040088493 A1	5/6/04	Glasco			
	A18	US 20040117559 A1	6/17/04	Glasco			

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation	
							Yes	No

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	B4	Martin et al., "Bandwidth Adaptive Snooping", Proceedings of the Eighth International Symposium on High-Performance Computer Architecture on February 2-6, 2002; pp. 251-262.
	B5	Sorin et al., "Specifying and Verifying a Broadcast and a Multicast Snooping Cache Coherence Protocol", IEEE Transactions on Parallel and Distributed Systems, Vol. 13, No. 6, June 2002.

Examiner	Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

DAC

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Morton et al.	Attorney Docket No.: NWISP052
Application No.: 10/966,161	Examiner: Not yet assigned
Filed: October 15, 2004	Group: 2187

Title: REDUCING PROBE TRAFFIC IN MULTIPROCESSOR SYSTEMS

CERTIFICATE OF MAILING
I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first-class mail on February 7, 2005 in envelope addressed to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.

Signed: _____
Mia Mitchell-Haynes

PETITION FOR APPLICATION BY OTHER THAN ALL THE INVENTORS
Pursuant to 37 C.F.R. §1.47 (a)

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicants Eric Morton, Rajesh Kota, and Adnan Khaleel (the "remaining joint inventors") hereby petition the Commissioner to accept for application the above-identified U.S. Patent Application by other than all of the inventors.

The above-referenced application names four (4) inventors: Eric Morton, Rajesh Kota, Adnan Khaleel, and David B. Glasco. The joint inventors Eric Morton, Rajesh Kota, and Adnan Khaleel have executed the application, however, Mr. Glasco has refused to execute the application.

Filed herewith in response to the Notice to File Missing Parts of Application (Filing Date Granted) is the Patent Declaration of the signing inventors with the signature block of the non-signing inventor, Mr. Glasco, left blank. In accordance with M.P.E.P. §409.09(a), it is respectfully submitted that this Declaration may be treated as having been signed by the remaining joint inventors, on behalf of the non-signing inventor, Mr. Glasco.

A Declaration of Facts in Support of Applying on Behalf of Omitted Inventors is also attached hereto and provides proof of the pertinent facts regarding the omitted inventor who refused to sign as required by 37 C.F.R. §1.47(a) and M.P.E.P. §409.03(d).

02/15/2005 SSANDARA 00000001 10966161
200.00 OP
04 FC:1463

In view of the refusal of the omitted inventor to sign the papers required for the above-identified application, the remaining joint inventors are believed to be entitled to make such an application on behalf of and as agents for the omitted inventors. The required fee pursuant to 37 C.F.R. §1.17(i) is enclosed.

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP

Joseph M. Villeneuve
Registration No. 37,460

P.O. Box 70250
Oakland, CA 94612-0250
(510) 663-1100

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Morton et al.

Attorney Docket No.: NWISP052

Application No.: 10/966,161

Examiner: Unassigned

Filed: October 15, 2004

Group: 2187

Title: REDUCING PROBE TRAFFIC IN MULTIPROCESSOR SYSTEMS

POWER OF ATTORNEY BY ASSIGNEE, 37 CFR §3.73 STATEMENT, AND EXCLUSION OF INVENTOR UNDER 37 CFR §3.71

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

NEWISYS, INC. is the assignee of the above-referenced patent application by virtue of an assignment document. The assignment document is/was recorded:

☐ at Reel ___, Frame(s) ___

☐ on _____

☒ submitted concurrently herewith

The assignee represents, pursuant to 37 C.F.R. §3.73(b), that the undersigned is a representative authorized and empowered to sign on behalf of the assignee.

Pursuant to 37 C.F.R. §§1.36 and 3.71, the assignee hereby revokes all powers of attorney previously given and hereby appoints the law firm of Beyer Weaver & Thomas, LLP and all practitioners who are associated with the **Customer Number 022434** as principal attorneys to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

Please send all correspondence for this application as follows:

Customer Number 022434

022434

Attorney Docket No. NWISP052

BEYER WEAVER& THOMAS, LLP
P.O. Box 70250
Oakland, CA 94612-0250

Please direct any calls to **Joseph M. Villeneuve** (510) 843-6200.

Further, pursuant to 37 C.F.R. §3.71, the assignee hereby states that prosecution of the above-referenced patent application is to be conducted to the exclusion of the inventor(s).

Assignee of Interest:

Company Name Newisys, Inc.
Address 10814 Jollyville Road
Bldg. 4, Ste. 300
Austin, TX 78738

Date 1/13/05

Name: Phil Hester
Title: CEO

Attorney Docket No. NWISP052

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Morton et al.	Attorney Docket No.: NWISP052
Application No.: 10/966,161	Examiner: Not yet assigned
Filed: October 15, 2004	Group: 2187
Title: REDUCING PROBE TRAFFIC IN MULTIPROCESSOR SYSTEMS	

DECLARATION OF FACTS IN SUPPORT OF APPLYING ON BEHALF OF OMITTED INVENTORS
Pursuant to 37 C.F.R. §1.47 (a)

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This declaration is made as to the facts that are relied upon to establish the *bona fide* effort made to secure the execution of the Declaration for the above-identified patent application by the nonsigning inventor, David B. Glasco. This declaration is being made by the available person having first-hand knowledge of the facts recited therein

I, Joseph M. Villeneuve, do hereby declare:

1. I am a patent attorney involved in the preparation of the above referenced application. The application names four inventors, Eric Morton, Rajesh Kota, Adnan Khaleel, and David B Glasco. All were employed by and/or under an obligation to assign the invention to Newisys, Inc. ("Newisys") at the time the invention of the subject application was made.

2. On August 20, 2004, my assistant, Mia Mitchell-Haynes, sent a Declaration for Original U.S. Patent Application ("Declaration"), Power of Attorney by Assignee ("Power of Attorney"), and an Assignment of Patent Application ("Assignment") to Don Blaszak, Project Manager at Newisys, by Federal Express requesting that he have each of the

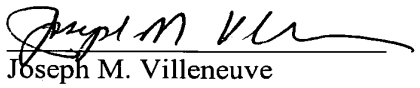
inventors sign and date the Declaration and Assignment for filing with the application in the U.S. Patent Office. A copy of the cover letter dated August 20, 2004, is attached as Exhibit A.

3. The application was filed without an executed Patent Declaration on October 15, 2004. A Notice to File Missing Parts was mailed November 24, 2004.

4. On December 23, 2004, my assistant, Mia Mitchell-Haynes, e-mailed a Declaration for Original U.S. Patent Application ("Declaration"), Power of Attorney by Assignee ("Power of Attorney"), and an Assignment of Patent Application ("Assignment") to Mr. Blaszak for execution by each of the inventors. A copy of Ms. Mitchell-Haynes' e-mail message of December 23, 2004 is attached hereto as Exhibit B.

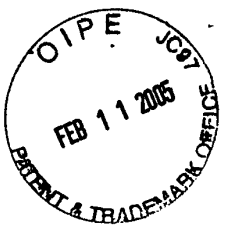
5. On January 31, 2005, I received an e-mail from Mr. Blaszak stating that David Glasco decided not to sign the Declaration. Included in Mr. Blaszak's e-mail are copies of e-mails exchanged between Richard Oehler, Chief Technology Officer of Newisys, and Mr. Glasco in which Mr. Glasco clearly and unequivocally indicates his refusal to sign the Declaration. A copy of Mr. Blaszak's e-mail of January 31, 2005, including the e-mail exchange between Mr. Glasco and Mr. Oehler is attached hereto as Exhibit C.

6. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.



Joseph M. Villeneuve
Reg No.: 37,460

2/7/05
Date



BEYER WEAVER & THOMAS, LLP

INTELLECTUAL PROPERTY LAW

2030 Addison Street, Seventh Floor, Berkeley, CA 94704
Telephone: (510) 843-6200 Facsimile: (510) 843-6203
www.beyerlaw.com

EXHIBIT A

August 20, 2004

By Federal Express

Don Blaszak
Newisys, Inc.
10814 Jollyville Road
Building 4, Suite 300
Austin, Tx 78738

Re: U.S. Patent Application Entitled: Reducing Probe Traffic in Multiprocessor Systems
Our File: NWISP052

Dear Don:

We have now revised the application in accordance with the Inventor's comments.

Enclosed please find a Declaration and an Assignment of rights to NEWISYS, Inc. for each of the inventors to execute, (a separate assignment document is enclosed for David Glasco's signature). Please have each Inventor sign and date each of the enclosed forms by their name.

Also enclosed is a Power of Attorney to be signed by Phil Hester, CEO. When all documents have been properly executed, please return the application together with the executed documents so that we may file them with the U.S. Patent and Trademark Office.

Please note that by law this application (as filed) will be published in the U.S. at 18 months from the earliest priority date. If the application will not be filed internationally, you may choose to request nonpublication, but this request **must** be made upon filing the application. You also have options of early publication and republication, but as these issues are complex, please telephone us should you have any questions on any aspect of publication.

Finally, we would again like to remind you of our duty to disclose the most pertinent prior art of which you are aware to the Patent and Trademark Office. If you can think of any pertinent references or patents, or any similar existing technology, please let us know. The duty to disclose prior art continues until the patent actually issues; if you become aware of other prior art in the future, please let us know.

Best regards,
BEYER WEAVER & THOMAS, LLP

Joseph M. Villeneuve
JMV:mmh
Enclosures
cc: Richard Oehler (w/out encls.)
Judith E. Brown (w/copy of cover letter & Application)

EXHIBIT B

From: Mia Mitchell
To: Glaszak, Don
Date: 12/23/2004 2:12:21 PM
Subject: Formal papers for NWISP052

Hello Don,

I am attaching an electronic copy of the application and drawings as filed with the Patent Office along with formal papers for the inventors execution in your application entitled "Reduced Probe Traffic in Multiprocessor Systems", filed on October 15, 2004.

The following documents are attached:

1. Declaration for Original U.S. Patent Application. *Please verify that the inventor's address is current.

2. Assignment of Patent Application. *I've attached a separate assignmend for David Glasco's signature.

3. Power of Attorney by Assignee. *This form is set-up for Phil Hester's signature.

Please have these documents signed and dated and returned to our office no later than January 17, 2004 (we have a deadline of 1/24/04 to file these documents).

Our new address is:

Attn: Mia Mitchell-Haynes
500 12th Street, Suite 200
Oakland, CA 94607

Thank you for your assistance with this matter.

Regards,

Mia

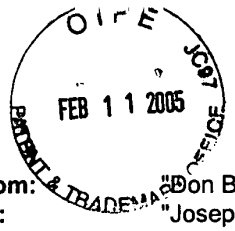


EXHIBIT C

From: "Don Blaszak" <don.blaszak@newisys.com>
To: "Joseph Villeneuve (E-mail)" <joev@beyerlaw.com>
Date: 1/31/2005 2:13:42 PM
Subject: NWISP052

Joe,

David has decided not to sign, but I do have the other signatures. How do we proceed?

Thanks, Don
512-340-9050 x229

-----Original Message-----
From: Rich Oehler
Sent: Monday, January 31, 2005 3:56 PM
To: Don Blaszak
Subject: FW: Hello

Don, after all of the dancing, we are going home alone.

Please tell Joe and have him start the next steps without David.

Rich

-----Original Message-----
From: David Glasco [mailto:daveglasco@swbell.net]
Sent: Monday, January 31, 2005 8:53 AM
To: Rich Oehler
Subject: RE: Hello

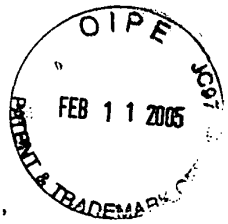
Rich,

I've decided not to sign the patent. Just too many
potential issues involved.

David

--- Rich Oehler <rich.oehler@newisys.com> wrote:

> David, I will be back in town Feb 1 afternoon
> through 4 afternoon. Will any of those days work for
> you for lunch, dinner or coffee?
>
> We are into the extension period on this application
> and we really need to conclude this process shortly.
>
> Rich
>
> -----Original Message-----
> From: David Glasco [mailto:daveglasco@swbell.net]
> Sent: Thursday, January 20, 2005 3:21 PM
> To: Rich Oehler
> Subject: Hello
>



>
> Hello Rich,
>
> I got your message - I have been traveling and
> swamped with meetings/work.
>
> I've not finished reading the patent application
> yet. I'll try to do so in the next week or so.
>
> Thanks,
> David
>
> 512-577-8693
> daveglasco@swbell.net
>
>

CC: "inventions" <inventions@newisys.com>, "Rich Oehler" <rich.oehler@newisys.com>

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Morton et al.

Attorney Docket No.: NWISP052

Application No.: 10/966,161

Examiner: Not yet assigned

Filed: October 15, 2004

Group: 2187

Title: REDUCING PROBE TRAFFIC IN MULTIPROCESSOR SYSTEMS

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first-class mail on February 7, 2005 in an envelope addressed to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.

Signed: _____

Mia Mitchell-Haynes

RESPONSE TO NOTICE TO FILE MISSING PARTS

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Enclosed herewith is the executed Declaration and Power of Attorney in response to the Notice to File Missing Parts of Application--Filing Date Granted mailed November 24, 2004. Please file these documents in the subject application.

Applicant hereby request a one month(s) extension of time in which to respond to the Notice to File Missing Parts of Application--Filing Date Granted mailed November 24, 2004.

Enclosed is our Check No. 10214 for $1,700.00 in payment of the filing fee, excess claims fee, surcharge, and one-month(s) extension fee (if any) for a Large Entity. The Commissioner is authorized to charge any additional fees that may be due to our Deposit Account No. 500388 (Order No. 50-0388).

02/15/2005 SSANDARA 00000001 10966161
05 FC:1251 120.00 OP

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP

Joseph M. Villeneuve
Registration No. 37,460

P.O. Box 70250
Oakland, CA 94612-0250
(510) 663-1100

02/15/2005 SSANDARA 00012463400
Repln. Ref: 10966161
DAM:500388 Name/Number:
FC: 9204 $170.00 CR

IFW

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
10/966,161	10/15/2004	Eric Morton	NWISP052

CONFIRMATION NO. 6289

022434
BEYER WEAVER & THOMAS LLP
P.O. BOX 778
BERKELEY, CA 94704-0778

FORMALITIES LETTER

OC000000014447731

Date Mailed: 11/24/2004

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
  Applicant must submit $ **790** *to complete the basic filing fee for a non-small entity. If appropriate, applicant may make a written assertion of entitlement to small entity status and pay the small entity filing fee (37 CFR 1.27).*
- The oath or declaration is missing.
  A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(e) of $130 for a non-small entity, must be submitted with the missing items identified in this letter.

The applicant needs to satisfy supplemental fees problems indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- Additional claim fees of **$90** as a non-small entity, including any required multiple dependent claim fee, are required. Applicant must submit the additional claim fees or cancel the additional claims for which fees are due.

02/15/2005 SSANDARA 00000001 10966161

SUMMARY OF FEES DUE:

01 FC:1001	790.00 OP
02 FC:1051	130.00 OP
03 FC:1202	250.00 OP

Total additional fee(s) required for this application is **$1010** for a Large Entity

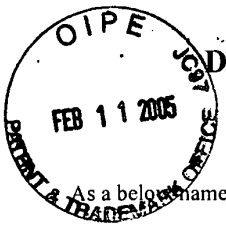
- **$790** Statutory basic filing fee.
- **$130** Late oath or declaration Surcharge.

- Total additional claim fee(s) for this application is **$90**
  - **$90** for **5** total claims over 20.

Replies should be mailed to: Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

A copy of this notice MUST be returned with the reply.

Customer Service Center
Initial Patent Examination Division (703) 308-1202
PART 2 - COPY TO BE RETURNED WITH RESPONSE



DECLARATION FOR ORIGINAL U.S. PATENT APPLICATION

Attorney's Docket No. **NWISP052**

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: **REDUCING PROBE TRAFFIC IN MULTIPROCESSOR SYSTEMS**, the specification of which,

(check one)

1. ☐ is attached hereto.

2. ☒ was filed on **October 15, 2004** as
U.S. Application No. **10/966,161**
and was amended on _____.

3. ☐ was filed on _____ as
International PCT Application Serial No. _____
and was amended on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, CFR §1.56.

Prior Foreign Application(s)

I hereby claim foreign priority benefits under Title 35, United States code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

			Priority Benefits Claimed?
_____ (Appl. No.)	_____ (Country)	_____ (Date Filed- Day/Month/Year)	__ Yes __ No
_____ (Appl. No.)	_____ (Country)	_____ (Date Filed- Day/Month/Year)	__ Yes __ No

Provisional Application(s)

I hereby claim the benefit under 35 U.S.C. §119(e) of any United States provisional application(s) listed below:

_____ (Application No.)	_____ (Filing Date)
_____ (Application No.)	_____ (Filing Date)

Prior U.S. Application(s)

I hereby claim the benefit under Title 35, United Sates Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this applications is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

10/288,347 (Application No.)	**11/4/2002** (Filing Date)	**Pending** (Status - patented, pending, abandoned)
_____ (Application No.)	_____ (Filing Date)	_____ (Status - patented, pending, abandoned)

Send Correspondence To: **Customer Number: 022434**

022434

Direct Telephone Calls To: **Joseph M. Villeneuve at telephone number (510) 843-6200**

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Typewritten Full Name of Sole or First Inventor: **Eric Morton** Citizenship: **United States**

Inventor's signature: _____ **Date of Signature:** 1/13/05

Residence: (City) **Austin** (State/Country) **Texas/U.S.**

Post Office Address: **12901 Majestic Oaks Drive, Austin, TX 78732**

Typewritten Full Name of Sole or Second Inventor: **Rajesh Kota** Citizenship: **India**

Inventor's signature: Rajesh **Date of Signature:** 1/13/05

Residence: (City) **Austin** (State/Country) **Texas/U.S.**

Post Office Address: **5817 Miramonte Drive, Austin, TX 78759**

Typewritten Full Name of Sole or Third Inventor: **Adnan Khaleel** Citizenship: **India**

Inventor's signature: _____ **Date of Signature:** 1/13/05

Residence: (City) **Austin** (State/Country) **Texas/U.S.**

Post Office Address: **10430 Morado Circle, Apt. #2111, Austin, TX**

Typewritten Full Name of Sole or Fourth Inventor: **David B. Glasco** Citizenship: **United States**

Inventor's signature: _____ **Date of Signature:** _____

Residence: (City) **Austin** (State/Country) **Texas/U.S.**

Post Office Address: **10337 Ember Glen Drive, Austin, TX 78726**

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APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
10/966,161	10/15/2004	Eric Morton	NWISP052

CONFIRMATION NO. 6289

022434
BEYER WEAVER & THOMAS LLP
P.O. BOX 778
BERKELEY, CA 94704-0778

FORMALITIES LETTER

OC000000014447731

Date Mailed: 11/24/2004

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
  Applicant must submit $ **790** *to complete the basic filing fee for a non-small entity. If appropriate, applicant may make a written assertion of entitlement to small entity status and pay the small entity filing fee (37 CFR 1.27).*
- The oath or declaration is missing.
  A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(e) of $130 for a non-small entity, must be submitted with the missing items identified in this letter.

The applicant needs to satisfy supplemental fees problems indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- Additional claim fees of **$90** as a non-small entity, including any required multiple dependent claim fee, are required. Applicant must submit the additional claim fees or cancel the additional claims for which fees are due.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is **$1010** for a Large Entity

- **$790** Statutory basic filing fee.
- **$130** Late oath or declaration Surcharge.

- Total additional claim fee(s) for this application is **$90**
  - **$90** for **5** total claims over 20.

Replies should be mailed to: Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

A copy of this notice MUST be returned with the reply.

Customer Service Center
Initial Patent Examination Division (703) 308-1202

PART 3 - OFFICE COPY

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CERTIFICATE OF EXPRESS MAILING

I hereby certify that this paper and the documents and/or fees referred to as attached therein are being deposited with the United States Postal Service on October 15, 2004 in an envelope as "Express Mail Post Office to Addressee" service under 37 CFR §1.10, Mailing Label Number **EV332820115US**, addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Jeffrey Ng

Attorney Docket No.: NWISP052

First Named Inventor: Morton

UTILITY PATENT APPLICATION TRANSMITTAL (37 CFR. § 1.53(b))

(Continuation, Divisional or Continuation-in-part application)

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir: This is a request for filing a patent application under 37 CFR. § 1.53(b) in the name of inventors:
Eric Morton, Rajesh Kota, Adnan Khaleel and David B. Glasco

For: **REDUCING PROBE TRAFFIC IN MULTIPROCESSOR SYSTEMS**

Assigned to : Newisys, Inc.

This application is a ☐ Continuation ☐ Divisional ☒ Continuation-in-part

of prior Application No.: 10/288,347, from which priority under 35 U.S.C. §120 is claimed.

The specification has been amended to claim priority from the parent application, or such amendment is included in a separate sheet.

Application Elements:

☒ **54** Pages of Specification, Claims and Abstract
☒ **25** Sheets of formal Drawings
☐ Declaration
- ☐ Newly executed
- ☐ Copy from a prior application (37 CFR 1.63(d) for a continuation or divisional). The entire disclosure of the prior application from which a copy of the declaration is herein supplied is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
  - ☐ Deletion of inventors Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

Accompanying Application Parts:

- ☐ Do not publish this application. Nonpublication Request is attached.
- ☐ Assignment and Assignment Recordation Cover Sheet (recording fee of $40.00 enclosed)
- ☐ Power of Attorney
- ☐ 37 CFR 3.73(b) Statement by Assignee
- ☐ Information Disclosure Statement with Form PTO-1449 ☐ Copies of IDS Citations
- ☐ Preliminary Amendment (*New claims numbered after highest original claim in prior application.*)
- ☒ Return Receipt Postcard
- ☐ Other:

Claim For Foreign Priority

☐ Priority of Application No. filed on is claimed under 35 U.S.C. § 119.

- ☐ The certified copy has been filed in prior application U.S. Application No.
- ☐ The certified copy will follow.

Extension of Time for Prior Pending Application

☐ A Petition for Extension of Time is being concurrently filed in the prior pending application. A copy of the Petition for Extension of Time is attached.

Fee Calculation (37 CFR § 1.16)

☒ **PLEASE DEFER THE PAYMENT OF THE FILING FEES AT THIS TIME.**

General Authorization for Petition for Extension of Time (37 CFR §1.136)

☒ Applicants hereby make and generally authorize any Petitions for Extensions of Time as may be needed for any subsequent filings. The Commissioner is also authorized to charge any extension fees under 37 CFR §1.17 as may be needed to Deposit Account No. 500388 (Order No. NWISP052).

☒ Please send correspondence to the following address:

Customer Number 022434

Date: October 15, 2004

Joseph M. Villeneuve
Registration No. 37,460

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF EXPRESS MAILING

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Jeffrey Ng

Attorney Docket No.: NWISP052

First Named Inventor: Morton

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Date: October 15, 2004

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Jeffrey Ng

Attorney Docket No.: NWISP052

First Named Inventor: Morton

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☒ Please send correspondence to the following address:

Customer Number 022434

Date: October 15, 2004

Joseph M. Villeneuve
Registration No. 37,460

Attorney Docket No. NWISP052

PATENT APPLICATION

REDUCING PROBE TRAFFIC IN MULTIPROCESSOR SYSTEMS

Inventors: Eric Morton of
Austin, Texas
United States citizen

Rajesh Kota of
Austin, Texas
Citizen of India

Adnan Khaleel of
Austin, Texas
Citizen of India

David B. Glasco of
Austin, Texas
United States citizen

Assignee: Newisys, Inc.
A Delaware corporation

BEYER WEAVER & THOMAS, LLP
P.O. Box 778
Berkeley, California 94704-0778
(510) 843-6200

REDUCING PROBE TRAFFIC IN MULTIPROCESSOR SYSTEMS

CROSS-REFERENCE TO RELATED APPLICATIONS

The present application is a continuation-in-part of and claims priority under 35 U.S.C. 120 to U.S. Patent Application No. 10/288,347 for METHODS AND APPARATUS FOR MANAGING PROBE REQUESTS filed on November 4, 2002 (Attorney Docket No. NWISP024), the entire disclosure of which is incorporated herein by reference for all purposes. The subject matter described in the present application is also related to U.S. Patent Application No. 10/288,399 for METHODS AND APPARATUS FOR MANAGING PROBE REQUESTS filed on November 4, 2002 (Attorney Docket No. NWISP025), the entire disclosure of which is incorporated herein by reference for all purposes.

BACKGROUND OF THE INVENTION

The present invention generally relates to accessing data in a multiple processor system. More specifically, the present invention provides techniques for reducing memory transaction traffic in a multiple processor system.

Data access in multiple processor systems can raise issues relating to cache coherency. Conventional multiple processor computer systems have processors coupled to a system memory through a shared bus. In order to optimize access to data in the system memory, individual processors are typically designed to work with cache memory. In one example, each processor has a cache that is loaded with data that the processor frequently accesses. The cache is read or written by a processor. However, cache coherency problems arise because multiple copies of the same data can co-exist in systems having multiple processors and multiple cache memories. For example, a frequently accessed data block corresponding to a memory line may be loaded into the cache of two different processors. In one example, if both processors attempt to write new values into the data block at the same time, different data values may result. One value may be written into the first cache while a different value is written into the

second cache. A system might then be unable to determine what value to write through to system memory.

A variety of cache coherency mechanisms have been developed to address such problems in multiprocessor systems. One solution is to simply force all processor writes to go through to memory immediately and bypass the associated cache. The write requests can then be serialized before overwriting a system memory line. However, bypassing the cache significantly decreases efficiency gained by using a cache. Other cache coherency mechanisms have been developed for specific architectures. In a shared bus architecture, each processor checks or snoops on the bus to determine whether it can read or write a shared cache block. In one example, a processor only writes an object when it owns or has exclusive access to the object. Each corresponding cache object is then updated to allow processors access to the most recent version of the object.

Bus arbitration is used when both processors attempt to write the same shared data block in the same clock cycle. Bus arbitration logic decides which processor gets the bus first. Although, cache coherency mechanisms such as bus arbitration are effective, using a shared bus limits the number of processors that can be implemented in a single system with a single memory space.

Other multiprocessor schemes involve individual processor, cache, and memory systems connected to other processors, cache, and memory systems using a network backbone such as Ethernet or Token Ring. Multiprocessor schemes involving separate computer systems each with its own address space can avoid many cache coherency problems because each processor has its own associated memory and cache. When one processor wishes to access data on a remote computing system, communication is explicit. Messages are sent to move data to another processor and messages are received to accept data from another processor using standard network protocols such as TCP/IP. Multiprocessor systems using explicit communication including transactions such as sends and receives are referred to as systems using multiple private memories. By contrast, multiprocessor system using implicit communication including

transactions such as loads and stores are referred to herein as using a single address space.

Multiprocessor schemes using separate computer systems allow more processors to be interconnected while minimizing cache coherency problems. However, it would take substantially more time to access data held by a remote processor using a network infrastructure than it would take to access data held by a processor coupled to a system bus. Furthermore, valuable network bandwidth would be consumed moving data to the proper processors. This can negatively impact both processor and network performance.

Performance limitations have led to the development of a point-to-point architecture for connecting processors in a system with a single memory space. In one example, individual processors can be directly connected to each other through a plurality of point-to-point links to form a cluster of processors. Separate clusters of processors can also be connected. The point-to-point links significantly increase the bandwidth for coprocessing and multiprocessing functions. However, using a point-to-point architecture to connect multiple processors in a multiple cluster system sharing a single memory space presents its own problems.

Consequently, it is desirable to provide techniques for improving data access and cache coherency in systems having multiple processors connected using point-to-point links.

SUMMARY OF THE INVENTION

According to the present invention, various techniques are provided for reducing traffic relating to memory transactions in multi-processor systems. According to various specific embodiments, a computer system having a plurality of processing nodes interconnected by a first point-to-point architecture is provided. Each processing node has a cache memory associated therewith. A probe filtering unit is operable to receive probes corresponding to memory lines from the processing nodes and to transmit the probes only to selected ones of the processing nodes with reference to probe filtering information. The probe filtering information is representative of states associated with selected ones of the cache memories.

According to other embodiments, methods and apparatus are provided for reducing probe traffic in a computer system comprising a plurality of processing nodes interconnected by a first point-to-point architecture. A probe corresponding to a memory line is transmitted from a first one of the processing nodes only to a probe filtering unit. The probe is evaluated with the probe filtering unit to determine whether a valid copy of the memory line is in any of the cache memories. The evaluation is done with reference to probe filtering information associated with the probe filtering unit and representative of states associated with selected ones of the cache memories. The probe is transmitted from the probe filtering unit only to selected ones of the processing nodes identified by the evaluating. Probe responses from the selected processing nodes are accumulated by the probe filtering unit. Only the probe filtering unit responds to the first processing node.

A further understanding of the nature and advantages of the present invention may be realized by reference to the remaining portions of the specification and the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention may best be understood by reference to the following description taken in conjunction with the accompanying drawings, which are illustrative of specific embodiments of the present invention.

Figure 1A and 1B are diagrammatic representation depicting a system having multiple clusters.

Figure 2 is a diagrammatic representation of a cluster having a plurality of processors.

Figure 3 is a diagrammatic representation of a cache coherence controller.

Figure 4 is a diagrammatic representation showing a transaction flow for a data access request from a processor in a single cluster.

Figure 5A-5D are diagrammatic representations showing cache coherence controller functionality.

Figure 6 is a diagrammatic representation depicting a transaction flow for a request with multiple probe responses.

Figure 7 is a diagrammatic representation showing a cache coherence directory.

Figure 8 is a diagrammatic representation showing probe filter information that can be used to reduce the number of probes transmitted to various clusters.

Figure 9 is a diagrammatic representation showing a transaction flow for probing of a home cluster without probing of other clusters.

Figure 10 is a diagrammatic representation showing a transaction flow for probing of a single remote cluster.

Figure 11 is a flow process diagram showing the handling of a request with probe filter information.

Figure 12 is a diagrammatic representation showing memory controller filter information.

Figure 13 is a diagrammatic representation showing a transaction flow for probing a single remote cluster without probing a home cluster.

Figure 14 is a flow process diagram showing the handling of a request at a home cluster cache coherence controller using memory controller filter information.

Figure 15 is a diagrammatic representation showing a transaction flow for a cache coherence directory eviction of an entry corresponding to a dirty memory line.

Figure 16 is a diagrammatic representation showing a transaction flow for a cache coherence directory eviction of an entry corresponding to a clean memory line.

Figure 17 is a diagrammatic representation of a cache coherence controller according to a specific embodiment of the invention.

Figure 18 is a diagrammatic representation of a cluster having a plurality of processing nodes and a probe filtering unit.

Figure 19 is an exemplary representation of a processing node.

Figure 20 is a flowchart illustrating local probe filtering according to a specific embodiment of the invention.

Figure 21 is a diagrammatic representation of a transaction flow in which local probe filtering is facilitated according to a specific embodiment of the invention.

Figure 22 is a diagrammatic representation of another transaction flow in which local probe filtering is facilitated according to a specific embodiment of the invention.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS

Reference will now be made in detail to some specific embodiments of the invention including the best modes contemplated by the inventors for carrying out the invention. Examples of these specific embodiments are illustrated in the accompanying drawings. While the invention is described in conjunction with these specific embodiments, it will be understood that it is not intended to limit the invention to the described embodiments. On the contrary, it is intended to cover alternatives, modifications, and equivalents as may be included within the spirit and scope of the invention as defined by the appended claims. Multi-processor architectures having point-to-point communication among their processors are suitable for implementing specific embodiments of the present invention. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. The present invention may be practiced without some or all of these specific details. Well-known process operations have not been described in detail in order not to unnecessarily obscure the present invention. Furthermore, the present application's reference to a particular singular entity includes that possibility that the methods and apparatus of the present invention can be implemented using more than one entity, unless the context clearly dictates otherwise.

According to various embodiments, techniques are provided for increasing data access efficiency in a multiple processor system. In a point-to-point architecture, a cluster of processors includes multiple processors directly connected to each other through point-to-point links. By using point-to-point links instead of a conventional shared bus or external network, multiple processors are used efficiently in a system sharing the same memory space. Processing and network efficiency are also improved by avoiding many of the bandwidth and latency limitations of conventional bus and external network based multiprocessor architectures. According to various embodiments, however, linearly increasing the number of processors in a point-to-point architecture leads to an exponential increase in the number of links used to connect the multiple processors. In order to reduce the number of links used and to further modularize a multiprocessor system using a point-to-point architecture, multiple clusters may be used.

According to some embodiments, multiple processor clusters are interconnected using a point-to-point architecture. Each cluster of processors includes a cache coherence controller used to handle communications between clusters. In one embodiment, the point-to-point architecture used to connect processors are used to connect clusters as well.

By using a cache coherence controller, multiple cluster systems can be built using processors that may not necessarily support multiple clusters. Such a multiple cluster system can be built by using a cache coherence controller to represent non-local nodes in local transactions so that local nodes do not need to be aware of the existence of nodes outside of the local cluster. More detail on the cache coherence controller will be provided below.

In a single cluster system, cache coherency can be maintained by sending all data access requests through a serialization point. Any mechanism for ordering data access requests (also referred to herein as requests and memory requests) is referred to herein as a serialization point. One example of a serialization point is a memory controller. Various processors in the single cluster system send data access requests to one or more memory controllers. In one example, each memory controller is configured to serialize or lock the data access requests so that only one data access request for a given memory line is allowed at any particular time. If another processor attempts to access the same memory line, the data access attempt is blocked until the memory line is unlocked. The memory controller allows cache coherency to be maintained in a multiple processor, single cluster system.

A serialization point can also be used in a multiple processor, multiple cluster system where the processors in the various clusters share a single address space. By using a single address space, internal point-to-point links can be used to significantly improve intercluster communication over traditional external network based multiple cluster systems. Various processors in various clusters send data access requests to a memory controller associated with a particular cluster such as a home cluster. The memory controller can similarly serialize all data requests from the different clusters.

However, a serialization point in a multiple processor, multiple cluster system may not be as efficient as a serialization point in a multiple processor, single cluster system. That is, delay resulting from factors such as latency from transmitting between clusters can adversely affect the response times for various data access requests. It should be noted that delay also results from the use of probes in a multiple processor environment.

Although delay in intercluster transactions in an architecture using a shared memory space is significantly less than the delay in conventional message passing environments using external networks such as Ethernet or Token Ring, even minimal delay is a significant factor. In some applications, there may be millions of data access requests from a processor in a fraction of a second. Any delay can adversely impact processor performance.

According to various embodiments, probe management is used to increase the efficiency of accessing data in a multiple processor, multiple cluster system. A mechanism for eliciting a response from a node to maintain cache coherency in a system is referred to herein as a probe. In one example, a mechanism for snooping a cache is referred to as a probe. A response to a probe can be directed to the source or target of the initiating request. Any mechanism for filtering or reducing the number of probes and requests transmitted to various nodes is referred to herein as managing probes. In one example, managing probes entails characterizing a request to determine if a probe can be transmitted to a reduced number of entities.

In typical implementations, requests are sent to a memory controller that broadcasts probes to various nodes in a system. In such a system, no knowledge of the cache line state needs to be maintained by the memory controller. All nodes in the system are probed and the request cluster receives a response from each node. In a system with a coherence directory, state information associated with various memory lines can be used to reduce the number of transactions. Any mechanism for maintaining state information associated with various memory lines is referred to herein as a coherence directory. According to some embodiments, a coherence directory includes information for memory lines in a local cluster that are cached in a

remote cluster. According to others, such a directory includes information for locally cached lines. According to various embodiments, a coherence directory is used to reduce the number of probes to remote quads by inferring the state of local caches. According to some embodiments, such a directory mechanism is used in a single cluster system or within a cluster in a multi-cluster system to reduce the number of probes within a cluster.

Figure 1A is a diagrammatic representation of one example of a multiple cluster, multiple processor system that can use the techniques of the present invention. Each processing cluster 101, 103, 105, and 107 can include a plurality of processors. The processing clusters 101, 103, 105, and 107 are connected to each other through point-to-point links 111a-f. In one embodiment, the multiple processors in the multiple cluster architecture shown in Figure 1A share the same memory space. In this example, the point-to-point links 111a-f are internal system connections that are used in place of a traditional front-side bus to connect the multiple processors in the multiple clusters 101, 103, 105, and 107. The point-to-point links may support any point-to-point protocol.

Figure 1B is a diagrammatic representation of another example of a multiple cluster, multiple processor system that can use the techniques of the present invention. Each processing cluster 121, 123, 125, and 127 can be coupled to a switch 131 through point-to-point links 141a-d. It should be noted that using a switch and point-to-point links allows implementation with fewer point-to-point links when connecting multiple clusters in the system. A switch 131 can include a processor with a coherence protocol interface. According to various implementations, a multicluster system shown in Figure 1A is expanded using a switch 131 as shown in Figure 1B.

Figure 2 is a diagrammatic representation of a multiple processor cluster, such as the cluster 101 shown in Figure 1A. Cluster 200 includes processors 202a-202d, one or more Basic I/O systems (BIOS) 204, a memory subsystem comprising memory banks 206a-206d, point-to-point communication links 208a-208e, and a service processor 212. The point-to-point communication links are configured to allow interconnections between processors 202a-202d, I/O switch 210, and cache coherence

controller 230. The service processor 212 is configured to allow communications with processors 202a-202d, I/O switch 210, and cache coherence controller 230 via a JTAG interface represented in Figure 2 by links 214a-214f. It should be noted that other interfaces are supported. It should also be noted that in some implementations, a service processor is not included in multiple processor clusters. I/O switch 210 connects the rest of the system to I/O adapters 216 and 220. It should further be noted that the terms node and processor are often used interchangeably herein. However, it should be understood that according to various implementations, a node (e.g., processors 202a-202d) may comprise multiple sub-units, e.g., CPUs, memory controllers, I/O bridges, etc.

According to specific embodiments, the service processor of the present invention has the intelligence to partition system resources according to a previously specified partitioning schema. The partitioning can be achieved through direct manipulation of routing tables associated with the system processors by the service processor which is made possible by the point-to-point communication infrastructure. The routing tables are used to control and isolate various system resources, the connections between which are defined therein.

The processors 202a-d are also coupled to a cache coherence controller 230 through point-to-point links 232a-d. Any mechanism or apparatus that can be used to provide communication between multiple processor clusters while maintaining cache coherence is referred to herein as a cache coherence controller. The cache coherence controller 230 can be coupled to cache coherence controllers associated with other multiprocessor clusters. It should be noted that there can be more than one cache coherence controller in one cluster. The cache coherence controller 230 communicates with both processors 202a-d as well as remote clusters using a point-to-point protocol.

More generally, it should be understood that the specific architecture shown in Figure 2 is merely exemplary and that embodiments of the present invention are contemplated having different configurations and resource interconnections, and a variety of alternatives for each of the system resources shown. However, for purpose of illustration, specific details of server 200 will be assumed. For example, most of the

resources shown in Figure 2 are assumed to reside on a single electronic assembly. In addition, memory banks 206a-206d may comprise double data rate (DDR) memory which is physically provided as dual in-line memory modules (DIMMs). I/O adapter 216 may be, for example, an ultra direct memory access (UDMA) controller or a small computer system interface (SCSI) controller which provides access to a permanent storage device. I/O adapter 220 may be an Ethernet card adapted to provide communications with a network such as, for example, a local area network (LAN) or the Internet.

According to a specific embodiment and as shown in Figure 2, both of I/O adapters 216 and 220 provide symmetric I/O access. That is, each provides access to equivalent sets of I/O. As will be understood, such a configuration would facilitate a partitioning scheme in which multiple partitions have access to the same types of I/O. However, it should also be understood that embodiments are envisioned in which partitions without I/O are created. For example, a partition including one or more processors and associated memory resources, i.e., a memory complex, could be created for the purpose of testing the memory complex.

According to one embodiment, service processor 212 is a Motorola MPC855T microprocessor which includes integrated chipset functions. The cache coherence controller 230 is an Application Specific Integrated Circuit (ASIC) supporting the local point-to-point coherence protocol. The cache coherence controller 230 can also be configured to handle a non-coherent protocol to allow communication with I/O devices. In one embodiment, the cache coherence controller 230 is a specially configured programmable chip such as a programmable logic device or a field programmable gate array.

Figure 3 is a diagrammatic representation of one example of a cache coherence controller 230. According to various embodiments, the cache coherence controller includes a protocol engine 305 configured to handle packets such as probes and requests received from processors in various clusters of a multiprocessor system. The functionality of the protocol engine 305 can be partitioned across several engines to improve performance. In one example, partitioning is done based on packet type

(request, probe and response), direction (incoming and outgoing), or transaction flow (request flows, probe flows, etc).

The protocol engine 305 has access to a pending buffer 309 that allows the cache coherence controller to track transactions such as recent requests and probes and associate the transactions with specific processors. Transaction information maintained in the pending buffer 309 can include transaction destination nodes, the addresses of requests for subsequent collision detection and protocol optimizations, response information, tags, and state information.

The cache coherence controller has an interface such as a coherent protocol interface 307 that allows the cache coherence controller to communicate with other processors in the cluster as well as external processor clusters. The cache coherence controller can also include other interfaces such as a non-coherent protocol interface 311 for communicating with I/O devices. According to various embodiments, each interface 307 and 311 is implemented either as a full crossbar or as separate receive and transmit units using components such as multiplexers and buffers. It should be noted, however, that the cache coherence controller 230 does not necessarily need to provide both coherent and non-coherent interfaces. It should also be noted that a cache coherence controller in one cluster can communicate with a cache coherence controller in another cluster.

Figure 4 is a diagrammatic representation showing the transactions for a cache request from a processor in a system having a single cluster without using a cache coherence controller or other probe management mechanism. A processor 401-1 sends an access request such as a read memory line request to a memory controller 403-1. The memory controller 403-1 may be associated with this processor, another processor in the single cluster or may be a separate component such as an ASIC or specially configured Programmable Logic Device (PLD). To preserve cache coherence, only one processor is typically allowed to access a memory line corresponding to a shared address space at anyone given time. To prevent other processors from attempting to access the same memory line, the memory line can be locked by the memory controller 403-1. All other requests to the same memory line are blocked or queued. Access by

another processor is typically only allowed when the memory controller 403-1 unlocks the memory line.

The memory controller 403-1 then sends probes to the local cache memories 405, 407, and 409 to determine cache states. The local cache memories 405, 407, and 409 then in turn send probe responses to the same processor 401-2. The memory controller 403-1 also sends an access response such as a read response to the same processor 401-3. The processor 401-3 can then send a done response to the memory controller 403-2 to allow the memory controller 403-2 to unlock the memory line for subsequent requests. It should be noted that CPU 401-1, CPU 401-2, and CPU 401-3 refer to the same processor.

Figures 5A-5D are diagrammatic representations depicting cache coherence controller operation. The use of a cache coherence controller in multiprocessor clusters allows the creation of a multiprocessor, multicluster coherent domain without affecting the functionality of local nodes in each cluster. In some instances, processors may only support a protocol that allows for a limited number of processors in a single cluster without allowing for multiple clusters. The cache coherence controller can be used to allow multiple clusters by making local processors believe that the non-local nodes are merely a one or more local nodes embodied in the cache coherence controller. In one example, the processors in a cluster do not need to be aware of processors in other clusters. Instead, the processors in the cluster communicate with the cache coherence controller as though the cache coherence controller were representing all non-local nodes. In addition, although generally a node may correspond to one or a plurality of resources (including, for example, a processor), it should be noted that the terms node and processor are often used interchangeably herein. According to a particular implementation, a node comprises multiple sub-units, e.g., CPUs, memory controllers, I/O bridges, etc.

It should be noted that nodes in a remote cluster will be referred to herein as non-local nodes or as remote nodes. However, non-local nodes refer to nodes not in a request cluster generally and includes nodes in both a remote cluster and nodes in a home cluster. A cluster from which a data access or cache access request originates is

referred to herein as a request cluster. A cluster containing a serialization point is referred to herein as a home cluster. Other clusters are referred to as remote clusters. The home cluster and the remote cluster are also referred to herein as non-local clusters.

Figure 5A shows the cache coherence controller acting as an aggregate remote cache. When a processor 501-1 generates a data access request to a local memory controller 503-1, the cache coherence controller 509 accepts the probe from the local memory controller 503-1 and forwards it to non-local node portion 511. It should be noted that a coherence protocol can contain several types of messages. In one example, a coherence protocol includes four types of messages; data or cache access requests, probes, responses or probe responses, and data packets. Data or cache access requests usually target the home node memory controller. Probes are used to query each cache in the system. The probe packet can carry information that allows the caches to properly transition the cache state for a specified line. Responses are used to carry probe response information and to allow nodes to inform other nodes of the state of a given transaction. Data packets carry request data for both write requests and read responses.

According to various embodiments, the memory address resides at the local memory controller. As noted above, nodes including processors and cache coherence controllers outside of a local cluster are referred to herein as non-local nodes. The cache coherence controller 509 then accumulates the response from the non-local nodes and sends a single response in the same manner that local nodes associated with cache blocks 505 and 507 send a single response to processor 501-2. Local processors may expect a single probe response for every local node probed. The use of a cache coherence controller allows the local processors to operate without concern as to whether non-local nodes exist.

It should also be noted that components such as processor 501-1 and processor 501-2 refer herein to the same component at different points in time during a transaction sequence. For example, processor 501-1 can initiate a data access request

and the same processor 501-2 can later receive probe responses resulting from the request.

Figure 5B shows the cache coherence controller acting as a probing agent pair. When the cache coherence controller 521-1 receives a probe from non-local nodes 531, the cache coherence controller 521-1 accepts the probe and forwards the probe to local nodes associated with cache blocks 523, 525, and 527. The cache coherence controller 521-2 then forwards a final response to the non-local node portion 531. In this example, the cache coherence controller is both the source and the destination of the probes. The local nodes associated with cache blocks 523, 525, and 527 behave as if the cache coherence controller were a local processor with a local memory request.

Figure 5C shows the cache coherence controller acting as a remote memory. When a local processor 541-1 generates an access request that targets remote memory, the cache coherence controller 543-1 forwards the request to the non-local nodes 553. When the remote request specifies local probing, the cache coherence controller 543-1 generates probes to local nodes and the probed nodes provide responses to the processor 541-2. Once the cache coherence controller 543-1 has received data from the non-local node portion 553, it forwards a read response to the processor 541-3. The cache coherence controller also forwards the final response to the remote memory controller associated with non-local nodes 553.

Figure 5D shows the cache coherence controller acting as a remote processor. When the cache coherence controller 561-1 at a first cluster receives a request from a processor in a second cluster, the cache coherence controller acts as a first cluster processor on behalf of the second cluster processor. The cache coherence controller 561-1 accepts the request from portion 575 and forwards it to a memory controller 563-1. The cache coherence controller 561-2 then accumulates all probe responses as well as the data fetched and forwards the final response to the memory controller 563-2 as well as to non-local nodes 575.

By allowing the cache coherence controller to act as an aggregate remote cache, probing agent pair, remote memory, and remote processor, multiple cluster systems can

be built using processors that may not necessarily support multiple clusters. The cache coherence controller can be used to represent non-local nodes in local transactions so that local nodes do not need to be aware of the existence of nodes outside of the local cluster.

Figure 6 is a diagrammatic representation depicting the transactions for a data request from a local processor sent to a non-local cluster using a cache coherence controller. The multicluster system includes a request cluster 600, a home cluster 620, and a remote cluster 640. As noted above, the home cluster 620 and the remote cluster 640 as well as any other clusters excluding the request cluster 600 are referred to herein as non-local clusters. Processors and cache coherence controllers associated with local and non-local clusters are similarly referred to herein as local processors, local cache coherence controllers, non-local processors, and non-local cache coherence controllers, respectively.

According to various embodiments, processor 601-1 in a local cluster 600 sends a data access request such as a read request to a cache coherence controller 603-1. The cache coherence controller 603-1 tracks the transaction in the pending buffer of Figure 3 and forwards the request to a cache coherence controller 621-1 in a home cluster 620. The cache coherence controller 621-1 at the home cluster 620 receives the access request and tracks the request in its pending buffer. In one example, information associated with the requests are stored in the pending buffer. The cache coherence controller 621-1 forwards the access request to a memory controller 623-1 also associated with the home cluster 620. At this point, the memory controller 623-1 locks the memory line associated with the request. In one example, the memory line is a unique address in the memory space shared by the multiple processors in the request cluster 600, home cluster 620, and the remote cluster 640. The memory controller 623-1 generates a probe associated with the data access request and forwards the probe to local nodes associated with cache blocks 625 and 627 as well as to cache coherence controller 621-2.

It should be noted that although messages associated with requests, probes, responses, and data are described as forwarded from one node to another, the messages

themselves may contain variations. In one example, alterations are made to the messages to allow the multiple cluster architecture to be transparent to various local nodes. It should be noted that write requests can be handled as well. In write requests, the targeted memory controller gathers responses and sends the responses to the processor when gathering is complete.

The cache coherence controller 641-1 associated with the remote cluster 640 receives a probe from cache coherence controller 621-2 and probes local nodes associated with cache blocks 645, 647, and 649. Similarly, the cache coherence controller 603-2 associated with the request cluster 600 receives a probe and forwards the probe to local nodes associated with cache blocks 605, 607, and 609 to probe the cache blocks in the request cluster 600. Processor 601-2 receives probe responses from the local nodes associated with cache blocks 605, 607, and 609.

According to various embodiments, cache coherence controller 621-3 accumulates probe responses and sends the probe responses to cache coherence controller 603-3, which in turn forwards the probe responses to the processor 601-3. Cache coherence controller 621-4 also sends a read response to cache coherence controller 603-4, which forwards the read response to processor 601-4. While probes and probe responses carry information for maintaining cache coherency in the system, read responses can carry actual fetched data. After receiving the fetched data, processor 601-4 may send a source done response to cache coherence controller 603-5. According to various embodiments, the transaction is now complete at the requesting cluster 600. Cache coherence controller 603-5 forwards the source done message to cache coherence controller 621-5. Cache coherence controller 621-5 in turn sends a source done message to memory controller 623-2. Upon receiving the source done message, the memory controller 623-2 can unlock the memory line and the transaction at the home cluster 620 is now complete. Another processor can now access the unlocked memory line.

It should be noted that because the cache coherence controller 621-3 waits for remote cluster probe responses before sending a probe response to cache coherence controller 603-3, delay is introduced into the system. According to various

embodiments, probe responses are gathered at cache coherence controller 603-3. By having remote clusters send probe responses through a home cluster, both home cluster probe responses and remote cluster probe responses can be delayed at the home cache coherence controller. In one example, remote cluster probe responses have to travel an additional hop in order to reach a request cluster. The latency for transmission of a probe response between a remote cluster and a request cluster may be substantially less than the latency for transmission of a probe response between a remote cluster and a request cluster through a home cluster. Home cluster probe responses are also delayed as a result of this added hop.

As will be appreciated by one of skill in the art, the specific transaction sequences involving requests, probes, and response messages can vary depending on the specific implementation. In one example, a cache coherence controller 621-3 may wait to receive a read response message from a memory controller 623-1 before transmitting both a probe response message and a read response message to a cache coherence controller 603-3. In other examples, a cache coherence controller may be the actual processor generating the request. Some processors may operate as both a processor and as a cache coherence controller. Furthermore, various data access request messages, probes, and responses associated with reads and writes are contemplated. As noted above, any message for snooping a cache can be referred to as a probe. Similarly, any message for indicating to the memory controller that a memory line should be unlocked can be referred to as a source done message.

It should be noted that the transactions shown in Figure 6 show examples of cache coherence controllers performing many different functions, including functions of remote processors, aggregate local caches, probing agent pairs, and remote memory as described with reference to Figures 5A-5D.

The cache coherence controller 621-1 at the home cluster 620 is acting as a remote processor. When the cache coherence controller receives a request from a request cluster processor, the cache coherence controller is directed to act as the requesting processor on behalf of the request cluster processor. In this case, the cache coherence controller 621-1 accepts a forwarded request from processor 601-1 and sends

it to the memory controller 623-1, accumulates responses from all local nodes and the memory controller 623-1, and forwards the accumulated responses and data back to the requesting processor 601-3. The cache coherence controller 621-5 also forwards a source done to the local memory controller 623-2.

The cache coherence controller 603-1 at the request cluster 600 is acting as a remote memory. As remote memory, the cache coherence controller is designed to forward a request from a processor to a proper remote cluster and ensure that local nodes are probed. In this case, the cache coherence controller 603-1 forwards a probe to cache coherence controller 621-1 at a home cluster 620. Cache coherence controller 603-2 also probes local nodes 605, 607, and 609.

The cache coherence controller 641-1 at the request cluster 640 is acting as a probing agent pair. As noted above, when a cache coherence controller acting as a probing agent pair receives a probe from a remote cluster, the cache coherence controller accepts the probe and forwards it to all local nodes. The cache coherence controller accumulates the responses and sends a final response back to the request cluster. Here, the cache coherence controller 641-1 sends a probe to local nodes associated with cache blocks 645, 647, and 649, gathers probe responses and sends the probe responses to cache coherence controller 621-3 at home cluster 620. Similarly, cache coherence controller 603-2 also acts as a probing agent pair at a request cluster 600. The cache coherence controller 603-2 forwards probes to local nodes including local nodes associated with cache blocks 605, 607, and 609.

The cache coherence controller 621-2 and 621-3 is also acting as an aggregate remote cache. The cache coherence controller 621-2 is responsible for accepting the probe from the memory controller 623-1 and forwarding the probe to the other processor clusters 600 and 640. More specifically, the cache coherence controller 621-2 forwards the probe to cache coherence controller 603-2 corresponding to request cluster 600 and to cache coherence controller 641-1 corresponding to remote cluster 640. As noted above, using a multiple cluster architecture may introduce delay as well as other undesirable elements such as increased traffic and processing overhead.

Probes are transmitted to all clusters in the multiple cluster system even though not all clusters need to be probed. For example, if a memory line associated with a request is invalid or absent from cache, it may not be necessary to probe all of the caches associated with the various clusters. In a system without a coherence directory, it is typically necessary to snoop all clusters. However, by using a coherence directory, the number of transactions in the system can be reduced by probing only a subset of the clusters (or nodes) in a system in order to minimize traffic and processing overhead.

By using a coherence directory, global memory line state information (with respect to each cluster) can be maintained and accessed by a memory controller or a cache coherence controller in a particular cluster. According to various embodiments, the coherence directory tracks and manages the distribution of probes as well as the receipt of responses. If coherence directory information indicates that probing of a specific cluster is not required, the probe to the specific cluster can be eliminated. In one example, a coherence directory indicates that probing of requesting and remote clusters is not necessary. A cache coherence controller in a home cluster probes local nodes without forwarding probes to the request and remote clusters. The cache coherence controller in the home cluster then sends a response to the request cluster after probe responses are received. However, in typical multiple cluster systems, a requesting cluster expects a predetermined number of responses from the various probed clusters. In one example, if the multiple cluster system includes four clusters, a request cluster would expect probe responses associated with nodes in all four clusters.

According to various embodiments, the techniques of the present invention provide a completion bit associated with a probe response. The completion bit indicates to the requesting cluster that no other probe responses from other clusters should be expected. Any mechanisms for notifying a request cluster that no other probe responses should be expected from other clusters is referred to herein as a completion indicator. In one example, a completion indicator is a completion bit included in the response sent to a request cluster after local nodes are probed. In another example, a completion indicator is separate data transmitted to a request cluster. By using a coherence directory and a completion indicator, the number of transactions associated with probing various clusters can be reduced. For example,

with reference to Figure 6, probes to cache coherence controller 603-2 and cache coherence controller 641-1 can be eliminated. A single response with a completion indicator can be transmitted by cache coherence controller 621-4 to the request cluster 600.

Figure 7 is one example of a coherence directory that can be used to allow management and filtering of probes. Various coherence directories are available. In one example, a full directory provides an entry for every memory line in a system. In this example, the coherence directory is maintained at the memory controller and is accessible by a cache coherence controller. However, in a system with a large amount of system memory, a full directory may not be efficient or practical. According to various embodiments, a sparse directory is provided with a limited number of entries associated with a selected set of memory lines. In one example, the coherence directory 701 includes state information 713, dirty data owner information 715, and an occupancy vector 717 associated with the memory lines 711. In some embodiments, the memory line states are modified, owned, shared, and invalid.

In the invalid state, a memory line is not currently available in cache associated with any remote cluster. In the shared state, a memory line may be present in more than one cache, but the memory line has not been modified in any of these caches. When a memory line is in the shared state, an occupancy vector 717 can be checked to determine what caches share the relevant data. An occupancy vector 717 may be implemented as an N-bit string, where each bit represents the availability of the data in the cache of N clusters. Any mechanism for tracking what clusters hold a copy of the relevant memory line in cache is referred to herein as an occupancy vector. The memory line with address 741 is in the shared state, and the occupancy vector 717 indicates that clusters 1 and 3 each have a copy of the shared memory line in cache.

In the modified state, a memory line has been modified and the modified copy exists in cache associated with a particular cluster. When a memory line is modified, dirty data owner information field 715 can be checked to determine the owner of the dirty data. Any mechanism for indicating what cluster owns a modified copy of the memory line in cache is referred to herein as a dirty data owner information field. In

one example, the memory line associated with address 781 is modified, and the dirty data owner field 715 indicates that cluster 2 owns the memory line.

In the owned state, a dirty memory line is owned by a single cache but may be resident in multiple caches. In this case, the copy held in memory is stale. If the memory line is in the owned state, dirty data owner field 715 can be accessed to determine which cluster owns the dirty data. In one example, the memory line associated with address 761 is in the owned state and is owned by cluster 4. The occupancy vector 717 can also be checked to determine what other caches may have the relevant data. In this example, the occupancy vector 717 indicates that clusters 2, 3, and 4 each have a copy of the data associated with the memory line in cache.

Although the coherence directory 701 includes the four states of modified, owned, shared, and invalid, it should be noted that particular implementations may use a different set of states. In one example, a system may have the five states of modified, exclusive, owned, shared, and invalid. The techniques of the present invention can be used with a variety of different possible memory line states.

The coherence directory tracks the various transactions such as requests and responses in a multiple cluster system to determine when memory lines are added to the coherence directory, when memory lines are removed from the directory, and when information associated with each memory line is updated. By using the coherence directory, specific embodiments of the present invention recognize that the number of transactions such as probes can be reduced by managing or filtering probes that do not need to be sent to specific clusters. In addition, some embodiments employ this notion to manage or filter probes within a single cluster.

Figure 8 is a diagrammatic representation showing probe filter information that can be used to reduce the number of transactions in a multiple or single cluster system. Any criterion that can be used to reduce the number of clusters or nodes probed is referred to herein as probe filter information. Transactions such as probes can have a variety of characteristics. Characteristics of the probe include the next state of the memory line associated with the probe which indicates the type of the associated

request for instance whether the probe is a read block (read) 823 or a read block modify (read/write) 825. According to various embodiments, a coherence directory maintains information for memory lines in the local cluster that are cached in non-local clusters, where non-local clusters can include request and remote clusters. According to other embodiments, such a directory includes information about locally cached lines.

If the state of the memory line associated with a probe is invalid 831 as indicated in the coherence directory, no copies of the memory line reside in other clusters (or other nodes for single cluster embodiments). Consequently, only the home cluster needs to be probed and a completion bit can be used to indicate to a request cluster that the request cluster should expect only a single response from home cluster instead of a response from each of the clusters. If the memory line associated with the probe is in the shared state 833, and the transaction is a read transaction, only the home cluster needs to be probed and a completion bit can again be used to indicate to the request cluster that only a single response from home cluster should be expected (803).

For read transactions on owned memory lines, only the remote cluster with the line cached in the owned state needs to be probed. The remote cluster can transmit the response with a completion bit back to a request cluster. For transactions on modified memory lines, the probe can be sent to the remote cluster with the line cached in the modified state. Although transactions such as read block (read) and read block modify (read/write) are described, it should be noted that other transactions such as test and test and set are contemplated.

Figure 9 is a diagrammatic representation depicting one example of transactions for probing only a home cluster as indicated in entries 801, 809, and 803 in Figure 8. According to various embodiments, processor 901-1 in a local cluster 900 sends a data access request such as a read request to a cache coherence controller 903-1. The cache coherence controller 903-1 forwards the request to a cache coherence controller 921-1 in a home cluster 920. The cache coherence controller 921-1 at the home cluster 920 receives the access request and forwards the access request to a memory controller 923-1, which then probes local nodes 925, 927, and cache coherence controller 921-2. It should be noted that a cache coherence controller 921-1 is typically responsible for

updating the coherence directory during various transactions. The cache coherence controller 921-2 determines characteristics associated with the probe from the memory controller 923-1 to determine whether remote probes are needed and whether a completion bit can be used. Here, the cache coherence controller 921-2 determines that no remote probes are needed and does not forward probes to the remote cluster 940 or to request cluster 900.

After cache coherence controller 921-4 receives the probe responses from local nodes as well as the read response from the memory controller 923-1, the response message with a completion indicator is transmitted to the request cluster. With the completion indicator, the request cluster does not wait for additional responses from other clusters. The coherence controller 903-4 forwards the response with the completion bit set to CPU 901-4. After receiving the response with the completion bit set, the CPU does not wait for additional responses from the local caches. CPU 901-4 forwards a source done message to cache coherence controller 903-5 to home cluster cache coherence controller 921-5, which can then perform updates of its coherence directory. The source done is then forwarded to memory controller 923-1.

Figure 9 shows one example of a sequence where only the home cluster needs to be probed. Figure 10 shows one example of a sequence where only a single remote cluster needs to be probed. Figure 10 is a diagrammatic representation depicting an example of transactions for probing a remote cluster as indicated in entries 805, 807, and 815 in Figure 8. According to various embodiments, processor 1001-1 in a local cluster 1000 sends a data access request such as a read request to a cache coherence controller 1003-1. The cache coherence controller 1003-1 forwards the request to a cache coherence controller 1021-1 in a home cluster 1020. The cache coherence controller 1021-1 at the home cluster 1020 receives the access request and forwards the access request to a memory controller 1023-1, which then probes local nodes 1025, 1027, and cache coherence controller 1021-2. The cache coherence controller 1021-2 determines characteristics associated with the probe from the memory controller 1023-1 to determine whether remote probes are needed and whether a completion bit can be used. Here, the cache coherence controller 1021-2 determines that only a remote cluster needs to be probed and does not forward a probe to request cluster 1000.

After cache coherence controller 1021-4 receives the probes from local nodes as well as the read response from the memory controller 1023-1, a response message is not transmitted to the request cluster because the remote cluster is sending a response message with a completion indicator is transmitted to the request cluster. With the completion indicator, the request cluster does not wait for additional responses from other clusters. The response is forwarded to CPU 1001-4 and a source done message is sent from cache coherence controller 1003-5 to home cluster cache coherence controller 1021-5. With the completion bit set in the response to CPU 1001-4, it does not wait for any other local responses. After all responses from local nodes are received, the source done is then forwarded to memory controller 1023-1, which can then perform updates of its coherence directory.

Figure 11 is a process flow diagram showing one example of a technique for handling requests at a home cache coherence controller. At 1101, a request associated with a memory line is received. At 1105, the cache coherence controller forwards the request to the memory controller. At 1109, the cache coherence controller receives a probe from the memory controller and accesses a coherence directory and probe filter information at 1113 to determine whether the number of probes to various clusters in the system can be reduced. At 1121, it is determined whether filtering and a completion indicator can be used. In one example, it is determined the filtering and a completion indicator can be used by identifying the criteria specified in Figure 8 and by accessing a coherence directory as shown in Figure 7.

If a completion indicator cannot be used, probes are broadcast to the various nodes with no filtering and no completion bit 1145. If filtering and a completion indicator can be used, it is determined at 1131 if a remote cluster should be probed. If a single remote cluster is the cluster that should be probed, the probe is forwarded with the completion indicator to the remote cluster at 1135. At 1139, home cluster probe responses are received but are not forwarded to the request cluster. The response is not sent to the request cluster from home cluster because a remote cluster is sending a response with a completion indicator to the request cluster.

At 1149, source done information is received from the request cluster and forwarded to the memory controller. If it is determined at 1131 that only the home cluster needs to be probed, then the cache coherence controller at 1141 does not send probes to any request or remote clusters and instead sends a response to the request cluster with a completion indicator. The cache coherence controller sends the response with the completion indicator after receiving home cluster probe responses. At 1149, the cache coherence controller at the home cluster receives source done information from the request cluster and forwards the source done information to the memory controller.

According to various embodiments, when the only cluster that needs to be probed is the home cluster, only the nodes in the home cluster are probed. No probes are transmitted to any request or remote cluster. However, when the only cluster that needs to be probed is a remote or request cluster, not only are the nodes in the remote cluster probed, but the nodes in the home cluster are probed as well. As will be seen, in some embodiments, the nodes within a home cluster may be filtered using probe filter information corresponding to locally cached lines.

According to various embodiments, the techniques of the present invention provide that when only a remote or request cluster needs to be probed, the memory controller can sometimes be bypassed to allow probing of only the remote or request cluster. In one example, a probe is not forwarded within the home cluster and a probe is forwarded directly to the remote cluster from the home cluster cache coherence controller.

Figure 12 is a diagrammatic representation showing exemplary memory controller filter information. Any criterion used to reduce the number of requests forwarded to a memory controller is referred to herein as memory controller filter information. Characteristics of a request can again be analyzed when a cache coherence controller receives the request from a request cluster. Requests can have a variety of characteristics. Some characteristics include whether the request is a read block (read) 1223 or a read block modify (read/write) 1225. When the state of the memory line associated with the request is invalid 1231, no remote probes are required

because no remote clusters have a copy of the memory line in cache. In some embodiments, the cache coherence controller does not maintain knowledge of the home cluster cache state. In such cases, the request is forwarded to the memory controller. In other embodiments, the cache coherence controller does maintain such information and uses it to reduce the number of nodes probed within the home cluster.

For read block transactions on a shared memory line 1203, there is no need to probe the remote clusters as the home cluster contains a valid copy of the memory line in either cache or the memory controller. Consequently the request is forwarded to the memory controller. For read block modify transactions on shared memory lines 1211, the local node state is unknown and the request is sent to the memory controller.

For read block transactions on an owned memory line 1205, there is no need to send a request to the target or probe local nodes as the owned state implies that the home cluster caches are invalid or shared. A probe is forwarded directly to the owning cluster to acquire the cached data. For read block write transactions on an owned memory line 1213, the local state is unknown and consequently the request is forwarded to the memory controller. When the state of the memory line associated with the request is modified 1237, there is no need to probe local nodes, as a modified state implies the home cluster state is invalid. A probe is forwarded to the cluster owning the memory line.

Figure 13 shows one example of a sequence where a request does not need to be forwarded to the home cluster memory controller. According to various embodiments, processor 1301-1 in a local cluster 1300 sends a data access request such as a read request to a cache coherence controller 1303-1. The cache coherence controller 1303-1 forwards the request to a cache coherence controller 1321-1 in a home cluster 1320. The cache coherence controller 1321-1 at the home cluster 1320 receives the access request and determines whether the memory controller can be bypassed. Forwarding a probe to a remote or request cluster without forwarding the request to a memory controller is referred to herein as bypassing the memory controller. In one embodiment, the determination can be made by using memory controller filter information. If the probe characteristics fall within entries 1205, 1207, or 1215, the

memory controller is bypassed and a probe is sent to cache coherence controller 1341-1 in the remote cluster 1340. In one example, the probe is forwarded with an indication that a completion bit should be used.

The cache coherence controller 1321-1 in the home cluster 1320 is acting as a serialization point in place of the memory controller to maintain cache coherency. Once it is determined that the memory controller can be bypassed, the cache coherence controller 1321-1 blocks all other incoming requests and outgoing probes until a final source done is received from the request cluster. The remote cluster cache coherence controller 1341-1 probes remote cluster nodes and sends a response with a completion indicator to the request cluster 1300. The response is forwarded to CPU 1301-4 and a source done message is sent from cache coherence controller 1303-5 to home cluster cache coherence controller 1321-5. The source done is not forwarded to the memory controller, because the memory controller never processed the transaction.

Figure 14 is a flow process diagram showing request handling at a home cache coherence controller using memory controller filter information. At 1401, a request associated with a particular memory line is received. At 1403, characteristics associated with the request are identified. At 1411, it is determined if the memory controller can be bypassed. According to various embodiments, memory controller filter information shown in Figure 12 is used to determine whether a memory controller can be bypassed. If it is determined that a memory controller can be bypassed, requests associated with the same memory line are blocked at 1415 and a probe is sent to a remote or a request cluster. At 1417, the memory line is unblocked after receiving a source done from the request cluster. If it is determined at 1411 that a memory controller can not be bypassed, the request is forwarded to a serialization point 1405. The transaction sequence can then proceed with or without probe filtering and a completion indicator as shown in 1109 of Figure 11.

As described above and according to some embodiments, a cache coherence directory is a mechanism associated with each cache coherence controller which facilitates the tracking by that cache coherence controller of where particular memory lines within its cluster's memory are being cached in remote clusters. That is, a portion

of the global memory space for the multi-cluster system is associated with each cluster. The cache coherence directory enables the cache coherence controller in each cluster to track which memory lines from the portion of the global memory space associated with its cluster have been cached with processors in remote clusters.

Each cache coherence controller in each cluster has such a cache coherence directory associated with it. Given the size of the memory space associated with each cluster, it is not practical to have an entry in the coherence directory for each memory line. Rather, the directory is sized in relation to the amount of cache memory associated with the processors in all remote clusters, a much smaller amount of memory. That is, the coherence directory is an associative memory which associates the memory line addresses with their remote cache locations. According to one embodiment, the cache coherence directory is fully associative. According to another embodiment, the directory is set-associative.

According to a specific embodiment, a typical entry in the cache coherence directory includes the memory address corresponding to the cached memory line, the remote cache location, whether the line is "clean" or "dirty," and whether the associated processor has read-only access or read/write access. This information corresponds to the standard coherence protocol states which include "invalid" (not cached in any remote clusters), "shared" (cached as "clean" and read-only), "modified" (cached as "dirty" and read/write), and "owned" (cached as "dirty" but read-only). A coherence directory entry also includes one or more fields identifying which, if any, of the remote clusters have the line cached in the "dirty" state, and which other clusters have the line cached in the "shared" state.

When the cache coherence controller in a particular cluster, e.g., the home cluster, receives a request for a particular memory line in its memory, it transmits the request to a memory controller associated with one of the local nodes to which the requested address maps, e.g., the home controller. To determine whether the most recently modified copy of the memory line resides in any of the cache memories in the system, the home controller then generates probes to all of the nodes in the cluster (including the cache coherence controller) asking whether any of the nodes have the

requested memory line stored in their corresponding caches in either a "dirty" (i.e., modified) or "clean" (unmodified) state. These probes can tell the nodes to invalidate their copies of the memory line, as well as to return the memory line in the case where the memory line has been modified.

Because the cache coherence controller in each cluster maps to the remainder of the global memory space outside of its cluster, it is responsible for ensuring that the appropriate processors in remote clusters receive corresponding probes. This is where the cache coherence directory comes into play. Without such a mechanism, the cache coherence controller would have to transmit probes to all of the nodes in all of the remote clusters having cache memories associated with them. By contrast, because the cache coherence directory provides information about where memory lines are cached as well as their states, probes only need be directed toward the clusters in which the requested memory line is cached. The state of a particular cached line will determine what type of probe is generated. As will be seen, such a cache coherence controller may also be configured to include information about locally cached memory lines and be operable to use such information to reduce the number of probes within its cluster.

The associative nature of the cache coherence directory of the present invention necessitates an eviction mechanism so that the most relevant information may be maintained in the limited number of directory entries. In addition, the distributed, multi-cluster architecture described herein also requires that the eviction mechanism be able to guarantee that the memory line corresponding to an evicted directory entry is purged from all remote caches. As mentioned above, the directory entry field indicating the location(s) of the memory line helps to reduce the number of transactions required to effect this purging. In addition, the appropriate type of request to effect the purging depends on the state of the remotely cached memory lines.

Thus, if a directory entry to be purged indicates that the line is only cached in the "clean" state, what is required is a mechanism which invalidates the memory line in each of the remote caches in which the line is cached. On the other hand, if the directory entry indicates that the line is in the "dirty" state in any of the remote caches,

the modified memory line to memory must first be written back to memory before the line is invalidated.

In a conventional multiprocessor system, i.e., a system which does not have remote clusters of processors, there typically are not mechanisms by which external requests to a particular processor may be generated for the purpose of instructing the processor how to manage its cache. That is, in such a system, each processor is responsible for maintaining its own cache and evicting and/or writing lines back to memory to free up room for new entries. Thus, there is no provision for allowing one processor to instruct another processor to write a particular line back to memory. Similarly, there is no provision for allowing one processor to instruct another processor to invalidate a particular line in its cache without returning any data. That is, transactions between processor in a cache coherence protocol typically assume that one processor is trying to get a copy of the line from the other. Therefore, according to the present invention, mechanisms are provided for a system having a plurality of multiprocessor clusters by which such requests may be generated.

According to various specific embodiments of the invention, the semantics of transaction types developed for a single cluster system are altered to enable external devices to generate requests to specific processors to invalidate cache entries and to write cache entries back to memory. According to one embodiment which assumes the multi-cluster architecture described above, one such transaction type referred to herein as a "sized write" (i.e., a partial line write to memory) is employed to achieve the effect of instructing a processor having a "dirty" copy of a memory line stored in its cache to write the line back to memory.

The sized write transaction normally allows a processor to initiate a write to a any arbitrarily sized portion of a memory line (e.g., a particular byte or the entire line). That is, a request to write the byte to the memory line is sent to the memory controller which maps to the memory line. The memory controller then sends out a request to any other caches in the system having the corresponding line in the "dirty" state. If a positive response is received, i.e., if a modified copy of the line is returned in response

to the request, the memory controller than merges the original byte with the retrieved memory line, and then writes the merged line back to memory.

Generally speaking, the eviction of a cache coherence directory entry corresponding to a "dirty" line in a remote cache requires that the remote cache write the line back to memory and invalidate its copy. Thus, a transaction is needed which results in the following actions:

1. A write back is generated for the cached memory line,
2. The copy of the line in the cache is invalidated, and
3. The eviction mechanism is notified when the memory line has been written back to memory.

According to a specific embodiment of the invention, the semantics of the sized write transaction are altered resulting in a transaction having these characteristics. The altered sized write is generated such that no data are provided for the partial write, i.e., the sized write request has zero size. When the cache coherence directory associated with the cache coherence controller in a particular cluster, i.e., the home cluster, determines that it needs to evict an entry which corresponds to remotely cached "dirty" memory line, it generates a sized write request specifying no data and directs the request to the local memory controller corresponding to the memory line, i.e., the home memory controller. The home memory controller then generates probes to all of the local nodes in the cluster (including the cache coherence controller) requesting the most recent copy of the memory line. The local nodes respond as described above, returning any dirty copy of the line and invalidating the corresponding entries in their caches.

As described above, the cache coherence controller forwards the probe to the appropriate remote cluster(s) based on the information in its associated cache coherence directory which indicates the existence and location of any remotely cached copies of the memory line. The nodes in remote clusters which receive the probe behave similarly to the local nodes in that they respond by returning any dirty copy of the line and invalidating the corresponding entries in their caches.

The home memory controller receives the "dirty" copy of the memory line (if one exists), performs a NOP (because there are no data to merge with the modified line), writes the line back to memory, and notifies the cache coherence directory (i.e., the originator of the transaction) that the transaction is complete. In this way, the "altered" sized write transaction is employed to achieve the effect of instructing a remote processor to write back a specific "dirty" line in its cache to memory.

According to a specific embodiment of the invention, the notification by the home memory controller that the transaction is complete plays an important part in avoiding race conditions. That is, because the coherence directory is in flux during the period of time required to complete an eviction, it is possible that subsequent transactions corresponding to the same memory line might be generated somewhere in the system. Fortunately, as described above, the memory controllers of the multi-cluster architecture described herein act as serialization points for memory transactions. That is, once a memory controller accepts a transaction for one of its memory lines, it blocks all other transaction to that same memory line. Therefore, once the home memory controller accepts the sized write transaction, it does not allow any further transactions for the same memory line until the eviction process is completed.

Generally speaking, the eviction of a cache coherence directory entry corresponding to a "clean" line in a remote cache requires that the remote cache invalidate its copy. Thus, a transaction is needed which results in the following actions:

1. The copy of the line in the cache is invalidated, and
2. The eviction mechanism is notified when the invalidation is complete.

According to some embodiments, the zero sized write described above is employed as described with reference to dirty lines. According to another embodiment of the invention, the semantics for another type of transaction referred to herein as a "validate block" transaction are altered to achieve these results. That is, the semantics of the validate block transaction are altered such that it has the effect of instructing remote systems nodes having "clean" copies of a memory line to invalidate those lines

in their caches without resulting in any returned copies of the line in response to the request.

The validate block transaction is normally intended for the case in which a processor or I/O device (via the I/O bridge) writes an entire memory line of data atomically. This might occur, for example, when an I/O device, such as a disk drive, is writing blocks of data to memory. Such a transaction does not require a data response from the memory controller responsible for the memory line. In such a case, however, there still is a need to invalidate all cached copies of the line. The transaction saves the bandwidth that would normally be consumed to send the line from the memory controller to the processor or I/O bridge, which would be completely overwritten.

Therefore, according to a specific embodiment of the invention, when the cache coherence directory associated with the cache coherence controller in a particular cluster, i.e., the home cluster, determines that it needs to evict an entry which corresponds to one or more remotely cached "clean" memory lines, it generates a validate block request and directs the request to the local memory controller corresponding to the memory line, i.e., the home memory controller. The home memory controller then generates invalidating probes to all of the local nodes in the cluster (including the cache coherence controller). The local nodes invalidate their copies of the memory line and send confirming responses to home memory controller indicating that the invalidation took place.

The cache coherence controller forwards the invalidating probe to the appropriate remote cluster(s) based on the information in its associated cache coherence directory which indicates the existence and location of any remotely cached copies of the memory line. The remote nodes behave similarly to the local nodes in that they also invalidate any copies of the memory line and send the corresponding responses back to the cache coherence controller in the home cluster. The cache coherence controller aggregates the responses and transmits the aggregated response to the home memory controller.

The home memory controller receives the responses from the local nodes and the cache coherence controller, and notifies the cache coherence directory (i.e., the originator of the transaction) that the transaction is complete. The cache coherence directory then transmits a "source done" to the memory controller in response to which the memory line is freed up for subsequent transactions. In this way, the validate block transaction is employed to achieve the effect of instructing a remote processor to invalidate its copy of a "clean" memory line. As with the altered sized write transaction, the home memory controller acts as a serialization point for the validate block transaction thereby avoiding race conditions caused by subsequent transactions corresponding to the same memory line.

As described above, the eviction mechanism employed to effect an eviction of an entry from the cache coherence directory may depend on the indicated state of the corresponding memory line, e.g., "clean" vs. "dirty." According to specific embodiments of the invention, the determination of which of the existing entries is to be evicted to make room for a new entry may be done in a wide variety of ways. For example, different approaches might select the oldest or least frequently used entries. According to one embodiment, "modified" lines are chosen ahead of "shared" lines, with a random mechanism being employed to select among like copies. It will be understood that any kind of policy for selecting the entry to be evicted may be employed without departing from the scope of the invention.

As described above, the serialization point of the home memory controller guarantees that transactions to the memory line corresponding to the directory entry being evicted will be locked out once the home memory controller receives the sized write or validate block request from the directory. However, it is possible that conflicting transactions may be generated during the time between when the cache coherence directory to evict a particular entry and the corresponding request is received by the memory controller. Until the sized write or validate block request corresponding to the entry being evicted is received by the memory controller, it is desirable to guarantee that any other requests corresponding to the same memory line are properly serviced.

Therefore, according to a specific embodiment of the invention, an eviction buffer is provided in the cache coherence directory in which the directory places the entry it has determined should be evicted. The entry in the eviction buffer remains visible to the cache coherence controller as one of the entries in the directory, i.e., the cache coherence controller cannot distinguish between entries in the directory and entries in the eviction buffer. The entry in the eviction buffer remains there until the home memory controller receives the corresponding eviction request from the cache coherence directory and the cache coherence controller receives a probe corresponding to the eviction request, at which point the entry in the eviction buffer is invalidated. However, if an intervening request corresponding to the entry in the eviction buffer is received, it may be processed by the cache coherence controller with reference to the eviction buffer entry and, because of the ordering of transactions at the memory controller serialization point, it is guaranteed that this intervening transaction will complete before the eviction request is serviced by the memory controller. In this way, a cache coherence directory entry may be "earmarked" for eviction, but may still be used for servicing subsequent requests until the memory line is locked by the home memory controller for the eviction process. According to a specific embodiment, if the eviction buffer is full, a status bit instructs the cache coherence controller to stall, i.e., to queue up any new requests for which there are no corresponding entries already in the cache coherence directory.

Figure 15 is a diagrammatic representation showing a transaction flow for a cache coherence directory eviction of a directory entry corresponding to a "dirty" memory line according to a specific embodiment of the invention. When the cache coherence directory 1501-1 determines that an eviction of one of its entries showing a "dirty" state must occur, e.g., in response to a new request for which no entry exists, it places the entry to be evicted into its eviction buffer and generates a sized write request (having zero size) to the local memory controller responsible for the memory line corresponding to the directory entry being evicted, i.e., the home memory controller 1502-1.

Assuming a previous transaction corresponding to the same memory line is not currently being processed, the home memory controller 1502-1 accepts the sized write

request and generates invalidating probes to all nodes in its cluster including local nodes 1503-1505 and cache coherence controller 1506-1. Each of the local nodes 1503-1505 invalidates any copies of the memory line and responds accordingly to the home memory controller 1502-2. When the cache coherence controller 1506-1 in the home cluster receives the invalidating probe, it forwards the invalidating probe to the remote cluster having the dirty copy of the memory line according to the directory information (i.e., the entry in the eviction buffer). The directory entry in the eviction buffer is then invalidated.

The cache coherence controller 1507-1 in the remote cluster receives the invalidating probe and forwards it to the local nodes in the remote cluster, i.e., local nodes 1508-1510. The local node having the "dirty" copy of the memory line replies to cache coherence controller 1507-2 with a dirty data response (i.e., returning the modified copy of the memory line from its cache), and the other local nodes reply with clean responses. In addition, any copies of the memory line in the remote cluster's caches are invalidated. The cache coherence controller 1507-2 then forwards the dirty data response back to the cache coherence controller 1506-2 in the home cluster which forwards the response to the home memory controller 1502-3.

The home memory controller 1502-3 receives the dirty data response and merges the modified data with the data from the sized write request (i.e., no data). Once all responses from the local nodes are received by the home memory controller 1502-3, a target done (TD) message is sent by the home memory controller 1502-3 to the cache coherence directory 1501-2 which completes the transaction with a source done (SD) message back to the home memory controller 1502-4, which then unlocks the memory line for subsequent transactions. As mentioned above, this mechanism may also be employed to evict directory entries corresponding to "clean" memory lines.

Figure 16 is a diagrammatic representation showing a transaction flow for an eviction of a directory entry corresponding to a "clean" memory line according to another specific embodiment of the invention. When the cache coherence directory 1601-1 determines that an eviction of one of its entries showing a "clean" state must occur it places the entry to be evicted into its eviction buffer and generates a validate

block request for the corresponding memory line and sends the request to the local memory controller responsible for the memory line, i.e., the home memory controller 1602-1.

Assuming the memory line is not locked, the home memory controller 1602-1 accepts the validate block request and generates invalidating probes to all nodes in its cluster including local nodes 1603-1605 and cache coherence controller 1606-1. Each of the local nodes 1603-1605 invalidates any copies of the memory line and responds accordingly to the home memory controller 1602-2. When the cache coherence controller 1606-1 in the home cluster receives the invalidating probe, it forwards the invalidating probe to any remote clusters having a copy of the memory line according to the directory information (i.e., the entry in the eviction buffer). The directory entry in the eviction buffer is then invalidated.

The cache coherence controller 1607-1 in any such remote cluster receives the invalidating probe and forwards it to the local nodes in the remote cluster, i.e., local nodes 1608-1610. Each of the local nodes 1608-1610 having a copy of the line invalidates its copy and responds accordingly to the cache coherence controller 1607-2. The cache coherence controller 1607-2 aggregates and forwards these responses back to the cache coherence controller 1606-2 in the home cluster which sends a source done (SD) message to the home memory controller 1602-3, which then unlocks the memory line for subsequent transactions.

In general, the entry in the eviction buffer may be invalidated by an earlier request, such as a write by a local processor. When the invalidating probe, associated with the eviction request, reaches the coherence controller, it will find the directory entry in the eviction buffer invalid. In this case, the coherence controller responds to the request without generating any remote probes.

The foregoing description assumes that the cache coherence directory includes processing functionality, e.g., an eviction manager, which may, according to different embodiments of the invention, be implemented in a variety of ways. For example, the directory may include its own memory controller configured to manage the directory

and implement the various functionalities described above. Alternatively, these functionalities may reside in application specific hardware, e.g., an ASIC, as a separate eviction manager. A further alternative might configure the cache coherence controller to incorporate at least some of the functionalities described.

According to a specific embodiment illustrated in Figure 17, the eviction manager 1702 is part of the cache coherence directory 1701 which is a functional block within the cache coherence controller 1700. The protocol engine 1705 (which may actually be one or more protocol engines) is responsible for processing transactions and corresponds to the CCC blocks in Figures 15 and 16. The cache coherence directory corresponds to the DIR blocks in Figures 15 and 16. The remaining blocks within controller 1700 are similar to the corresponding blocks described above with reference to Figure 3. Eviction manager 1702 communicates with protocol engine 1705 via coherent interface 1707. The protocol engine 1705 communicates with the coherence directory via a dedicated interface, which is used to communicate lookup and update commands and responses.

The basic architecture of Figure 17 may also be used to implement a probe filtering unit which is operable to reduce probe traffic within a cluster of processing nodes. Various embodiments of such a probe filtering unit are described below with reference to Figures 18-22.

As described above with reference to Figures 12-14, embodiments of the invention are contemplated in which the memory controller in the home cluster may be bypassed with reference to characteristics of a received request in accordance with, for example, the memory controller information described with reference to Figure 12. According to such embodiments, if the request is forwarded to the memory controller in the home cluster, all of the local nodes in the home cluster are then probed as shown in and described above with reference to Figure 4. On the other hand, if the request is not forwarded to the memory controller in the home cluster, none of the local nodes are probed.

As will be understood, such embodiments are effective in reducing unnecessary probe traffic in the former case, but may still generate unnecessary probes in the latter. That is, for example, in cases where the memory controller filter information of Figure 12 indicates that a valid copy of the requested memory line may exist in the home cluster, all of the local nodes in the home cluster end up being probed whether or not they have valid copies of the line in their caches. It is therefore desirable to provide techniques by which probe traffic may be more precisely "filtered" and system performance may be further enhanced. It will be understood that any reference herein to "filtering" includes any mechanism or technique by which the number of recipients of a probe is reduced.

According to specific embodiments of the invention, the techniques described above are adapted to reduce the number of probes within a cluster. Such techniques are referred to herein as local probe filtering. It should be noted that the following discussion applies both to systems having multiple multi-processor clusters such as those described above, as well as to systems having multiple processing nodes configured in a single cluster.

The behavior of a single cluster of processors implemented without local probe filtering will now be described again with reference to Figure 4. CPU 401-1 sends a read request to memory controller MC 403-1 which is responsible for controlling access to the memory range including the line identified in the request. If the memory controller MC 403-1 is available to respond to the request, it generates probes to the other processing nodes in the system (405, 407 and 409), each of which sends a probe response back to the requesting CPU 401-2. These probe responses may or may not include copies of the requested memory line depending on whether a valid copy of the line existed in the caches associated with these nodes. To account for the case in which the memory line does not exist in any of the caches, MC 403-1 also generates a read response back to the requesting CPU 401-3 which includes the memory line retrieved from main memory.

In implementations without local probe filtering, CPU 401 is programmed to expect responses from each of the nodes probed (including its own node) as well as a

response from memory controller MC 403. It will only send the "source done" message to the memory controller (which then unlocks the memory line) when all of the expected messages have been received. Thus, where the requested memory line is not held by a particular node's cache, there is unnecessary probe related traffic consuming the precious bandwidth of the system's point-to-point infrastructure.

It will be understood that the foregoing is an exemplary read transaction in which the probe responses and read responses are directed to the requesting processor. It should also be understood that the present invention is applicable to operations in which the responses are directed to the memory controller, e.g., write operations. The former probe responses are precipitated by what is called a probe source; the latter by a probe target. Probes also include "next state" information which indicates to each node what the state of its copy of the line should be at the end of the transaction. According to a specific embodiment, the next state information indicates one of three possibilities, i.e., that there should be no change to the line status, that it should be moved to "shared," or moved to "invalid." In general, for the typical memory transaction depicted in Figure 4, each of the nodes in the cluster is "consulted" and makes its own independent assessment of how to proceed based on its current condition.

As mentioned above, the filtering of probes within a cluster, i.e., local probe filtering, may be implemented in systems having multiple clusters as well as systems having a single cluster of processors. In the former and as described above, the probe filtering functionalities described herein may be implemented in a cache coherence controller which facilitates communication between clusters. In the latter, these functionalities may be implemented in a device which will be referred to herein as a probe filtering unit (PFU) which may occupy a similar location in the cluster as the cache coherence controller, and may include some subset of the other functionalities of the cache coherence controller. In either case, it should be noted that the functionalities described may be implemented in a single device, e.g., a cache coherence controller or probe filtering unit, or be distributed among multiple devices including, for example, the processing nodes themselves. It should be understood that the use of the term "probe filtering unit" or "PFU" in the following discussion is not intended to be limiting or exclusive. Rather, any device or object operable to perform the described

functionalities, e.g., a cache coherency controller as described herein, is within the scope of the invention.

Figure 18 is a diagrammatic representation of a multiple processor system 1800 in which embodiments of the invention relating to the filtering of probes within a single cluster of processors may be practiced. System 1800 may comprise one cluster in a multiprocessor system (as described above with reference to Figure 2) or the entirety of a single cluster system. System 1800 includes processing nodes 1802a-1802d, one or more Basic I/O systems (BIOS) 1804, a memory subsystem comprising memory banks 1806a-1806d, and point-to-point communication links 1808a-1808e. The point-to-point communication links are configured to allow interconnections between processing nodes 1802a-1802d, I/O switch 1810, and probe filtering unit 1830 according to a point-to-point communication protocol.

According to embodiments having multiple clusters of processors, PFU 1830 may comprise a cache coherence controller which facilitates communication with remote clusters as described above. According to one embodiment, PFU 1830 is an Application Specific Integrated Circuit (ASIC) supporting the local point-to-point coherence protocol. PFU 1830 can also be configured to handle a non-coherent protocol to allow communication with I/O devices. In one embodiment, PFU 1830 is a specially configured programmable chip such as a programmable logic device or a field programmable gate array. An exemplary architecture for PFU 1830 may be implemented as described above with reference to Fig. 17. I/O switch 1810 connects the rest of the system to I/O adapters 1816 and 1820. As mentioned above with reference to Figure 2, it should be understood that a node (e.g., processing nodes 1802a-1802d) may comprise multiple sub-units, e.g., CPUs, memory controllers, I/O bridges, etc.

According to various embodiments of the invention, processing nodes 1802a-1802d are substantially identical. Figure 19 is a simplified block diagram of such a processing node 1802 which includes an interface 1902 having a plurality of ports 1904a-1904c and routing tables 1906a-1906c associated therewith. Each port 1904

allows communication with other resources, e.g., processors or I/O devices, in the computer system via associated links, e.g., links 1808a-1808e of Figure 18.

The infrastructure shown in Figure 19 can be generalized as a point-to-point, distributed routing mechanism which comprises a plurality of segments interconnecting the systems processors according to any of a variety of topologies, e.g., ring, mesh, etc. Each of the endpoints of each of the segments is associated with a connected processing node which has a unique node ID and a plurality of associated resources which it "owns," e.g., the memory and I/O to which it's connected.

The routing tables associated with each of the nodes in the distributed routing mechanism collectively represent the current state of interconnection among the computer system resources. According to a specific embodiment, each node has different routing tables for requests, broadcasts (e.g., probes), and responses. Each of the resources (e.g., a specific memory range or I/O device) owned by any given node (e.g., processor) is represented in the routing table(s) associated with the node as an address. When a request arrives at a node, the requested address is compared to a two level entry in the node's routing table identifying the appropriate node and link, i.e., given a particular address within a range of addresses, go to node x; and for node x use link y.

As shown in Figure 19, processing node 1802 can conduct point-to-point communication with three other processing nodes according to the information in the associated routing tables. According to a specific embodiment, routing tables 1906a-1906c comprise two-level tables, a first level associating the unique addresses of system resources (e.g., a memory bank) with a corresponding node (e.g., one of the processors), and a second level associating each node with the link (e.g., 1808a-1808e) to be used to reach the node from the current node.

Processing node 1802 also has a set of JTAG handshake registers 1908 which, among other things, may be used to facilitate modification of the routing tables (which are initially set by the BIOS). That is, routing table entries can be written to handshake registers 1908 for eventual storage in routing tables 1906a-1906c. It should be

understood that the processor architecture depicted in Figure 19 is merely exemplary for the purpose of describing a specific embodiment of the present invention. For example, a fewer or greater number of ports and/or routing tables may be used to implement other embodiments of the invention.

According to a specific embodiment, the processing nodes in a single cluster are programmed according to their normal setup rules with a few exceptions. First, the broadcast routing tables in each of the nodes are programmed such that the broadcasts initiated from each node go directly to the PFU rather than on all of the node interfaces. Second, the broadcast routing table in each node is programmed such that broadcasts originating from the PFU enter the node and are not forwarded to any other node. Third, each node is programmed to expect only one or two probe responses instead of one from each node in the system. More specifically, each node is programmed to expect one probe response if the PFU contains temporary storage to hold dirty data, and two if it does not. Some of the exemplary embodiments described below will assume the latter. However, this should not be construed as limiting the scope of the invention.

Referring now to Figure 20, when a memory controller generates a probe (2002), the node's routing table is consulted (2004) and the probe is sent only to the PFU (2006), and not to any of the nodes (including the node associated with the memory controller). The PFU accepts the probe and looks up the address in its directory of shared cache states (2008). According to a specific embodiment, the directory of shared states may be implemented as described above with reference to Figures 7 and 8, and indicates where particular memory lines are cached within the cluster. According to various embodiments, the directory may be full or sparse. And in embodiments where the directory is sparse, eviction mechanisms such as those described above with reference to the cache coherence controller may be employed.

If the directory lookup determines that the cache line is not cached anywhere in the system, i.e., ignoring the requesting node (2010), then the PFU responds to the probe with no traffic generated to any of the other nodes. That is, the response is sent back to the correct unit (either the CPU or the memory controller depending on the type of the probe) with an indication that there are no copies of the line in the system (2012).

If the node counts are programmed to expect two probe responses, then the PFU sends two copies of the response.

If, on the other hand, the directory lookup determines the cache line may be cached in the system (2010), the PFU sends out a probe only on links corresponding to the nodes that may contain the cache line (2014). The outgoing probe is the same as the incoming probe, except that it is modified to identify the PFU as the target, i.e., the source of the probe, and the command is changed such that it is always a "Probe – respond to target" regardless of the original command (either respond to source or respond to target).

The nodes that receive the modified probe automatically look up the cache line (2016) and return their response to the PFU (2018). The PFU uses these responses to update the directory (which may remove the responding node from the list of nodes that is caching the data) (2020). Once all the nodes to which the probe was sent have responded (2022), the PFU accumulates the responses as described above with reference to remote probe filtering (2024), and responds to the node from which the original request originated (2026).

As mentioned above, embodiments are contemplated in which the requesting node is programmed to expect two responses from the PFU. This relates to the fact that it may be desirable to immediately forward "dirty" data to the requesting node even where the PFU has not yet received all of the expected responses from the probed nodes. That is, if a probed node has the requested line "dirty" in its cache, i.e., it is the exclusive owner of the most recent copy of the line, that node sends back a read response with the requested data. If the PFU receives a read response from one of the probed nodes, but waits for all probe responses before sending a final response to the requesting node, deadlock may occur (i.e., if the PFU's buffers are full of dirty data, it won't be able to receive the incoming read responses).

Therefore, according to this embodiment, when the PFU receives a read response from one of the probed nodes, it immediately forwards the response to the requesting node. A final response which is cumulative of all received probe responses

is then sent to the requesting node to complete the transaction. In cases where the PFU does not receive a read response, i.e., none of the probed nodes own the line, two copies of the final probe response must be sent to the requesting node to complete the transaction, i.e., it is expecting two responses. Alternatively, embodiments are contemplated in which the PFU includes sufficient temporary storage for dirty data, and the requesting nodes are programmed to expect only one response. In either case, because the PFU centrally manages the probe traffic, cache coherency can be maintained without having all nodes respond to a requester.

Figure 21 illustrates an example of a memory request in a multi-processor system designed according to a specific embodiment of the invention. In this example, a four processing node system with a PFU or cache coherence controller (e.g., the system of Figure 18) is assumed. A CPU makes a memory request Req to the memory controller M to which the requested line corresponds. The memory controller retrieves the requested line from the memory banks (as indicated by read response RR), and generates a probe to the probe filtering unit PFU for any cached copies of the line. The PFU, in turn, probes nodes N0 and N2 after it applies its directory lookup and probe filtering algorithm. As discussed above, the determination as to which nodes get probed depends on the state of the PFU's directory and is independent of the source of the request, i.e., the requesting node may receive a probe. The PFU then accumulates the responses from nodes N0 and N2 and sends two responses (one of which may be a read response from N0 or N2) back to the requesting CPU. As mentioned above, some embodiments may only require a single response. The CPU then sends a source done to the memory controller to complete the transaction and unlock the memory line.

Figure 22 is an example of a memory request in which the PFU does not have to probe any nodes. This example illustrates the case in which the local filtering mechanism has its greatest effect. That is, because the PFU determines that none of the nodes in the system (i.e., N0-N3) has the requested line in its cache (i.e., a directory miss), no probes are needed, and the two probe responses PR are immediately sent back to the requesting CPU which then sends the source done (SD) to the memory controller to complete the transaction. Thus, the probe traffic between the requesting CPU and each of nodes N0-N3 which would have otherwise consumed bandwidth and clock

cycles is almost entirely eliminated, i.e., only one probe to the PFU and two probe responses back to the requester are required. As mentioned above, some embodiments may only require a single response to the requesting CPU.

In some embodiments, the modification of routing tables also affects transactions that must go to every node in the system (and thus should not be filtered). Such broadcast transactions include, for example, lock requests and system management messages. In such embodiments, the probe filtering unit or cache coherence controller is programmed to send out such broadcasts and to accumulate the responses.

It should be noted that some of the arrows shown in these diagrams may represent multiple "hops" in the point-to-point infrastructure interconnecting the processing nodes. That is, depending on the number of processors and the topology in which the processors are interconnected, a probe from the PFU to a particular processor may need to go through another node before it arrives at its intended destination. In any case, whether a transmission requires one or multiple hops, it is represented in the figures by a single arrow for clarity.

One of the benefits of local probe filtering is that it allows a multi-processor system to scale better because it reduces or eliminates unnecessary probes that go to nodes that are known not to be caching the desired data. In addition, latency may be significantly reduced for lines which are not highly shared across nodes by reducing the number of messages that have to be sent. Moreover, where the underlying multi-processor architecture comprises the HyperTransport™ architecture from AMD, embodiments of the invention may be implemented with little or no alteration to the underlying architecture. That is, redirecting probes to a probe filtering unit and probe responses back to the probe filtering unit can be accomplished with little or no change to the current HyperTransport architecture and the implementation of that architecture. In addition, embodiments of the invention may be implemented in which non-probe related traffic (requests and responses) go directly between the nodes without having to go through the probe filtering unit.

While the invention has been particularly shown and described with reference to specific embodiments thereof, it will be understood by those skilled in the art that changes in the form and details of the disclosed embodiments may be made without departing from the spirit or scope of the invention. For example, embodiments of the present invention may be employed with multiple processor clusters connected through a point-to-point, switch, or bus architecture. In another example, multiple clusters of processors may share a single cache coherence controller, or multiple cache coherence controllers can be used in a single cluster. In addition, the mechanisms for facilitating local and remote probe filtering may be included in the same device or in separate devices. For example, the remote probe filtering functionality of a cache coherence controller in a multi-cluster system can be extended to facilitate local probe filtering. Alternatively, local probe filtering could be provided in a separate device deployed on a cluster's point-to-point interconnect.

In addition, although various advantages, aspects, and objects of the present invention have been discussed herein with reference to various embodiments, it will be understood that the scope of the invention should not be limited by reference to such advantages, aspects, and objects. Rather, the scope of the invention should be determined with reference to the appended claims.

WHAT IS CLAIMED IS:

1. A computer system comprising a plurality of processing nodes interconnected by a first point-to-point architecture, each processing node having a cache memory associated therewith, the computer system further comprising a probe filtering unit which is operable to receive probes corresponding to memory lines from the processing nodes and to transmit the probes only to selected ones of the processing nodes with reference to probe filtering information representative of states associated with selected ones of the cache memories.

2. The computer system of claim 1 wherein the probe filtering unit corresponds to an additional node interconnected with the plurality of processing nodes via the first point-to-point architecture.

3. The computer system of claim 2 wherein the additional node comprises a cache coherence controller, and the probe filtering information comprises a cache coherence directory which includes entries corresponding to memory lines stored in the selected cache memories.

4. The computer system of claim 1 wherein the plurality of processing nodes comprises a first cluster of processors, the computer system comprising a plurality of clusters of processors including the first cluster, the plurality of clusters being interconnected via a second point-to-point architecture.

5. The computer system of claim 4 further comprising a cache coherence controller on the first point-to-point architecture which is operable to facilitate interconnection of the first cluster with others of the plurality of clusters via the second point-to-point architecture.

6. The computer system of claim 5 wherein the cache coherence controller comprises the probe filtering unit, and the probe filtering information comprises a cache coherence directory.

7. The computer system of claim 1 wherein the first point-to-point architecture comprises a HyperTransport architecture.

9. The computer system of claim 1 wherein each of the processing nodes is operable to transmit the probes only to the probe filtering unit.

10. The computer system of claim 9 wherein each of the processing nodes has at least one routing table associated therewith which governs which portions of the first point-to-point architecture the associated processing node employs for communicating with others of the processing nodes, the at least one routing table in each of the processing nodes being configured to direct all of the probes to the probe filtering unit.

11. The computer system of claim 10 wherein the at least one routing table in each of the processing nodes is configured to direct all broadcasts to the probe filtering unit.

12. The computer system of claim 1 wherein each of the processing nodes is programmed to complete a memory transaction after receiving a first number of responses to a first probe, the first number being fewer than the number of processing nodes.

13. The computer system of claim 12 wherein the probe filtering unit has temporary storage associated therewith for holding read response data from one of the cache memories, and the first number is one.

14. The computer system of claim 12 wherein the probe filtering unit is operable to forward read response data to a requesting node before accumulating all probe responses associated with the memory transaction, and the first number is two.

15. The computer system of claim 1 wherein the probe filtering unit is further operable to modify the probes such that the selected processing nodes transmit responses to the probes to the probe filtering unit.

16. The computer system of claim 1 wherein the probe filtering unit is operable to accumulate responses to each probe, and respond to requesting nodes in accordance with the accumulated responses.

17. A probe filtering unit for use in a computer system comprising a plurality of processing nodes interconnected by a first point-to-point architecture, each processing node having a cache memory associated therewith, the probe filtering unit being operable to receive probes corresponding to memory lines from the processing nodes and to transmit the probes only to selected ones of the processing nodes with reference to probe filtering information representative of states associated with selected ones of the cache memories.

18. An integrated circuit comprising the probe filtering unit of claim 17.

19. The integrated circuit of claim 18 wherein the integrated circuit comprises an application-specific integrated circuit.

20. At least one computer-readable medium having data structures stored therein representative of the probe filtering unit of claim 17.

21. The at least one computer-readable medium of claim 20 wherein the data structures comprise a simulatable representation of the probe filtering unit.

22. The at least one computer-readable medium of claim 21 wherein the simulatable representation comprises a netlist.

23. The at least one computer-readable medium of claim 20 wherein the data structures comprise a code description of the probe filtering unit.

24. The at least one computer-readable medium of claim 23 wherein the code description corresponds to a hardware description language.

25. A set of semiconductor processing masks representative of at least a portion of the probe filtering unit of claim 17.

26. A computer implemented method for reducing probe traffic in a computer system comprising a plurality of processing nodes interconnected by a first point-to-point architecture, each processing node having a cache memory associated therewith, the method comprising:

transmitting a probe from a first one of the processing nodes only to a probe filtering unit, the probe corresponding to a memory line;

evaluating the probe with the probe filtering unit to determine whether a valid copy of the memory line is in any of the cache memories, the evaluating being done with reference to probe filtering information associated with the probe filtering unit and representative of states associated with selected ones of the cache memories;

transmitting the probe from the probe filtering unit only to selected ones of the processing nodes identified by the evaluating;

accumulating probe responses from the selected processing nodes with the probe filtering unit; and

responding to the probe from the first processing node only with the probe filtering unit.

REDUCING PROBE TRAFFIC IN MULTIPROCESSOR SYSTEMS

ABSTRACT OF THE DISCLOSURE

A computer system having a plurality of processing nodes interconnected by a first point-to-point architecture is described. Each processing node has a cache memory associated therewith. A probe filtering unit is operable to receive probes corresponding to memory lines from the processing nodes and to transmit the probes only to selected ones of the processing nodes with reference to probe filtering information. The probe filtering information is representative of states associated with selected ones of the cache memories.

Figure 1A

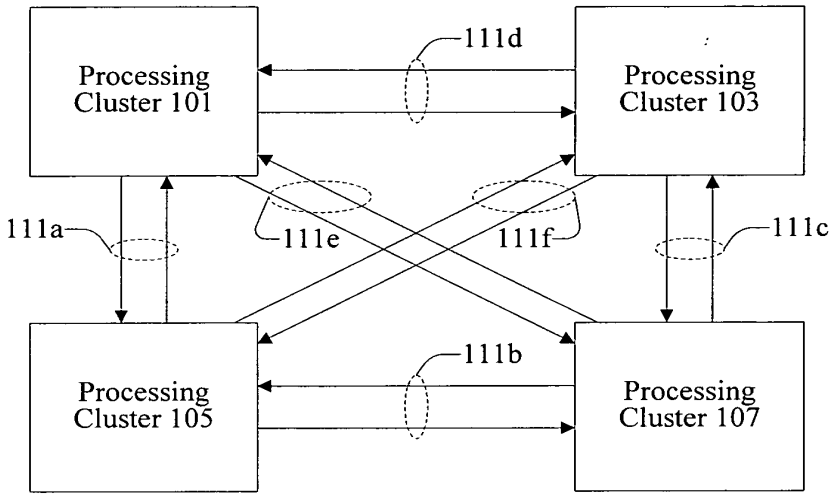


Figure 1B

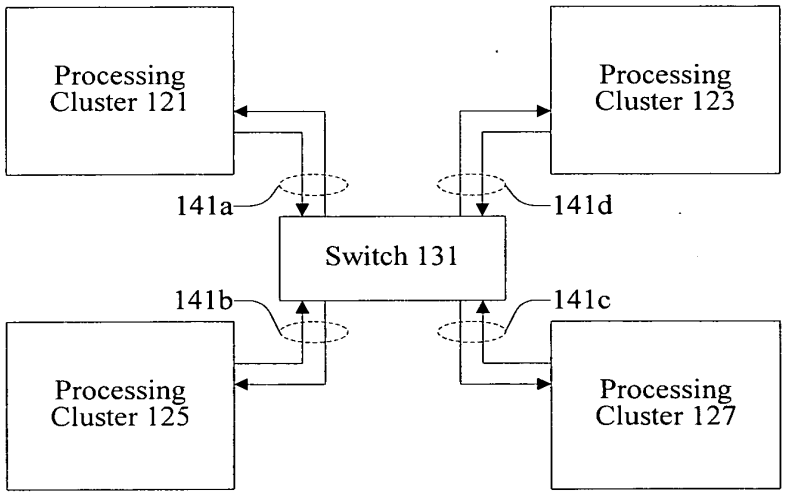


Figure 2

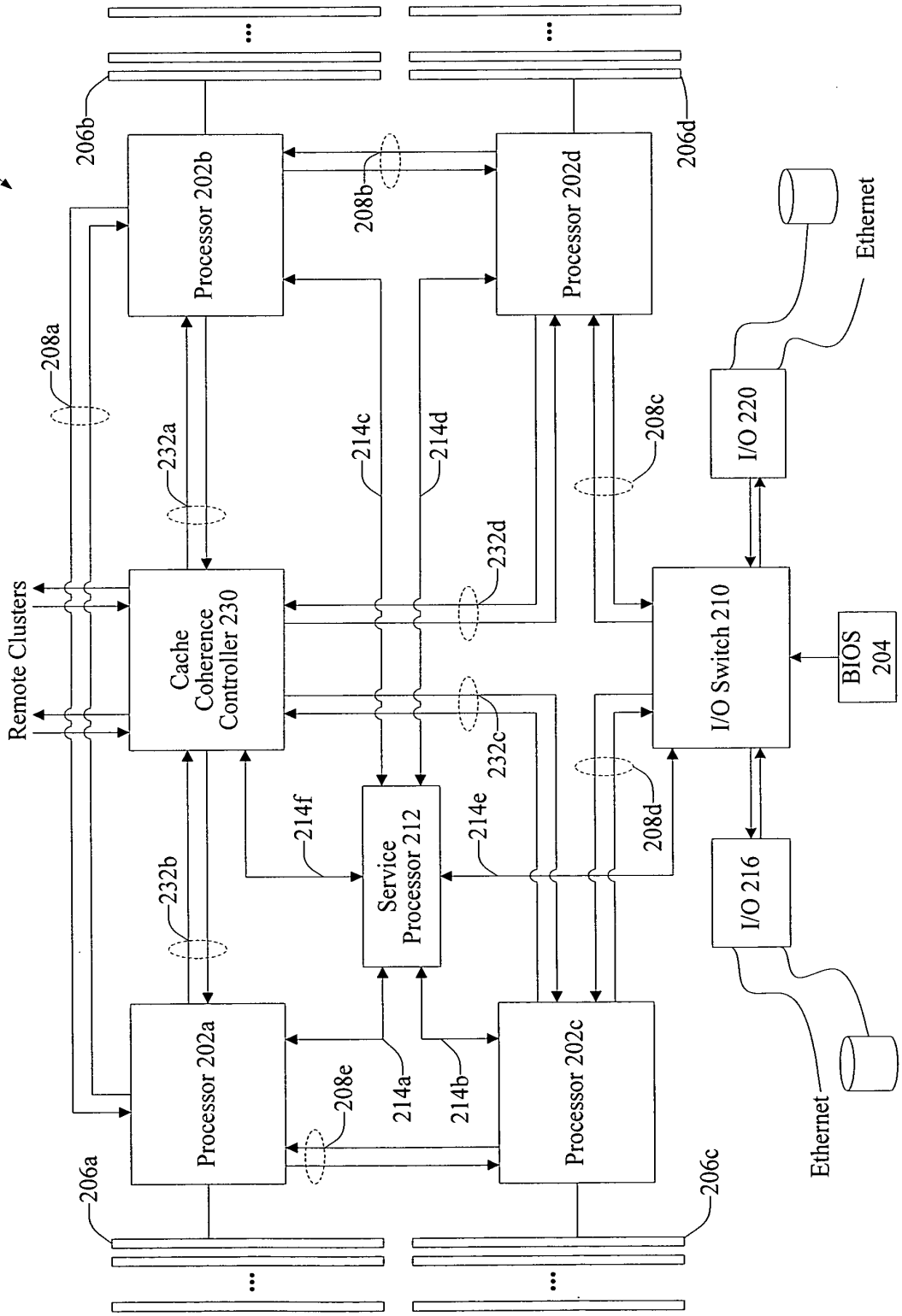

200
206b
206d
Processor 202b
Processor 202d
208b
208a
232a
214c
214d
208c
I/O 220
Ethernet
Remote Clusters
Cache Coherence Controller 230
232d
I/O Switch 210
BIOS 204
232c
214f
Service Processor 212
214e
208d
232b
I/O 216
Processor 202a
Processor 202c
208e
214a
214b
206a
206c
Ethernet

Figure 3

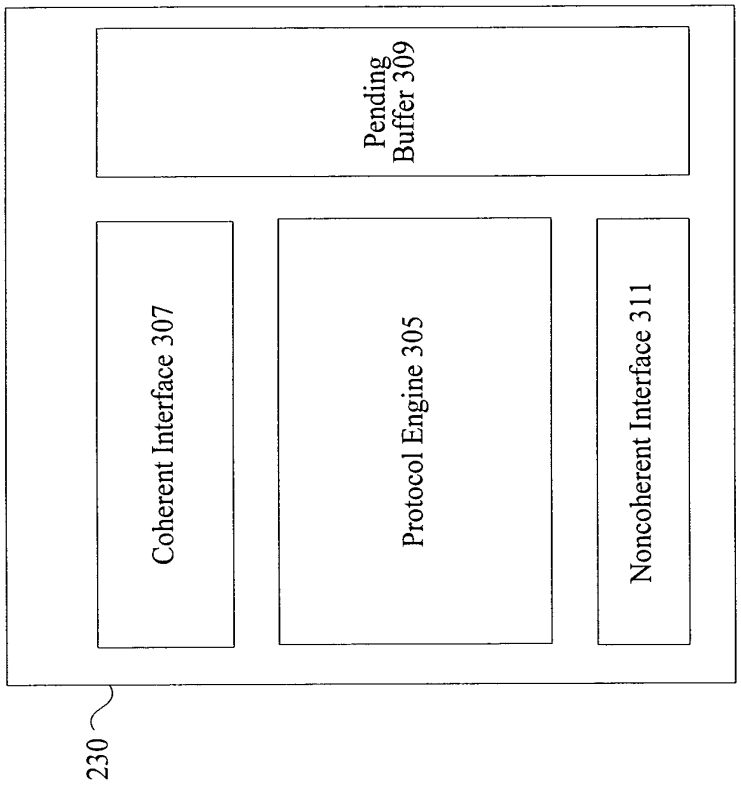

Coherent Interface 307
Protocol Engine 305
Noncoherent Interface 311
Pending Buffer 309
230

Figure 4

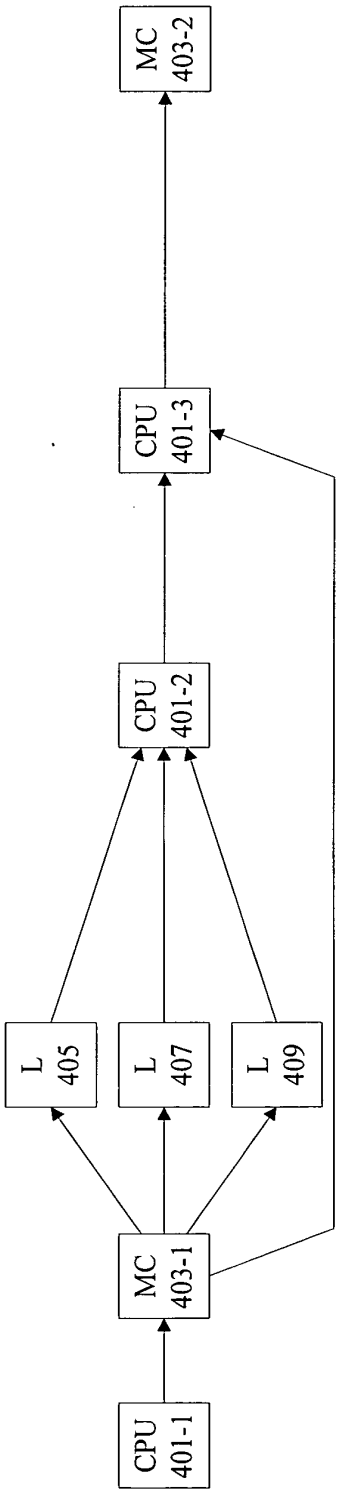


Figure 5A

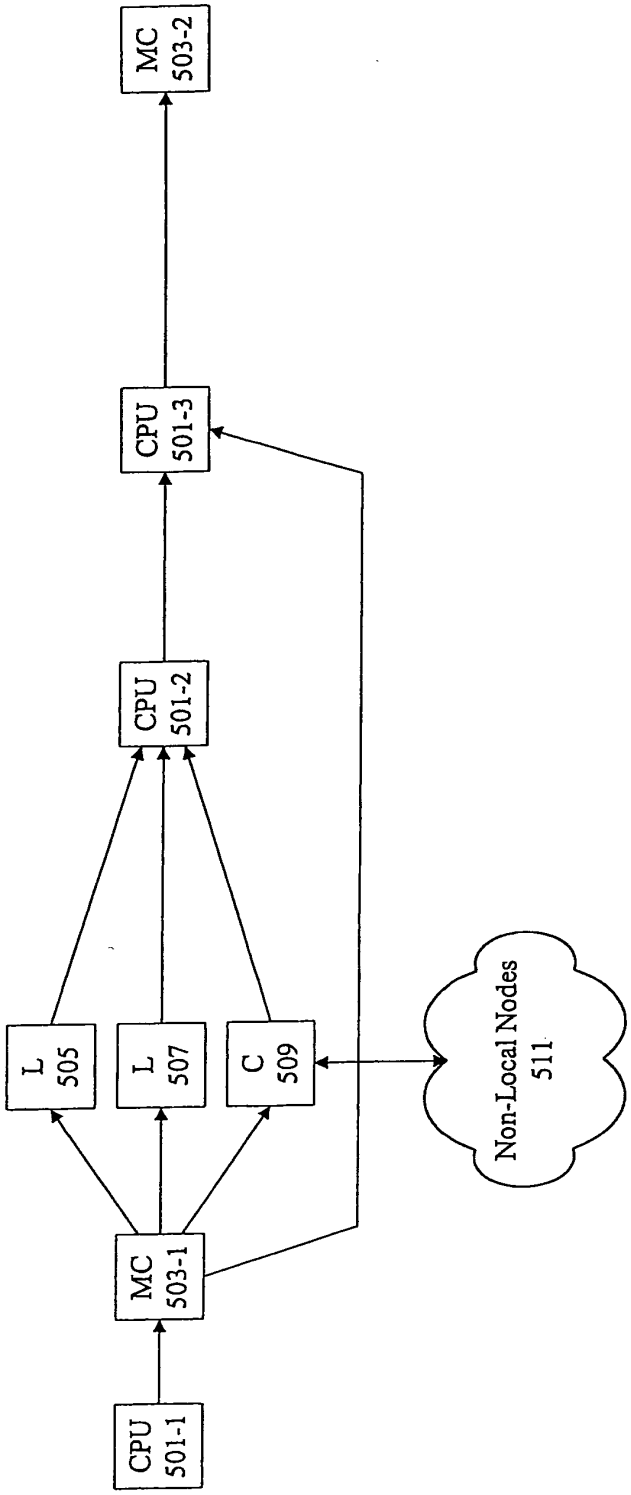

CPU 501-1
MC 503-1
L 505
L 507
C 509
CPU 501-2
CPU 501-3
MC 503-2
Non-Local Nodes 511

Figure 5B

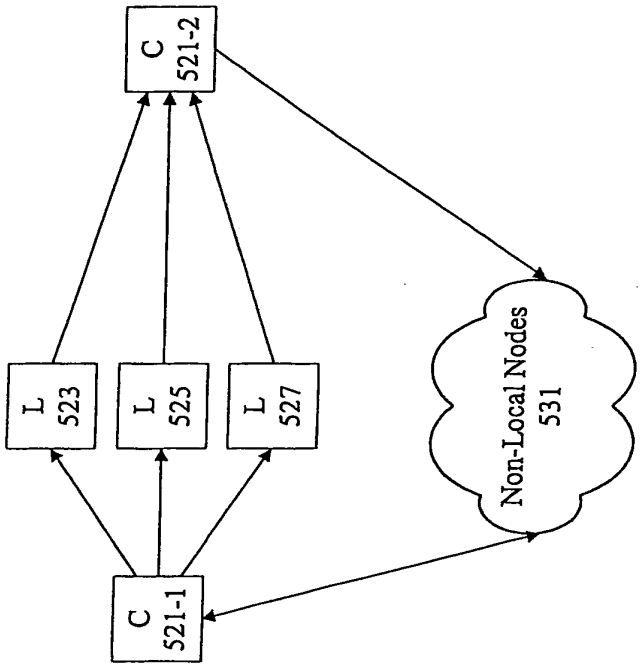


Figure 5C

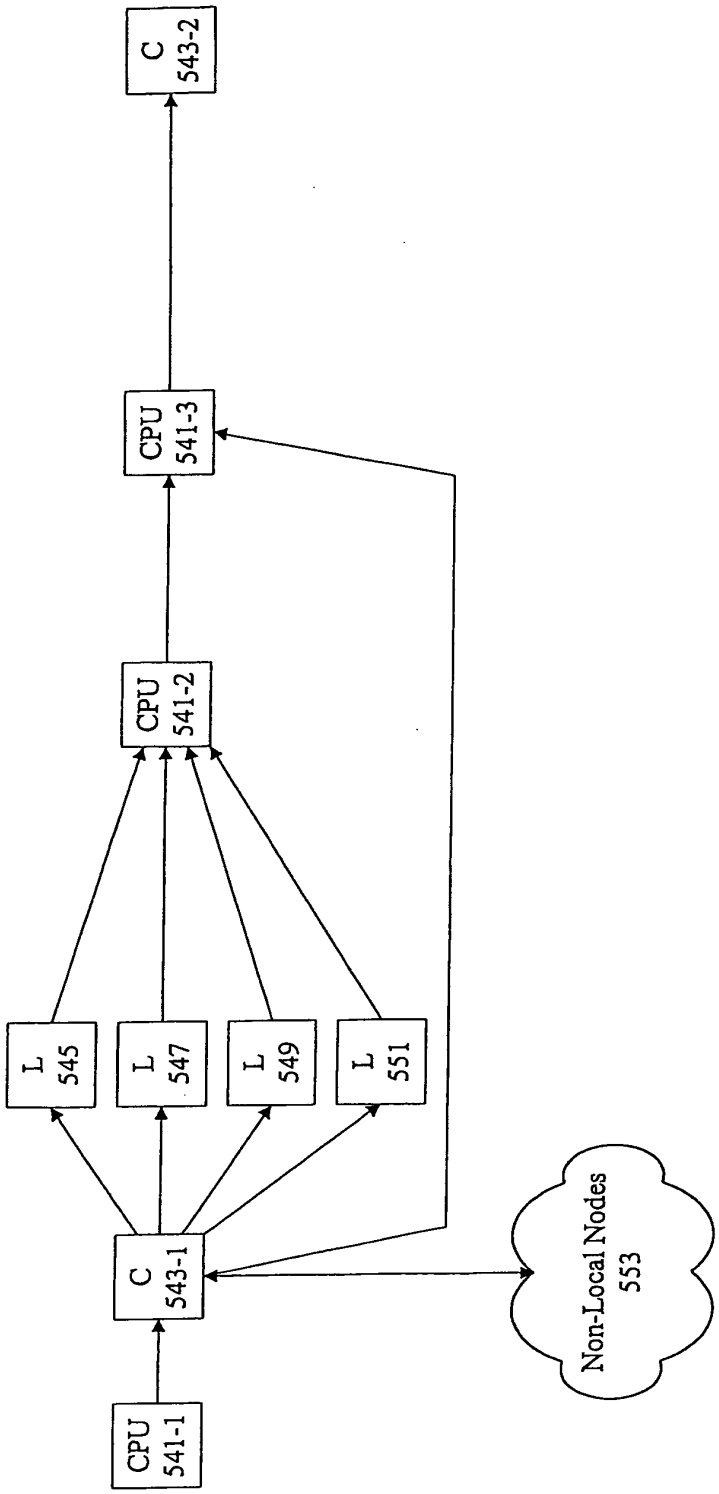

CPU 541-1
C 543-1
L 545
L 547
L 549
L 551
CPU 541-2
CPU 541-3
C 543-2
Non-Local Nodes 553

Figure 5D

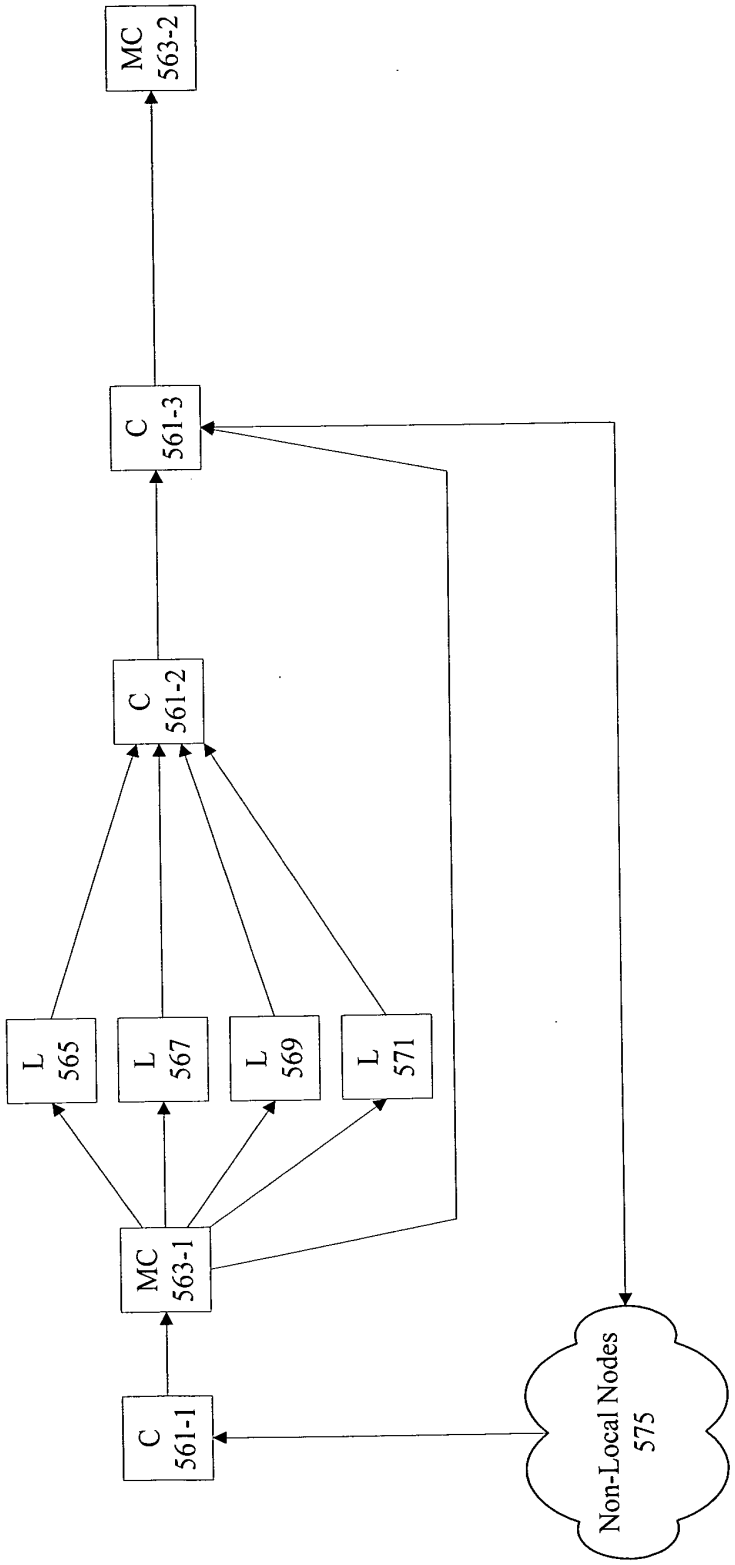

C 561-1
MC 563-1
L 565
L 567
L 569
L 571
C 561-2
C 561-3
MC 563-2
Non-Local Nodes 575

Figure 6

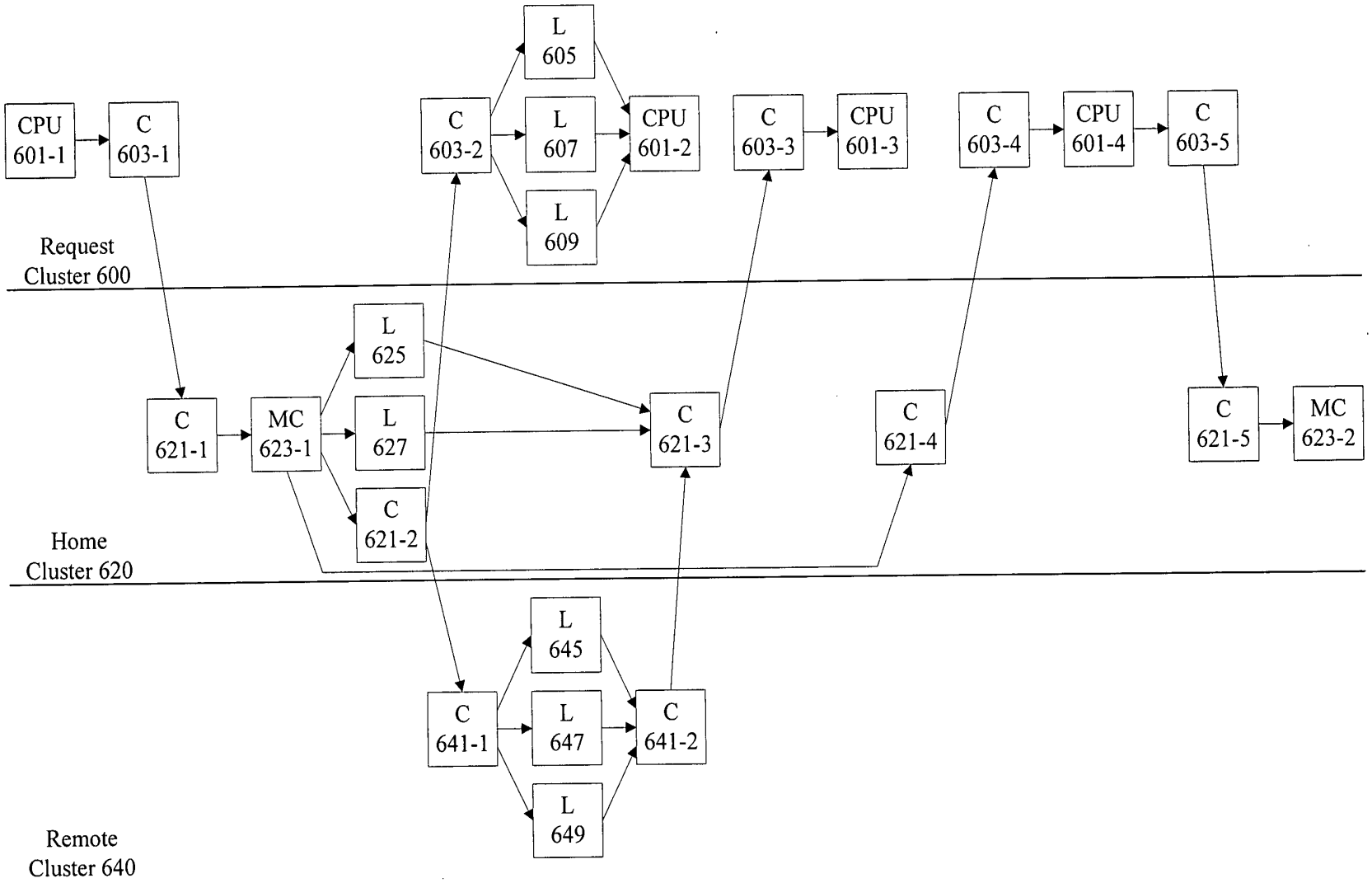

CPU 601-1
C 603-1
C 603-2
L 605
L 607
L 609
CPU 601-2
C 603-3
CPU 601-3
C 603-4
CPU 601-4
C 603-5
Request Cluster 600
L 625
C 621-1
MC 623-1
L 627
C 621-2
C 621-3
C 621-4
C 621-5
MC 623-2
Home Cluster 620
L 645
C 641-1
L 647
L 649
C 641-2
Remote Cluster 640

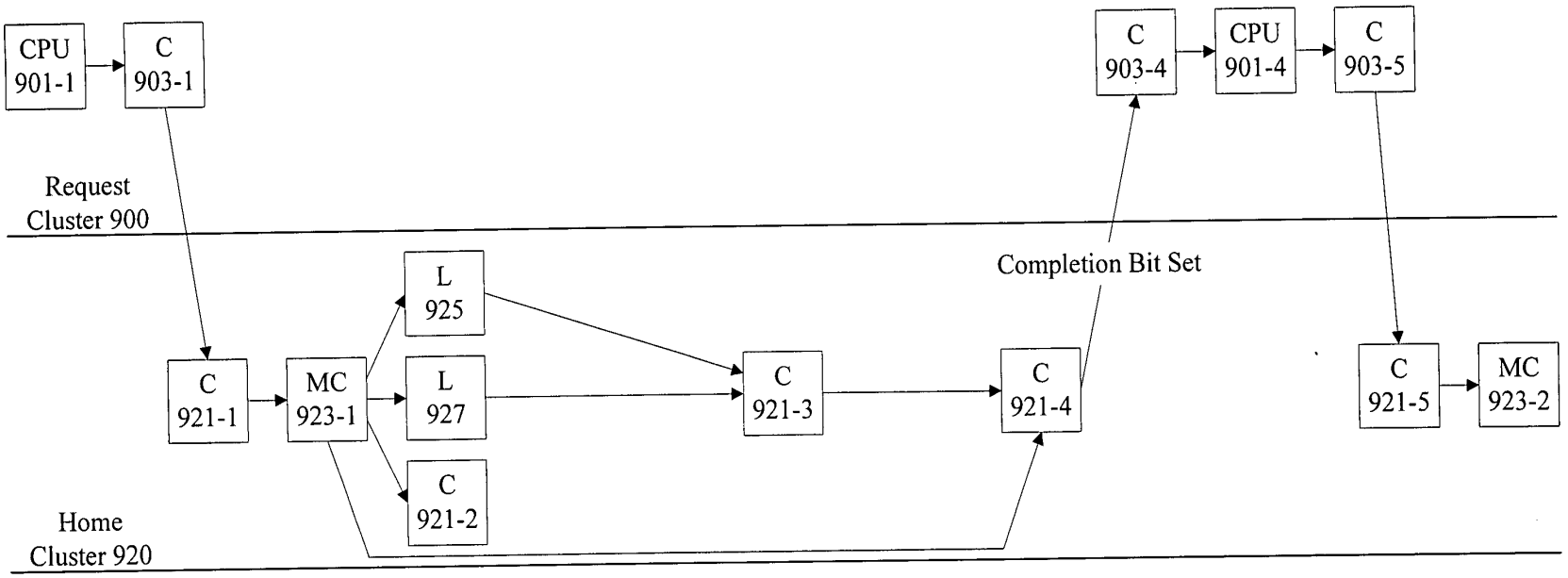
Figure 7

Coherence Directory 701			
Memory Line 711	State 713	Dirty Data Owner 715	Occupancy Vector 717
Address 721	Invalid	N/A	N/A
Address 731	Invalid	N/A	N/A
Address 741	Shared	N/A	Clusters 1,3
Address 751	Shared	N/A	Clusters 1, 2, 3, 4
Address 761	Owned	Cluster 4	Cluster 2, 3, 4
Address 771	Owned	Cluster 2	Cluster 2, 4
Address 781	Modified	Cluster 2	N/A
Address 791	Modified	Cluster 3	N/A
...	...	...	...

Figure 8

Probe Filter Information 821	Read Block (Read) 823	Read Block Modify (Read/Write) 825
Invalid 831	Can use completion bit. Probe home cluster. (801)	Can use completion bit. Probe home cluster. (809)
Shared 833	Can use completion bit. Probe home cluster. (803)	N/A (811)
Owned 835	Can use completion bit. Probe remote cluster with line cached in owned state. (805)	N/A (813)
Modified 837	Can use completion bit. Probe remote cluster with line cached in modified state. (807)	Can use completion bit. Probe remote cluster. (815)

Figure 9


CPU 901-1
C 903-1
Request Cluster 900
C 921-1
MC 923-1
L 925
L 927
C 921-2
C 921-3
C 921-4
Completion Bit Set
C 903-4
CPU 901-4
C 903-5
C 921-5
MC 923-2
Home Cluster 920
Remote Cluster 940

232

Figure 10

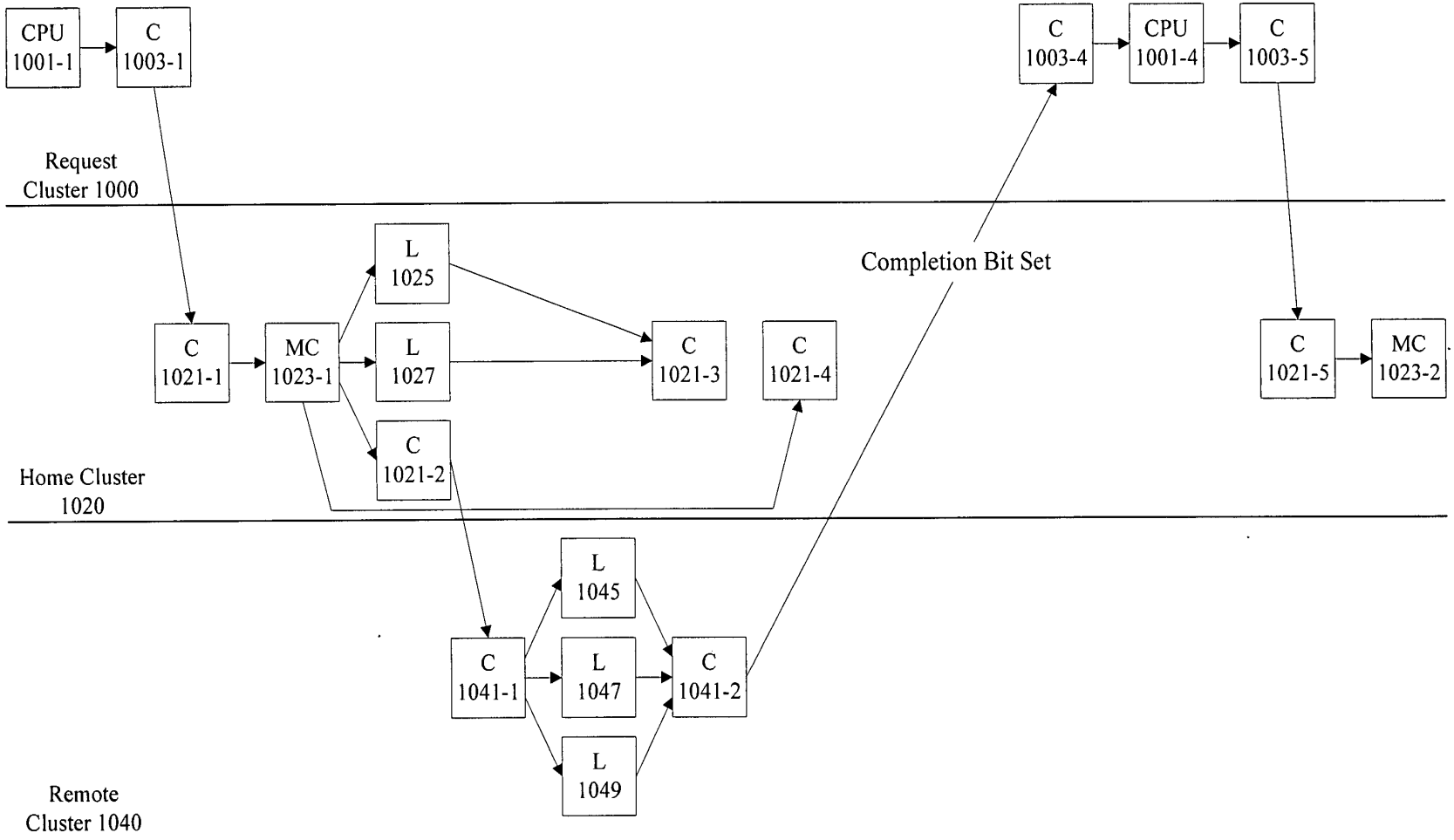

CPU 1001-1
C 1003-1
C 1003-4
CPU 1001-4
C 1003-5
Request Cluster 1000
L 1025
Completion Bit Set
C 1021-1
MC 1023-1
L 1027
C 1021-3
C 1021-4
C 1021-5
MC 1023-2
C 1021-2
Home Cluster 1020
L 1045
C 1041-1
L 1047
C 1041-2
L 1049
Remote Cluster 1040

Figure 11

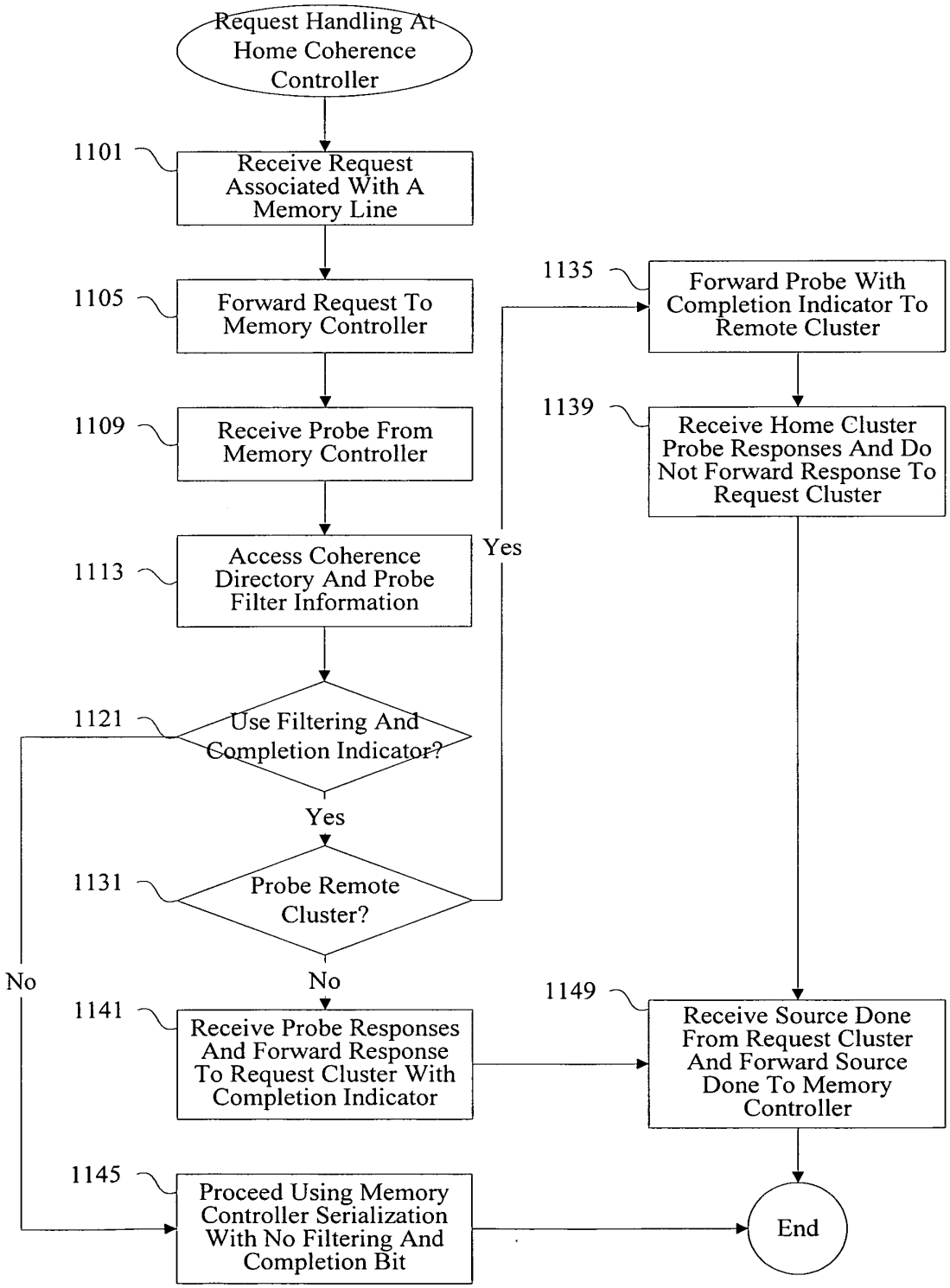

Request Handling At Home Coherence Controller
1101
Receive Request Associated With A Memory Line
1105
Forward Request To Memory Controller
1109
Receive Probe From Memory Controller
1113
Access Coherence Directory And Probe Filter Information
1121
Use Filtering And Completion Indicator?
Yes
No
1131
Probe Remote Cluster?
Yes
No
1135
Forward Probe With Completion Indicator To Remote Cluster
1139
Receive Home Cluster Probe Responses And Do Not Forward Response To Request Cluster
1141
Receive Probe Responses And Forward Response To Request Cluster With Completion Indicator
1145
Proceed Using Memory Controller Serialization With No Filtering And Completion Bit
1149
Receive Source Done From Request Cluster And Forward Source Done To Memory Controller
End

Figure 12

Memory Controller Filter Information 1221		
	Read Block [Read] 1223	Read Block Modify [Read/Write] 1225
Invalid 1231	Send request to target. (1201)	Send request to target. (1209)
Shared 1233	Send request to target. (1203)	Send request to target. (1211)
Owned 1235	Forward Probe To Owning Cluster. (1205)	Send request to target. (1213)
Modified 1237	Forward Probe To Modified Cluster. (1207)	Forward Probe To Modified Cluster. (1215)

Figure 13

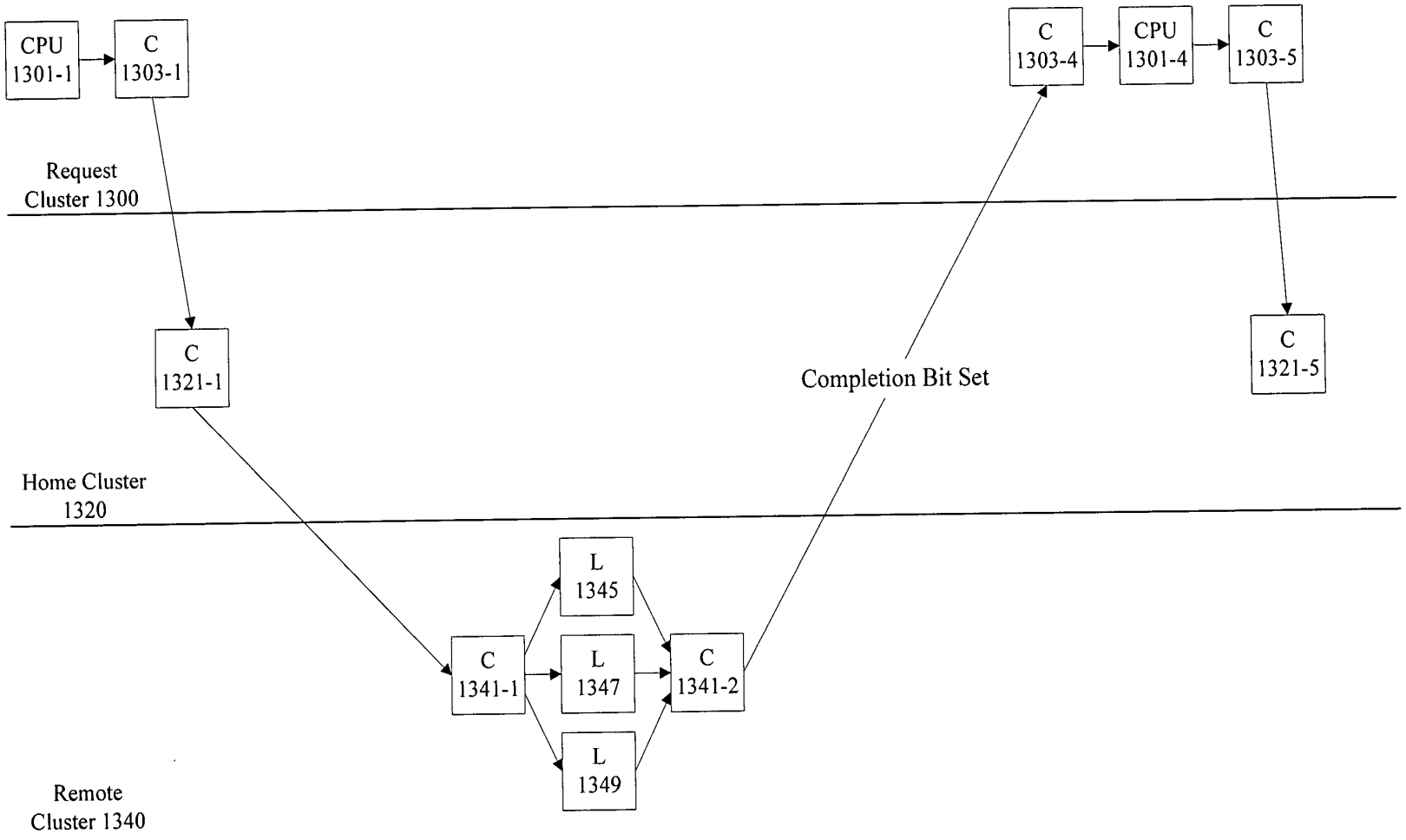
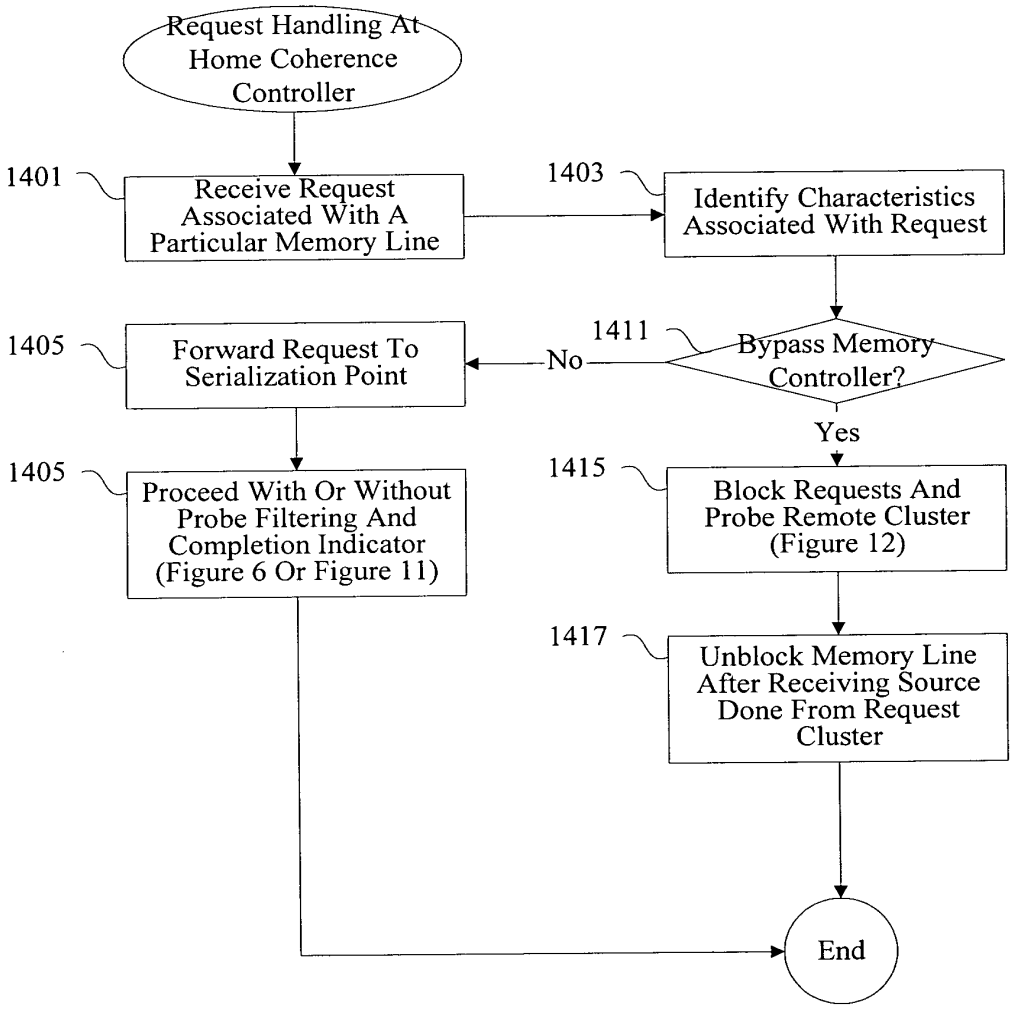

CPU
1301-1
C
1303-1
C
1303-4
CPU
1301-4
C
1303-5
Request
Cluster 1300
C
1321-1
Completion Bit Set
C
1321-5
Home Cluster
1320
L
1345
C
1341-1
L
1347
C
1341-2
L
1349
Remote
Cluster 1340

Figure 14


Request Handling At Home Coherence Controller
1401
Receive Request Associated With A Particular Memory Line
1403
Identify Characteristics Associated With Request
1411
Bypass Memory Controller?
No
1405
Forward Request To Serialization Point
Yes
1405
Proceed With Or Without Probe Filtering And Completion Indicator (Figure 6 Or Figure 11)
1415
Block Requests And Probe Remote Cluster (Figure 12)
1417
Unblock Memory Line After Receiving Source Done From Request Cluster
End

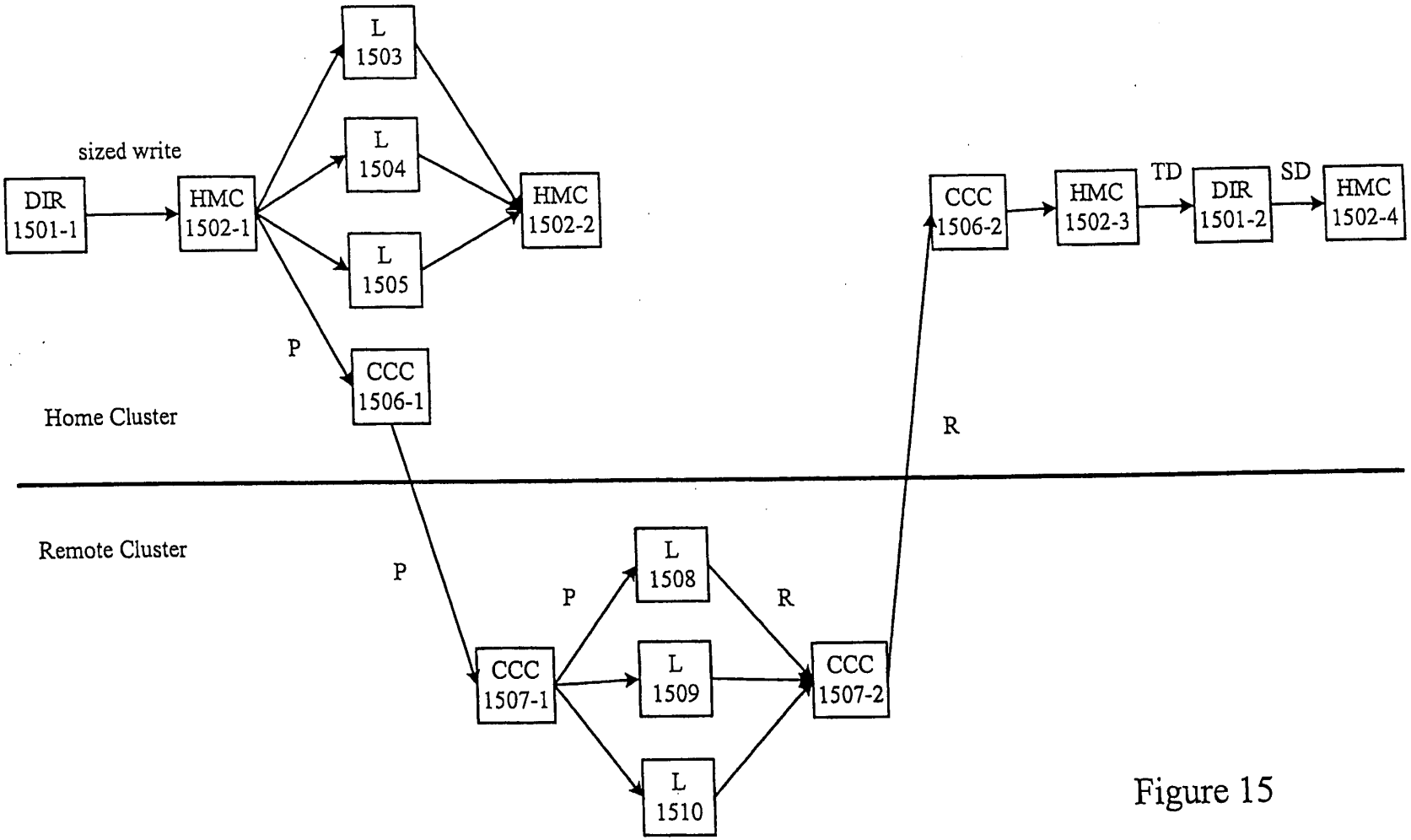

sized write
DIR 1501-1
HMC 1502-1
L 1503
L 1504
L 1505
HMC 1502-2
P
CCC 1506-1
Home Cluster
Remote Cluster
P
CCC 1507-1
P
L 1508
L 1509
L 1510
R
CCC 1507-2
R
CCC 1506-2
HMC 1502-3
TD
DIR 1501-2
SD
HMC 1502-4

Figure 15

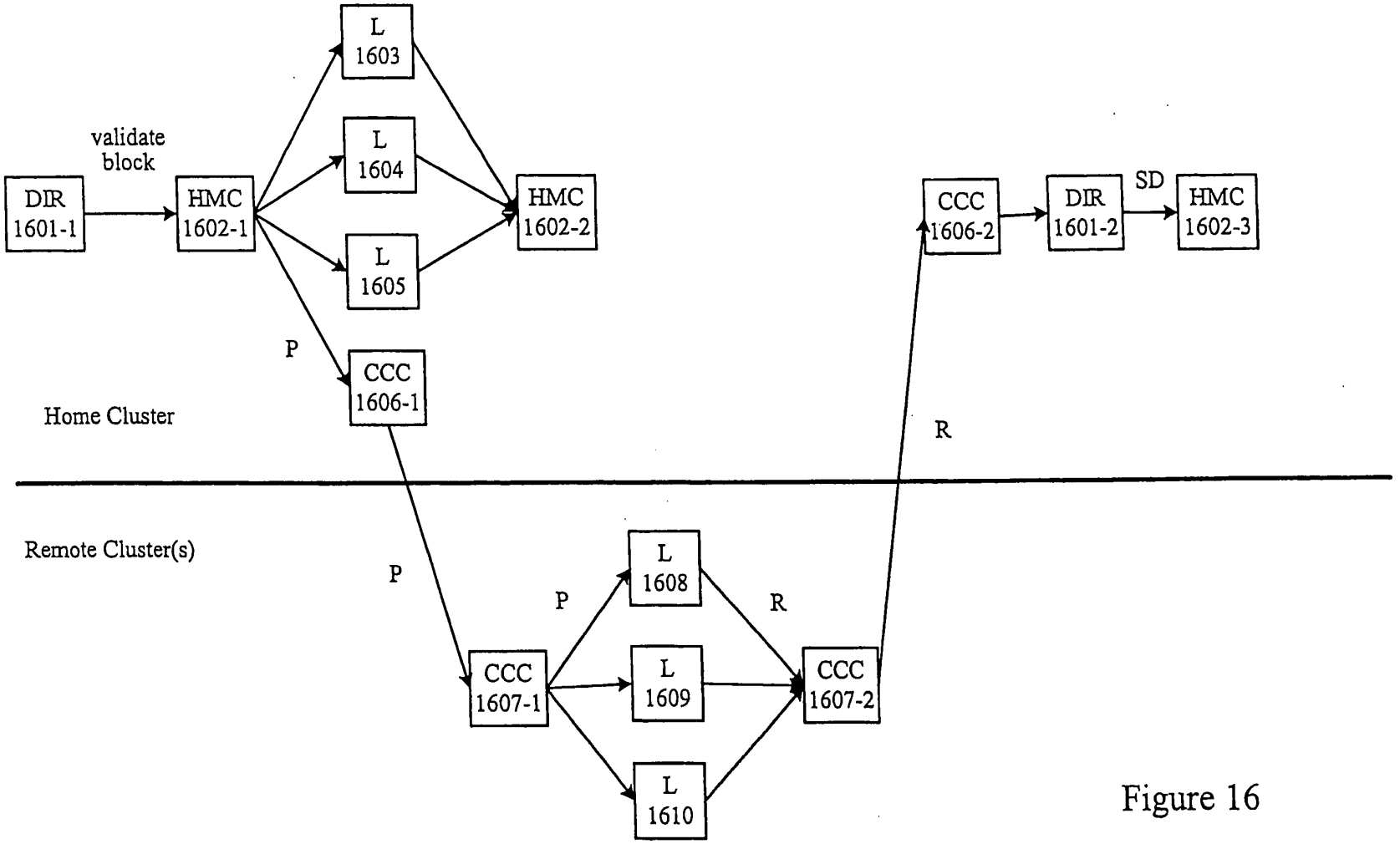

validate block
DIR 1601-1
HMC 1602-1
L 1603
L 1604
L 1605
HMC 1602-2
P
CCC 1606-1
Home Cluster
Remote Cluster(s)
P
CCC 1607-1
P
L 1608
L 1609
L 1610
R
CCC 1607-2
R
CCC 1606-2
DIR 1601-2
SD
HMC 1602-3

Figure 16

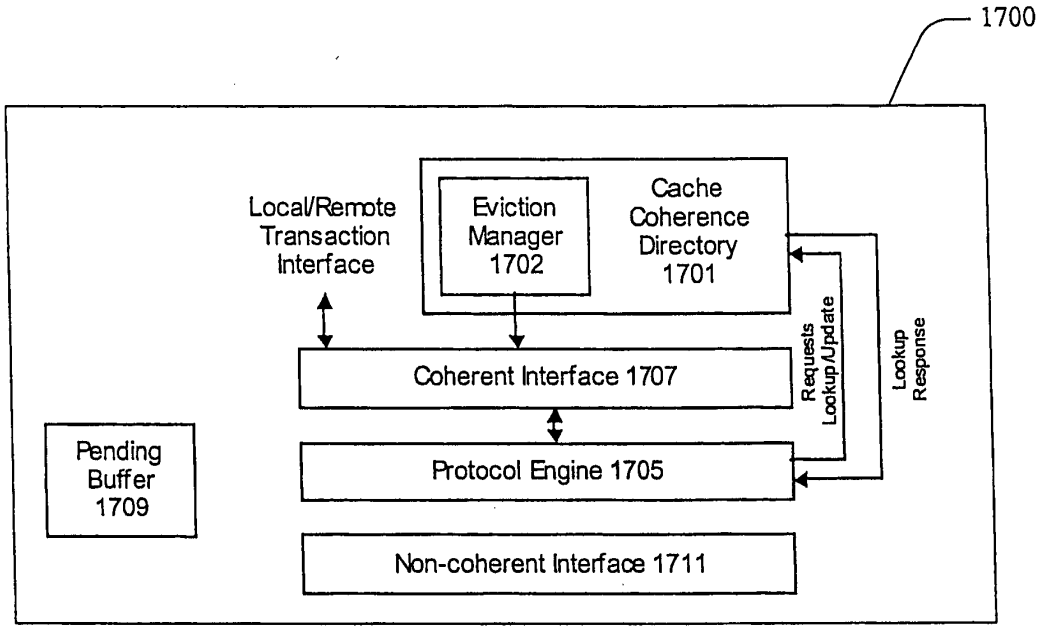
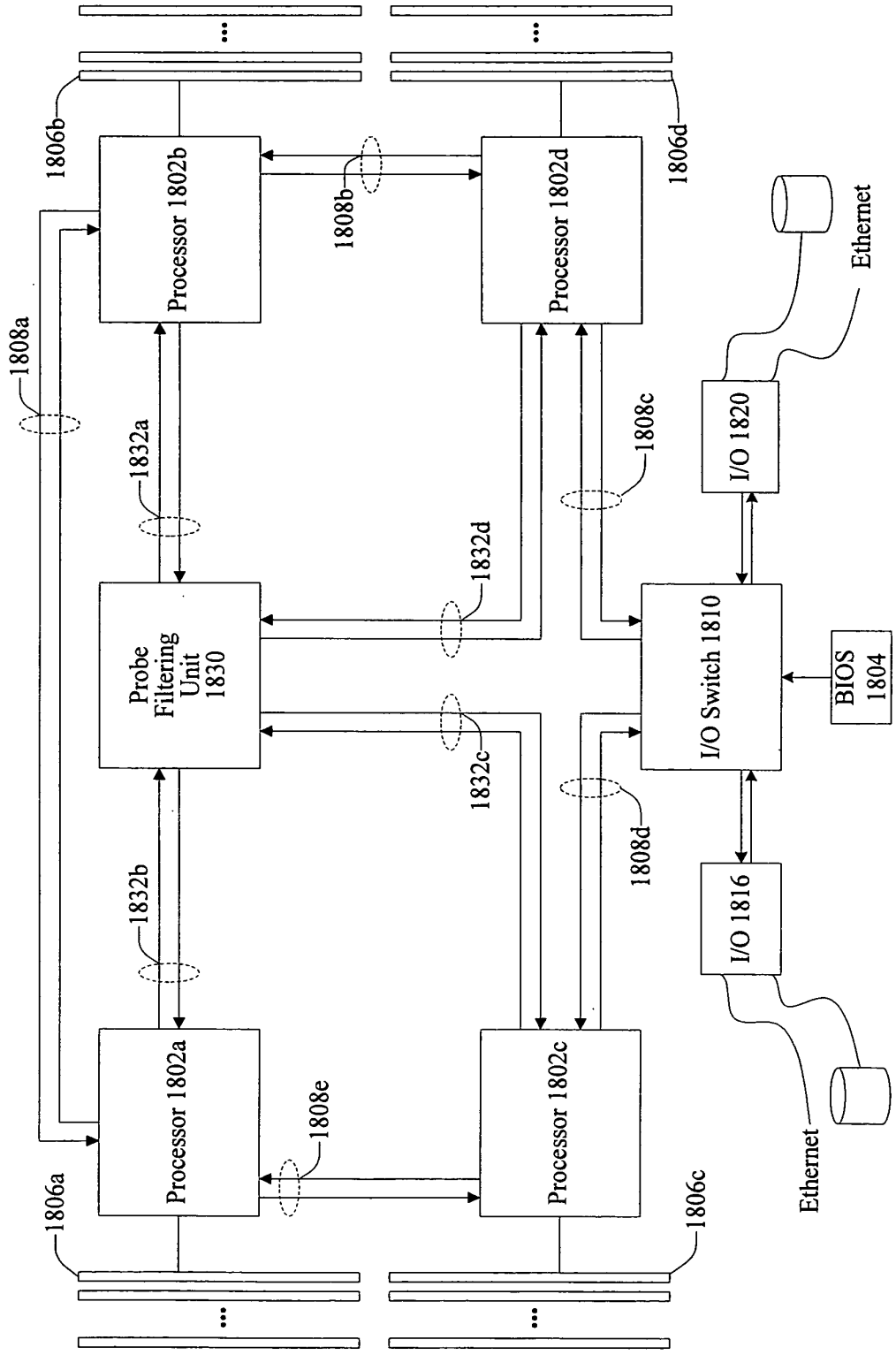

1700
Local/Remote
Transaction
Interface
Eviction
Manager
1702
Cache
Coherence
Directory
1701
Requests
Lookup/Update
Lookup
Response
Coherent Interface 1707
Pending
Buffer
1709
Protocol Engine 1705
Non-coherent Interface 1711

Figure 17

Figure 18


1800
1806b
1806d
1808b
Processor 1802b
Processor 1802d
1808a
1832a
1808c
1832d
Probe Filtering Unit 1830
I/O Switch 1810
I/O 1820
Ethernet
BIOS 1804
1832c
1808d
1832b
I/O 1816
Processor 1802a
Processor 1802c
1808e
1806a
1806c
Ethernet

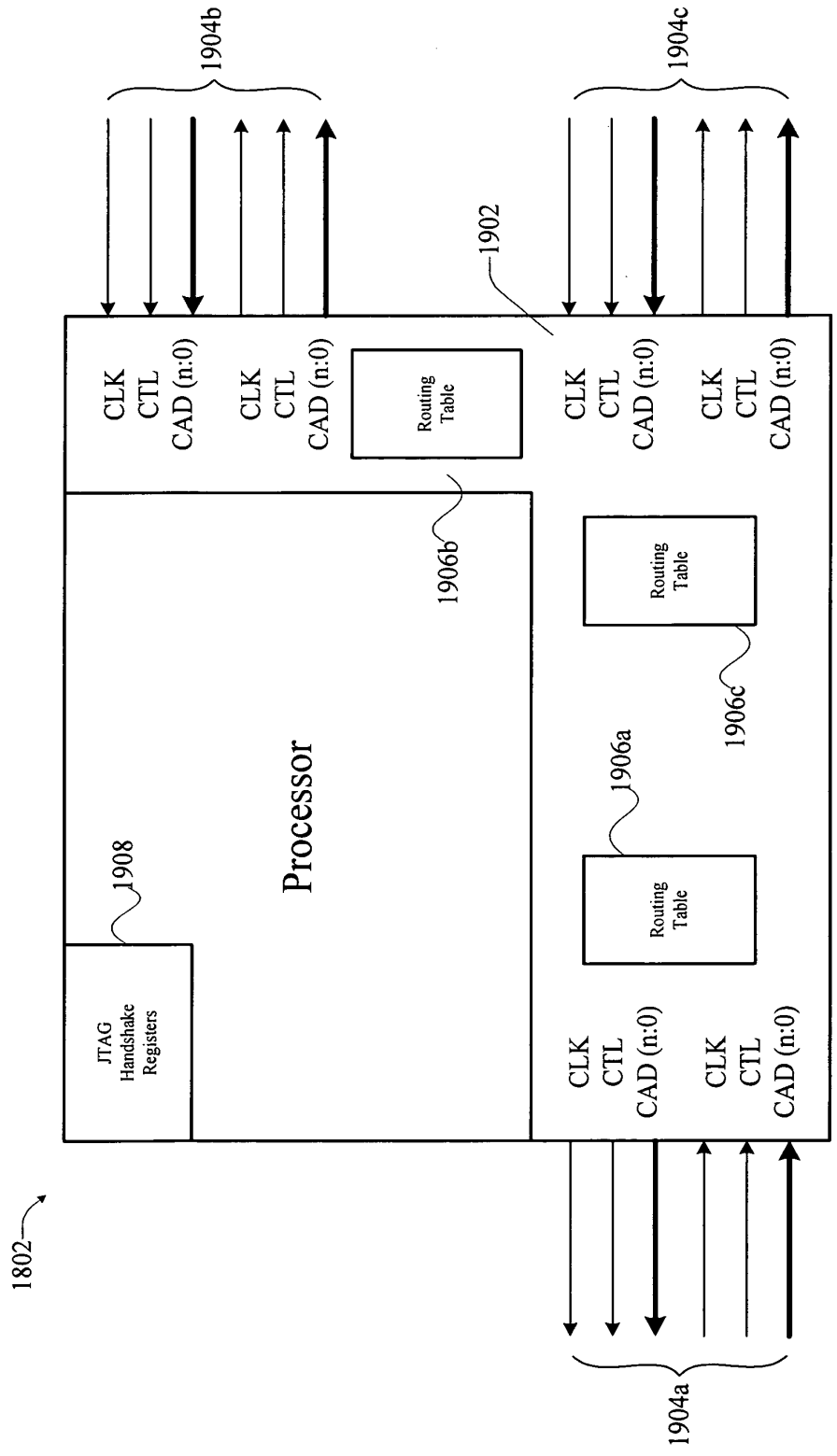

1802
1904b
1904c
1902
CLK
CTL
CAD (n:0)
CLK
CTL
CAD (n:0)
Routing Table
CLK
CTL
CAD (n:0)
CLK
CTL
CAD (n:0)
1906b
Routing Table
1906c
1906a
Routing Table
Processor
1908
JTAG Handshake Registers
CLK
CTL
CAD (n:0)
CLK
CTL
CAD (n:0)
1904a

Figure 19

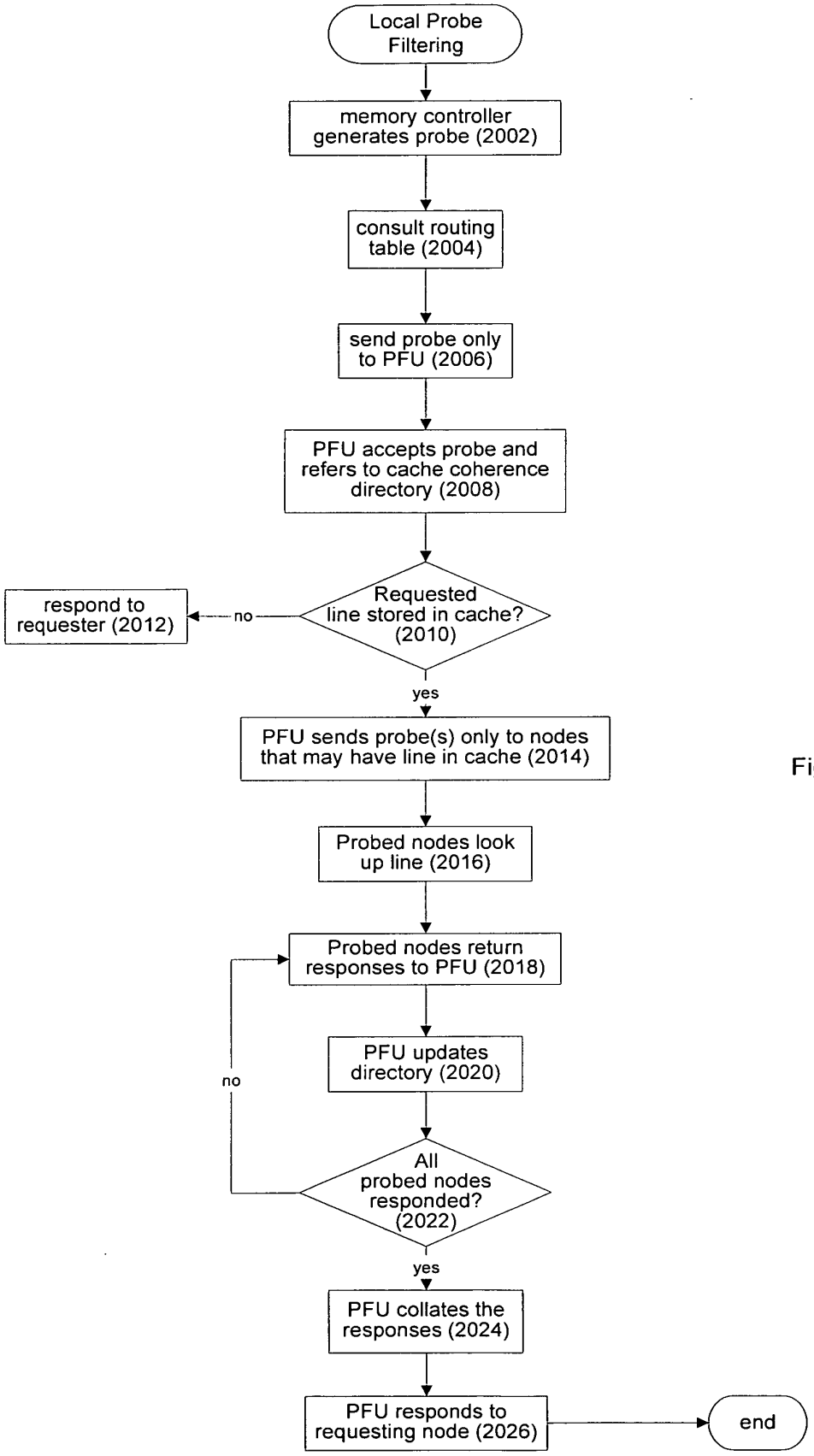
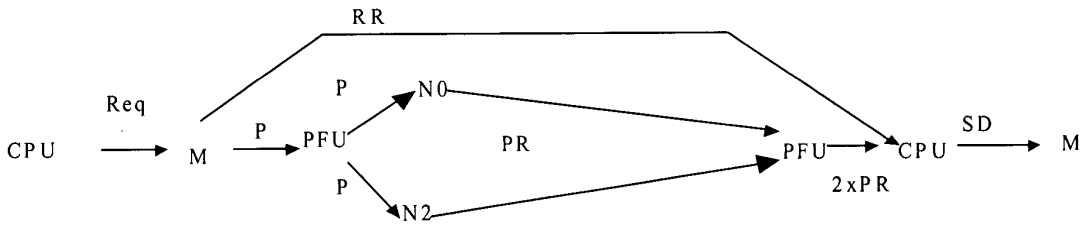

Local Probe Filtering
memory controller generates probe (2002)
consult routing table (2004)
send probe only to PFU (2006)
PFU accepts probe and refers to cache coherence directory (2008)
Requested line stored in cache? (2010)
no
respond to requester (2012)
yes
PFU sends probe(s) only to nodes that may have line in cache (2014)
Probed nodes look up line (2016)
Probed nodes return responses to PFU (2018)
PFU updates directory (2020)
All probed nodes responded? (2022)
no
yes
PFU collates the responses (2024)
PFU responds to requesting node (2026)
end

Figure 20

ProbeSrc only goes to filtering unit from M CT, gets new TGT and resent out as a ProbeTgt.

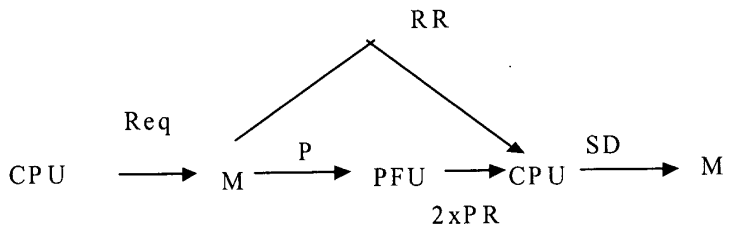


N1

N3

Non probed nodes due to probe filtering are not aware of the transactoin.

Figure 21



N0 N1

N2 N3

Non probed nodes due to probe filtering are not aware of the transactoin.

Figure 22

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2004

Application or Docket Number: 10966161

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	25	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	25 minus 20=	* 5
INDEPENDENT CLAIMS	3 minus 3 =	* 0
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	395.00	OR	BASIC FEE	790.00
X$ 9=		OR	X$18=	90
X44=		OR	X88=	
+150=		OR	+300=	
TOTAL		OR	TOTAL	880

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X44=		OR	X88=	
+150=		OR	+300=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X44=		OR	X88=	
+150=		OR	+300=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X44=		OR	X88=	
+150=		OR	+300=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.