UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of:	Morton et al.	Case Nos. IPR2015-00158
U.S. Patent No.	7,296,121	IPR2015-00159
Issue Date:	Nov. 13, 2007	IPR2015-00163
Appl. Serial No.:	10/966,161	
Filing Date:	Oct. 15, 2004	

Title: REDUCING PROBE TRAFFIC IN MULTIPROCESSOR SYSTEMS

DECLARATION OF VOJIN OKLOBDZIJA, Ph.D. IN SUPPORT OF PATENT OWNER'S MOTIONS TO AMEND

I, Vojin Oklobdzija, PhD, hereby declare as follows:

1. My name is Dr. Vojin Oklobdzija. I submit this declaration in support of Patent Owner's Motions to Amend in IPR2015-00158, -00159, and -00163. I have been asked to offer technical opinions relating to U.S. Patent No. 7,296,121 and the proposed substitute claims presented by the motions.

2. I received a Dipl. Ing. (equivalent to a Master's in Electrical Engineering in the U.S.) degree in Telecommunications and Electronics in 1971 from the University of Belgrade, Yugoslavia, followed by a Master's in Computer Science from the University of California, Los Angeles in 1978. I received a Ph.D. in Computer Science with a minor in Electronics from the University of California, Los Angeles in 1982.

3. Following my Ph.D. graduation, I spent 9 years at IBM's T.J. Watson Research Center working on microprocessor architecture, development

and design. In my career at IBM, I worked on the early development of RISC (Reduced Instruction Set Architecture Computer) architecture and development of a new processor generation for IBM. Most notably, I worked on the first commercial RISC computer, IBM ROMP, as well as the first super-scalar microprocessor, IBM RS/6000.

4. After leaving IBM, I have held faculty (Full Professor) position at the University of California, Davis; and visiting positions at the University of California Berkeley, Sydney University in Australia; EPFL in Switzerland and others. I have over 20 years of teaching experience, teaching courses in: Computer Architecture, Computer Design, Digital Design, VLSI Circuits as well as advanced post-graduate courses in Computer Architecture and Design. During this time, I served as a consultant with members of the microprocessor industry extensively and was a principal architect in the Siemens/Infineon TriCore processor.

5. After retiring from the academia, I returned back to industry. In 2013, I became a Senior Director of Microprocessor Development at Skyera Inc., a startup company that was subsequently acquired by Hitachi Ltd. While working at Skyera, I lead a team developing an on-chip processor array consisting of a grid or 256 processors, including development of its cache-coherency mechanism and its fast cache memory hierarchy.

6. Currently I am President and CTO of my own startup company, Silicon Analytics Inc. and I also work as a consultant. I am a named inventor on 15 issued U.S. Patents and a similar number of international patents. I have also authored several books on microprocessor design, including a book titled "Computer Engineering Handbook," published by CRC Press in 2001, which won the CHOICE Outstanding Academic Title Award for 2002, as well as "High Performance Energy Efficient Microprocessor Design" published Springer in 2006. I have attached a true and correct copy of my curriculum vitae as Exhibit 2017, which further sets forth my qualifications.

7. I have reviewed and am familiar with the content of U.S. Patent No. 7,296,121 ("the '121 Patent"). I have also reviewed each of the items of prior art cited on the face of the '121 Patent. I have also reviewed the prior art submitted in connection with IPR2015-00158, -00159, -00161, -00163, and -00172. I have also reviewed the prior art disclosed by the Samsung defendants in their answer filed *Memory Integrity LLC v. Samsung Electronics Company Ltd. et al*, Dkt. No. 12 (D. Del. Feb. 24, 2014), Ex. 2038. I have also reviewed the invalidity contentions served by Intel Corporation for the '121 Patent in *Memory Integrity LLC v. Intel*

Corporation, (D. Or. filed Nov. 1, 2013), Ex. 2039, and the associated prior art[1]. I understand and am informed that, together, this comprises all prior art of record of the '121 Patent as well as all prior art to the '121 Patent known to the Patent Owner.

8. I have reviewed the art of record and the prior art known to the Patent Owner and it is my opinion that substitute claims 26-34 are patentable over such prior art, even if the Board concludes that the corresponding original claims are unpatentable. No single reference which I have reviewed contains each

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[1] The only qualification to my review of these materials is that, in the invalidity contentions served by Intel Corporation, there are certain documents relating to the Intel 870 Chipset which have not been provided to me, and certain quotes from those documents which have been redacted. I understand that I am not permitted to see those documents because Intel has designated those documents "Confidential Attorneys' Eyes Only" and "Subject to the Prosecution Bar," and because the protective order in the litigation prohibits anyone who sees such materials from being involved in, among other things, participating in advising on new or amended claims. However, I believe I have been able to adequately review and understand the materiality of the Intel 870 Chipset based on other public documentation available regarding that chipset.

limitation of any of the proposed substitute claims, and no combination of such references renders any of the proposed substitute claims obvious.

9. As to the limitations of the original claim 16 of the '121 Patent, it is my opinion that the Pong and Koster references are the closest and most material prior art to those claim limitations and the only references of which I have reviewed which arguably teach probe filtering in a system with processing nodes connected by point-to-point links.[2] As to the Koster reference, I am informed that Koster is not prior art because the substitute claims are entitled to the November 4, 2002 priority date of the '347 Application.

10. As to the Pong reference, Pong itself does not teach any particular cache coherence protocol states and thus does not practice the limitation of the proposed substitute claims that "wherein said states comprise cache coherency states of a cache coherence protocol, and wherein said cache coherence protocol includes at least a modified state, an exclusive state, a shared state, and an invalid

[2] I say arguably because, as set forth in my declaration in support of Patent Owner's responses, I do not believe that Pong or Koster render any claims of the '121 Patent invalid. However, I understand that the Board may disagree with my analysis and that the purpose of these motions is to substitute claims if the Board concludes that the original claims are invalid.

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