

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC., HTC CORPORATION, HTC AMERICA, INC.,
SAMSUNG ELECTRONICS CO. LTD,
SAMSUNG ELECTRONICS AMERICA, INC., AMAZON.COM, INC.,
SONY CORP., SONY ELECTRONICS INC.,
SONY MOBILE COMMUNICATIONS AB,
SONY MOBILE COMMUNICATIONS (USA) INC.,
LG ELECTRONICS, INC., LG ELECTRONICS USA, INC., and
LG ELECTRONICS MOBILECOMM USA, INC.,
Petitioner,

v.

MEMORY INTEGRITY, LLC,
Patent Owner.

Case IPR2015-00159¹
Patent 7,296,121 B2

Before JENNIFER S. BISK, NEIL T. POWELL, and KERRY BEGLEY,
Administrative Patent Judges.

BEGLEY, *Administrative Patent Judge.*

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

¹ Sony Corp., Sony Electronics Inc., Sony Mobile Communications AB, Sony Mobile Communications (USA) Inc., LG Electronics, Inc., LG Electronics USA, Inc., and LG Electronics Mobilecomm USA, Inc., who filed a Petition in IPR2015-01376, have been joined as petitioners in the instant proceeding.

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Apple Inc., HTC Corporation, HTC America, Inc., Samsung Electronics Co. Ltd., Samsung Electronics America, Inc.,² and Amazon.com, Inc. (collectively, “Initial Petitioners”) filed a Petition requesting *inter partes* review of claims 1–3, 8, and 11–25 of U.S. Patent No. 7,296,121 B2 (Ex. 1001, “the ’121 patent”). Pet. Pursuant to 35 U.S.C. § 314(a), we determined the Petition showed a reasonable likelihood that Petitioner would prevail in establishing the unpatentability of claims 1–3, 8, 11, and 15–25, and instituted an *inter partes* review of these claims. Paper 12 (“Inst. Dec.”). We, however, did not institute review of claims 12–14, because we determined the Petition did not show a reasonable likelihood that Petitioner would prevail with respect to these claims. *Id.* at 23–30.

After institution, Sony Corp., Sony Electronics Inc., Sony Mobile Communications AB, Sony Mobile Communications (USA) Inc., LG Electronics, Inc., LG Electronics USA, Inc., and LG Electronics Mobilecomm USA, Inc. (collectively, “Subsequent Petitioners”; and with Initial Petitioners, “Petitioner”) filed a Petition in IPR2015-01376, requesting *inter partes* review of claims 1–3, 8, 11, 12,³ and 15–25 of the

² The Petition also lists Samsung Telecommunications America, LLC (“STA”) as a petitioner. Paper 6 (“Pet.”), 1. After the filing of the Petition, however, STA merged with and into Samsung Electronics America, Inc. Paper 10. Thus, STA no longer exists as a separate corporate entity. *Id.*

³ Subsequent Petitioners represented that they included claim 12 “merely to conform” to the Petition and motion for rehearing of the Institution Decision, regarding claim 12, that was pending before the Board and that if the motion was denied, they requested joinder on “all claims except claim 12.” IPR2015-01376, Paper 3 (“IPR2015-01376 Pet.”), 1 n.1, 33 n.5. Because we denied the motion, we understood Subsequent Petitioners to no longer maintain their challenge of claim 12 and to the extent they did, we determined they had not shown the IPR2015-01376 Petition warranted institution of review of the claim. IPR2015-01376, Paper 12, at 12–15.

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'121 patent on the same grounds as those instituted in this proceeding.

IPR2015-01376 Pet. Subsequent Petitioners also filed a motion for joinder with this proceeding, which we granted. IPR2015-01376, Papers 4, 12.

Patent Owner Memory Integrity, LLC (“Patent Owner”) filed a Patent Owner Response (Paper 25 (“PO Resp.”)) and a Motion to Amend (Paper 26 (“Mot.”)). Petitioner filed a Reply to Patent Owner’s Response (Paper 35, “Reply”) and an Opposition to Patent Owner’s Motion to Amend (Paper 36, “Opp.”). Patent Owner then filed a Reply in support of its Motion to Amend (Paper 37, “Mot. Reply”). Petitioner also filed a Motion for Observations on the deposition testimony of Patent Owner’s expert. Paper 41. An oral hearing was held before the Board. Paper 45 (“Tr.”).

We issue this Final Written Decision pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. Having considered the record before us, we determine Petitioner has shown by a preponderance of the evidence that claims 1–3, 8, and 15–25 of the ’121 patent are unpatentable. *See* 35 U.S.C. § 316(e). Petitioner, however, has not demonstrated by a preponderance of the evidence that claim 11 is unpatentable.

I. BACKGROUND

A. RELATED PROCEEDINGS

The parties indicate Patent Owner has asserted the ’121 patent in numerous cases filed in the U.S. District Court for the District of Delaware. Pet. 1–2; Paper 8, 1–2. In addition, the ’121 patent was the subject of several petitions for *inter partes* review before the Office—IPR2015-00158, IPR2015-00161, IPR2015-00163, IPR2015-00172, and IPR2015-01353. *See* Paper 8, 4; IPR2015-00163, Paper 34. Of these proceedings, only IPR2015-00163 is ongoing and a final written decision in IPR2015-00163 is being issued concurrently with this Decision.

B. THE '121 PATENT

The '121 patent relates to techniques to reduce memory transaction traffic and to improve data access and cache coherency in systems with multiple processors connected using point-to-point links. Ex. 1001, 1:22–25, 2:39–51. The '121 patent explains that cache coherency problems can arise in a system with multiple processors, each with an individual cache memory, because the system may contain multiple copies of the same data. *Id.* at 1:26–45.

The '121 patent discloses a computer system with processing nodes, each with a cache memory, connected by a point-to-point architecture. *Id.* at [57], 2:48–62. The system also includes a “probe filtering unit” that can receive a probe from a processing node. *Id.* at [57], 2:52–65, 5:45–47. The '121 patent defines a probe as “[a] mechanism for eliciting a response from a node to maintain cache coherency in a system.” *Id.* at 5:45–47.

The probe filtering unit then can evaluate the probe based on probe filtering information and transmit the probe to selected processing nodes. *Id.* at [57], 2:52–3:5, 14:50–52; *see id.* at 28:29–58, 29:43–46. The '121 patent explains that probe filtering information is “[a]ny criterion that can be used to reduce the number of clusters or nodes probed.” *Id.* at 14:50–52.

The probe filtering unit also may be operable to accumulate responses from the selected processing nodes and to respond to the node from which the probe originated. *Id.* at 3:5–8, 28:59–67, 29:46–51. Figure 18 of the patent is reproduced below.

Figure 18

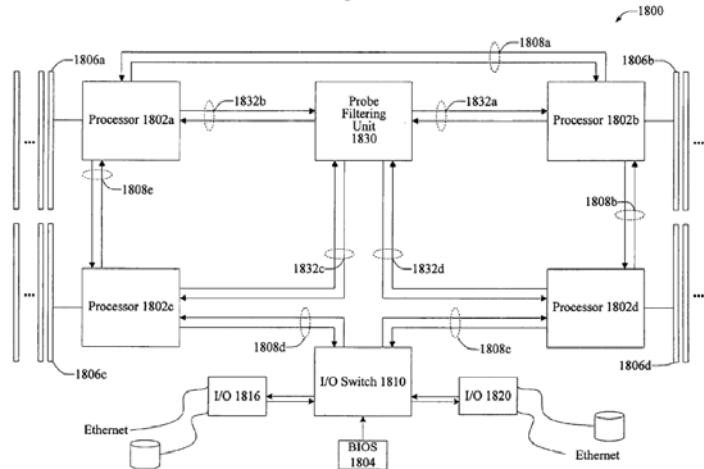


Figure 18 is a diagrammatic representation of a multiple processor system with a probe filtering unit. *Id.* at 3:61–63, 26:58–27:20, Fig. 18. Specifically, Figure 18 depicts multiple processor system 1800 with processing nodes 1802a–d interconnected by point-to-point communication links 1808a–e. *Id.* at 26:58–27:1. System 1800 also includes probe filtering unit 1830. *Id.* at 3:61–63, 26:58–27:20, Fig. 18.

Claims 1, 16, and 25 of the '121 patent are independent claims.

Claim 1 is illustrative of the claimed subject matter and recites:

1. A computer system comprising a plurality of processing nodes interconnected by a first point-to-point architecture, each processing node having a cache memory associated therewith, the computer system further comprising a probe filtering unit which is operable to receive probes corresponding to memory lines from the processing nodes and to transmit the probes only to selected ones of the processing nodes with reference to probe filtering information representative of states associated with selected ones of the cache memories.

Id. at 30:65–31:7 (line breaks added).

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