UNITED STATES PATENT AND TRADEMARK OFFICE BEFORE THE PATENT TRIAL AND APPEAL BOARD APPLE INC., HTC CORPORATION, HTC AMERICA, INC., SAMSUNG ELECTRONICS CO. LTD, SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG TELECOMMUNICATIONS AMERICA, LLC AND AMAZON.COM, INC. **Petitioners** V. MEMORY INTEGRITY, LLC Patent Owner U.S. Patent No. 7,296,121 Inter Partes Review Case No. 2015-00159

MEMORY INTEGRITY, LLC'S PATENT OWNER PRELIMINARY RESPONSE PURSUANT TO 37 CFR § 42.107(a)



# **TABLE OF CONTENTS**

| I.   | INTRODUCTION  |   |   | 1  |  |  |
|------|---|---|---|----|--|--|
| II.  | TEC   | TECHNOLOGY BACKGROUND   |   |    |  |  |
| III. | SUMMARY OF PETITIONERS' PROPOSED GROUND FOR REVIEW  |   |   |    |  |  |
| IV.  |   | THE PENDING PETITIONS FOR <i>INTER PARTES</i> REVIEW OF THE '121 PATENT PRESENT REDUNDANT GROUNDS |   |    |  |  |
| V.   | MEMORY INTEGRITY, LLC'S CLAIM CONSTRUCTIONS10   |   |   |    |  |  |
|      | A.  | "pro  | bbe filtering unit" (claims 1, 16, 25)  | 11 |  |  |
|      | B.  | "sta  | tes associated with selected ones of the cache memories"  | 13 |  |  |
|      |   | 1.  | The claimed "states" refers to cache coherence protocol states  | 14 |  |  |
|      |   | 2.  | A cache coherence protocol state is the current state of a data block in a protocol used to maintain the coherency of caches, in which a data block can only be in one current state at a time, and in which the current state can transition to a different state upon one or more triggering events or conditions |    |  |  |
|      |   | 3.  | "states associated with selected ones of cache memories" refers to the cache coherence protocol state(s) of data block(s) which are <i>stored</i> in the selected cache memories  | 22 |  |  |
|      | C.  |   | cumulate responses to each probe" and "accumulating probe onses" (claims 15 and 25)   | 24 |  |  |
| VI.  | THERE IS NO REASONABLE LIKELIHOOD OF PETITIONERS PREVAILING AS TO A CHALLENGED CLAIM OF THE '121 PATENT |   |   | 25 |  |  |
|      | A.  |   | tioners Failed to Demonstrate That Pong Anticipates Claims 1-3, 1, 12, 15, 16, and 25   |    |  |  |
|      |   | 1.  | Petitioners Improperly Combine Teachings from Distinct<br>Embodiments Within Pong, Which Is Improper for<br>Anticipation Grounds  | 25 |  |  |



| 2. | Petitioners Fail to Demonstrate that Pong Anticipates Any   |  |  |  |
|----|---|--|--|--|
|    | Independent Claim Because Pong's Memory Controller, Which Petitioners Contend is a "Probe Filtering Unit," Does Not Filter "Probes" |  |  |  |
|    | a.  | Petitioners fail to demonstrate that "read requests" in Pong constitute "probes" filtered by the claimed "probe filtering unit"  |  |  |
|    | b.  | Petitioners fail to demonstrate that "write requests" in Pong constitute "probes" filtered by the claimed "probe filtering unit"   |  |  |
|    |   | (1) Petitioners fail to demonstrate that, in Pong's "write update" embodiment, the "write requests" or "write updates" constitute "probes" filtered by the claimed "probe filtering unit"  |  |  |
|    |   | (2) Petitioners fail to demonstrate that, in Pong's "write invalidation" embodiment, the "write requests" or the "write invalidations" constitute "probes" filtered by the claimed "probe filtering unit"                                      |  |  |
| 3. | Inde<br>filte   | tioners Fail to Demonstrate That Pong Anticipates Any ependent Claim Because Pong Does Not Disclose "probe ering information" "representative of states associated with ected ones of the cache memories"                                      |  |  |
|    | a.  | Mere "presence," by itself, does not constitute a cache coherence protocol state   |  |  |
|    | b.  | Pong's "presence bit vector" does not indicate whether a data block is valid   |  |  |
| 4. | 25 I with   | Petitioners Fail to Demonstrate that Pong Anticipates Claim 25 Because Pong Does Not Disclose "evaluating the probe with the probe filtering unit to determine whether a <i>valid</i> copy of the memory line is in any of the cache memories" |  |  |



|     |    | 5. Petitioners Fail to Demonstrate that Pong Anticipates Claims 11 or 12 Because Pong Does Not Disclose "processing nodes" "programmed to complete a memory transaction after receiving a first number of responses to a first probe, the first number being fewer than the number of processing nodes"4 | 18 |
|-----|----|--|----|
|     |    | 6. Petitioners Fail to Demonstrate that Pong Anticipates Claim 15 Because Pong Does not Accumulate Responses   | 0  |
|     | В. | Petitioners Failed To Demonstrate That Claim 13 Is Obvious Over<br>Pong In View of Gaither   | 52 |
|     | C. | Petitioners Failed To Demonstrate That Claim 14 Is Obvious Over<br>Pong In View of Duato   | 54 |
|     | D. | Petitioners Failed To Demonstrate That Claims 17-24 Are Obvious Over Pong In View of Smith   | 8  |
| VII | CO | NCLUSION 5   | (0 |



# **EXHIBIT LIST**

| Exhibit No.           | Description  |
|-----------------------|--|
| Memory Integrity-2001 | Plaintiff Memory Integrity, LLC's Initial Identification |
|                       | of Asserted Claims And Accused Products, served on       |
|                       | Petitioners in Memory Integrity LLC v. Amazon.com        |
|                       | Inc., et al., Nos. 1:13-cv-01795, -01796, -01802,        |
|                       | -01808 (D. Del. served Oct. 13, 2014)                    |
| Memory Integrity-2002 | Excerpts from D. E. Culler, J. P. Singh, and A. Gupta    |
|                       | PARALLEL COMPUTER ARCHITECTURE, pp. 279-280              |
|                       | (1999)   |
| Memory Integrity-2003 | Sorin et al., "Specifying and Verifying a Broadcast and  |
|                       | a Multicast Snooping Cache Coherence Protocol,"          |
|                       | IEEE Transactions on Parallel and Distributed            |
|                       | SYSTEMS, Vol. 13, No. 6, pp. 1-23(June 2002)             |
| Memory Integrity-2004 | Excerpts from Merriam-Webster's Collegiate               |
|                       | Dictionary (10 <sup>th</sup> ed. 1999)                   |
| Memory Integrity-2005 |  |
|                       | Excerpts from David A. Patterson, et al., COMPUTER       |
|                       | Organization and Design (3d ed. 2005)                    |



# DOCKET

# Explore Litigation Insights



Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

# **Real-Time Litigation Alerts**



Keep your litigation team up-to-date with **real-time** alerts and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

### **Advanced Docket Research**



With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

### **Analytics At Your Fingertips**



Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

#### API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

#### **LAW FIRMS**

Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

#### **FINANCIAL INSTITUTIONS**

Litigation and bankruptcy checks for companies and debtors.

#### **E-DISCOVERY AND LEGAL VENDORS**

Sync your system to PACER to automate legal marketing.

