

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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SONY CORPORATION, SONY ELECTRONICS INC.,  
SONY MOBILE COMMUNICATIONS AB, and  
SONY MOBILE COMMUNICATIONS (USA) INC.  
Petitioners,

v.

MEMORY INTEGRITY, LLC,  
Patent Owner.

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Case IPR2015-00158  
Patent 7,296,121 B2

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**SUPPLEMENTAL EXPERT DECLARATION OF  
PROFESSOR DANIEL J. SORIN**

Sony Corporation v. Memory  
Integrity, LLC

**IPR2015 00158  
EXHIBIT**

**Sony-1015**

## **I. INTRODUCTION**

1. I, Professor Daniel J. Sorin, have been retained by counsel for Sony Corporation, Sony Mobile Communications AB, Sony Mobile Communications (USA) Inc., and Sony Electronics Inc. (collectively, “Petitioners”).
2. I submit this declaration in support of Petitioner’s Reply to Patent Owner’s Response to Petition in the *Inter Partes* Review of U.S. Pat. No. 7,296,121, No. IPR2015-00158.

## **II. QUALIFICATIONS**

3. I hold a Ph.D. in Electrical and Computer Engineering from the University of Wisconsin—Madison (awarded in 2002). My doctoral dissertation focused on checkpointing/recovery of multiprocessors with cache-coherent shared memory.
4. I am a Professor in the Department of Electrical and Computer Engineering at Duke University. Prior to being a Professor, I was an Associate Professor in the Department of Electrical and Computer Engineering at Duke University (2009-2015), an Assistant Professor in the Department of Electrical and Computer Engineering at Duke University (2002-2009), a Research Assistant in the Computer Sciences Department at the University of Wisconsin—Madison (1996-2002), and a Teaching Assistant in the

Department of Electrical and Computer Engineering at the University of Wisconsin—Madison (1996-1997).

5. I am the author or co-author of two books: “A Primer on Memory Consistency and Cache Coherence” *Synthesis Lectures on Computer Architecture*, Morgan & Claypool Publishers, 2011; and “Fault Tolerant Computer Architecture” *Synthesis Lectures on Computer Architecture*, Morgan & Claypool Publishers, 2009.
6. I have published over 70 technical articles, including over 20 related to cache coherence technology.
7. I have over 16 years of experience in the design and implementation of cache coherency systems and protocols in multi-processor computer systems.
8. My curriculum vitae more fully describes my education, professional experience, and relevant publications. *See Sony-1014.*

### **III. MATERIALS CONSIDERED**

9. I have reviewed U.S. Pat. No. 7,296,121 (the “’121 Patent”) including its claims.
10. I have reviewed U.S. Patent No. 7,698,509 to Koster (“Koster”). I understand Koster is prior art to at least claims 19–24 of the ’121 Patent.

11. I have reviewed all of the Exhibits entered thus far in IPR2015-00158, including Sony-1001–1014; Memory Integrity-2001–2040; and Exhibit-3001.
12. I have reviewed the Patent Trial and Appeal Board’s (“Board”) Decision in Institution in IPR2015-00158 (Paper No. 7) (“Institution Decision”).
13. I have reviewed the Patent Owner’s Response to Petition in IPR2015-00158 (Paper No. 17) (“Response”).

#### **IV. PERSON OF ORDINARY SKILL IN THE ART**

14. In the 2002–2004 timeframe, a person with ordinary skill in the art with respect to the technology disclosed by the ’121 Patent would have a PhD degree in Electrical Engineering, Computer Engineering, or Computer Science or a MS degree and two to three years of industry experience in the area of cache coherency in multi-processor computer systems.
15. Based upon my education and experience, I consider myself to be a person of at least ordinary skill in the field of technology disclosed by the ’121 Patent. In forming the opinions that I express herein, I have adopted the perspective of a person of ordinary skill in the art, as described in paragraph 14 above.

**V. CLAIM CONSTRUCTION**

16. I understand that in rendering an opinion on claim construction, I am to “interpret claims of an unexpired patent using the broadest reasonable construction in light of the specification of the patent in which they appear.” Institution Decision at 7.
17. In the Institution Decision, with respect to the term “states associated with selected ones of the cache memories” in claim 16 of the ’121 patent, the Board stated that “the term is not limited to cache coherence protocol states and is broad enough to include the condition of presence—i.e., what is stored in cache memory.” Institution Decision at 10. I agree with this construction. A person of ordinary skill in the art would understand the term “states associated with selected ones of the cache memories” to not be limited to cache coherence protocol states, and be broad enough to include the condition of presence—i.e., what is stored in cache memory. In fact, presence information alone (i.e., what is stored in cache memory), is enough information for maintaining coherence in a simple cache coherence protocol.
18. In the Response, with respect to the term “states” in claim 16 of the ’121 patent, the Patent Owner contends that “the appropriate construction of states is limited to cache coherence states, and does not include mere presence.” Response at 2. I disagree with this construction. The

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