Daniel J. Sorin

W.H. Gardner Jr. Associate Professor of Electrical and Computer Engineering

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Research Interests

Multiprocessor computer architectures, with an emphasis on memory system design

Fault tolerant computer architectures

Verification-aware microprocessor design

Architectures for emerging nanotechnologies

Evaluation of system performance and dependability

Education

University of Wisconsin—Madison, Madison, WI

Doctorate of Philosophy in Electrical and Computer Engineering, August 2002

Advisor: David A. Wood

University of Wisconsin—Madison, Madison, WI

Master of Science in Electrical and Computer Engineering, May 1998

Duke University, Durham, NC

Bachelor of Science in Electrical and Computer Engineering, May 1996

Honors and Awards

Best Paper Award at 2014 International Symposium on High-Performance Computer Architecture

Computing Community Consortium's Computing Research Highlight of the Week, February 11-18, 2011 [http://www.cra.org/ccc/rh-detouring.php]

2011 Lois and John L. Imhoff Distinguished Teaching Award

Paper chosen as one of IEEE Micro's Top Picks from Computer Architecture Conferences, 2010

Paper chosen as one of IEEE Micro's Top Picks from Computer Architecture Conferences, 2007

NSF Faculty Early Career Award, 2005

Technology Research News' Top of 2004 list for research performed by nanocomputing research group

Warren Faculty Scholarship, Pratt School of Engineering, Duke University

Outstanding Graduate Research Award, University of Wisconsin Department of Computer Sciences

Intel Foundation Graduate Fellowship

Phi Beta Kappa, Tau Beta Pi, and Eta Kappa Nu academic honor societies

Senior Member of the IEEE

Senior Member of the ACM

Experience

Associate Professor, Duke University, Department of Electrical and Computer Engineering and Department of Computer Science

July 2009-present

Assistant Professor, Duke University, Department of Electrical and Computer Engineering and Department of Computer Science

September 2002-June 2009

Research Assistant, University of Wisconsin—Madison, Computer Sciences Department

August 1996-August 2002

Teaching Assistant, University of Wisconsin—Madison, Dept. of Electrical and Computer Engr.

August 1996-May 1997

Books

1. Daniel J. Sorin, Mark D. Hill, and David A. Wood. "A Primer on Memory Consistency and Cache Coherence." *Synthesis Lectures on Computer Architecture*, Morgan & Claypool Publishers, 2011.

2. Daniel J. Sorin. "Fault Tolerant Computer Architecture." *Synthesis Lectures on Computer Architecture*, Morgan & Claypool Publishers, 2009.

Journal Publications

1. Ralph Nathan and Daniel J. Sorin. "Argus-G: Comprehensive, Low-Cost Error Detection for GPGPU Cores." Accepted for publication in *Computer Architecture Letters,* 2014.

2. Milo M. K. Martin, Mark D. Hill, and Daniel J. Sorin. "Why On-Chip Cache Coherence Is Here to Stay." *Communications of the ACM*, volume 55, number 7, July 2012, pages 78-89.

3. Bogdan F. Romanescu, Alvin R. Lebeck, and Daniel J. Sorin. "Address Translation-Aware Memory Consistency." *IEEE Micro: Micro's Top Picks from Computer Architecture Conferences*, volume 31, number 1, January/February 2011, pages 109-118.

4. Meng Zhang, Alvin R. Lebeck, and Daniel J. Sorin. "Fractal Consistency: Architecting the Memory System to Facilitate Verification." *Computer Architecture Letters*, volume 9, number 2, July-December 2010, pages 61-64.

5. Albert Meixner and Daniel J. Sorin. "Dynamic Verification of Memory Consistency in Cache-Coherent Multithreaded Computer Architectures." *IEEE Transactions on Dependable and Secure Computing (TDSC)*, volume 6, number 1, January-March 2009, pages 18-31.

6. Fred A. Bower, Daniel J. Sorin, and Landon P. Cox. "The Impact of Dynamically Heterogeneous Multicore Processors on Thread Scheduling." *IEEE Micro*, May/June 2008, pages 17-25.

7. Albert Meixner, Michael E. Bauer, and Daniel J. Sorin. "Argus: Low-Cost, Comprehensive Detection of Errors in Simple Cores." *IEEE Micro: Micro's Top Picks from Computer Architecture Conferences*, volume 28, number 1, January/February 2008, pages 52-59.

8. Fred A. Bower, Daniel J. Sorin, and Sule Ozev. "Online Diagnosis of Hard Faults in Microprocessors." *ACM Transactions on Architecture and Code Optimization (TACO)*, volume 4, number 2, June 2007, article 8.

9. Tong Li, Alvin R. Lebeck, and Daniel J. Sorin. "Spin Detection Hardware for Improved Management of Multithreaded Systems." *IEEE Transactions on Parallel and Distributed Systems (TPDS)*, volume 17, number 6, June 2006, pages 508-521.

10. Jaidev P. Patwardhan, Chris Dwyer, Alvin R. Lebeck, and Daniel J. Sorin. "NANA: A Nano-Scale Active Network Architecture." *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, volume 2, number 1, January 2006, pages 1-30.

11. Fred A. Bower, Sule Ozev, and Daniel J. Sorin. "Autonomic Microprocessor Execution via Self-Repairing Arrays." *IEEE Transactions on Dependable and Secure Computing (TDSC)*, volume 2, number 4, October-December 2005, pages 297-310.

12. Chris Dwyer, Alvin R. Lebeck, and Daniel J. Sorin. "Self-Assembled Architecture and the Temporal Aspects of Computing." *IEEE Computer*, volume 38, number 1, January 2005, pages 56-64.

13. Chris Dwyer, Vijeta Johri, Jaidev P. Patwardhan, Alvin R. Lebeck, and Daniel J. Sorin. "Design Tools for Self-assembling Nanoscale Technology", *Institute of Physics Nanotechnology*, volume 15, number 9, September 2004, pages 1240-1245. **[Paper chosen by *Technology Research News* as part of their Top of 2004 list]**

14. Alaa R. Alameldeen, Milo M. K. Martin, Carl J. Mauer, Kevin E. Moore, Min Xu, Daniel J. Sorin, Mark D. Hill, and David A. Wood. "Simulating a $2M Commercial Server on a $2K PC." *IEEE Computer*, volume 36, number 2, February 2003, pages 50-57.

15. Daniel J. Sorin, Jonathan L. Lemon, Derek L. Eager, and Mary K. Vernon. "Analytic Evaluation of Shared-Memory Architectures." *Transactions on Parallel and Distributed Systems (TPDS)*, volume 14, number 2, February 2003, pages 166-180.

16. Daniel J. Sorin, Manoj Plakal, Anne E. Condon, Mark D. Hill, Milo M. K. Martin, and David A. Wood. "Specifying and Verifying a Broadcast and a Multicast Snooping Cache Coherence Protocol." *Transactions on Parallel and Distributed Systems (TPDS)*, volume 13, number 6, June 2002, pages 556-578.

Refereed Conference Publications

1. Ralph Nathan, Bryan Anthonio, Shih-Lien Lu, Helia Naeimi, Daniel J. Sorin, and Xiaobai Sun. "Recycled Error Bits: Energy-Efficient Architectural Support for Floating Point Accuracy." *SC '14*, November 2014.

2. Ralph Nathan and Daniel J. Sorin. "Nostradamus: Low-Cost Hardware-Only Error Detection for Processor Cores." *Design, Automation & Test in Europe (DATE)*, March 2014.

3. Meng Zhang, Jesse D. Bingham, John Erickson, and Daniel J. Sorin. "PVCoherence: Designing Flat Coherence Protocols for Scalable Verification." *0th International Symposium on High Performance Computer Architecture (HPCA)*, February 2014. **[Best Paper Award]**

4. Opeoluwa Matthews, Meng Zhang, and Daniel J. Sorin. "Scalably Verifiable Dynamic Power Management." *20th International Symposium on High Performance Computer Architecture (HPCA)*, February 2014.

5. Kushal Seetharam, Lance Co Ting Keh, Ralph Nathan, and Daniel J. Sorin. "Applying Reduced Precision Arithmetic to Detect Errors in Floating Point Multiplication." *19th IEEE Pacific Rim International Symposium on Dependable Computing (PRDC)*, December 2013.

6. Blake A. Hechtman and Daniel J. Sorin. "Exploring Memory Consistency for Massively-Threaded Throughput-Oriented Processors." *International Symposium on Computer Architecture (ISCA)*, June 2013, pages 201-212.

7. Blake A. Hechtman and Daniel J. Sorin. "Evaluating Cache Coherent Shared Virtual Memory for Heterogeneous Multicore Chips." Extended abstract and poster in the *IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, April 2013, pages 118-119.

8. Adam N. Jacobvitz, A. Robert Calderbank, and Daniel J. Sorin. "Coset Coding to Improve the Lifetime of Memory." *International Symposium on High Performance Computer Architecture (HPCA)*, February, 2013, pages 222-233.

9. Adam N. Jacobvitz, A. Robert Calderbank, and Daniel J. Sorin. "Writing Cosets of a Convolutional Code to Increase the Lifetime of Flash Memory." Invited paper at the *50th Annual Allerton Conference on Communication, Control, and Computing*, October, 2012, pages 308-318.

10. Patrick J. Eibl, Albert Meixner, and Daniel J. Sorin. "An FPGA-Based Experimental Evaluation of Microprocessor Core Error Detection with Argus-2." Poster and 2-page paper at *ACM SIGMETRICS*, June 2011, pages 121-122.

11. Meng Zhang, Alvin R. Lebeck, and Daniel J. Sorin. "Fractal Coherence: Scalably Verifiable Cache Coherence." *43rd International Symposium on Microarchitecture (MICRO)*, December 2010, pages 471-482.

12. Bogdan F. Romanescu, Alvin R. Lebeck, Daniel J. Sorin. "Specifying and Dynamically Verifying Address Translation-Aware Memory Consistency." *15th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, March 2010. **[Selected by IEEE Micro as one of 11 "Top Picks" among all computer architecture conference publications in 2010]**

13. Bogdan F. Romanescu, Alvin R. Lebeck, Daniel J. Sorin, and Anne Bracy. "UNified Instruction/Translation/Data (UNITD) Coherence: One Protocol to Rule Them All." *16th IEEE International Symposium on High-Performance Computer Architecture (HPCA)*, January 2010.

14. Patrick J. Eibl, Daniel J. Sorin, and Andrew D. Cook. "Reduced Precision Checking for a Floating Point Adder." *24th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT)*, October 2009, pages 145-152.

15. Meng Zhang, Anita Lungu, and Daniel J. Sorin. "Analyzing Formal Verification and Testing Efforts of Different Fault Tolerance Mechanisms." *24th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT)*, October 2009, pages 277-285.

16. Anita Lungu, Pradip Bose, Alper Buyuktosunoglu and Daniel J. Sorin. "Dynamic Power Gating with Quality Guarantees." *International Symposium on Low Power Electronics and Design (ISLPED)*, August 2009, pages 377-382.

17. Anita Lungu, Pradip Bose, Daniel Sorin, Steven German and Geert Janssen. "Multicore Power Management: Ensuring Robustness via Early-Stage Formal Verification." *Seventh ACM-IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE)*, July 2009, pages 78-87.

18. Bogdan F. Romanescu and Daniel J. Sorin. "Core Cannibalization Architecture: Improving Lifetime Chip Performance for Multicore Processors in the Presence of Hard Faults." *Seventeenth International Conference on Parallel Architectures and Compilation Techniques (PACT)*, October 2008, pages 43-51.

19. Albert Meixner and Daniel J. Sorin. "Detouring: Translating Software to Circumvent Hard Faults in Simple Cores." *38th Annual International Conference on Dependable Systems and Networks (DSN)*, June 2008, pages 80-89.

20. Bogdan F. Romanescu, Michael E. Bauer, Daniel J. Sorin, and Sule Ozev. "Reducing the Impact of Intra-Core Process Variability with Criticality-Based Resource Allocation and Prefetching." *ACM International Conference on Computing Frontiers*, May 2008, pages 129-138.

21. Albert Meixner, Michael E. Bauer, and Daniel J. Sorin. "Argus: Low-Cost, Comprehensive Detection of Errors in Simple Cores." *40th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO)*, December, 2007, pages 210-222. **[Selected by IEEE Micro as one of 10 "Top Picks" among all computer architecture conference publications in 2007]**

22. Sule Ozev, Daniel J. Sorin, and Mahmut Yilmaz. "Low-Cost Run-time Diagnosis of Hard Delay Faults in the Functional Units of a Microprocessor." *IEEE International Conference on Computer Design (ICCD)*, October 2007, pages 317-324.

23. Mahmut Yilmaz, Albert Meixner, Sule Ozev, and Daniel J. Sorin. "Lazy Error Detection for Microprocessor Functional Units." *IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT)*, September 2007, pages 361-369.

24. Anita Lungu and Daniel J. Sorin. "Verification-Aware Microprocessor Design." *Sixteenth International Conference on Parallel Architectures and Compilation Techniques (PACT)*, September 2007, pages 83-93.

25. Albert Meixner and Daniel J. Sorin. "Error Detection Using Dynamic Dataflow Verification." *Sixteenth International Conference on Parallel Architectures and Compilation Techniques (PACT)*, September 2007, pages 104-115.

26. Bogdan F. Romanescu, Michael E. Bauer, Daniel J. Sorin, and Sule Ozev. "Reducing the Impact of Process Variability with Prefetching and Criticality-Based Resource Allocation." Poster and extended abstract in *Sixteenth International Conference on Parallel Architectures and Compilation Techniques (PACT)*, September 2007, page 424.

27. Albert Meixner and Daniel J. Sorin. "Unified Microprocessor Core Storage." *ACM Conference on Computing Frontiers*, May 2007, pages 23-34.

28. Albert Meixner and Daniel J. Sorin. "Error Detection via Online Checking of Cache Coherence with Token Coherence Signatures." *13th International Symposium on High Performance Computer Architecture (HPCA),* February, 2007, pages 145-156.

29. Mahmut Yilmaz, Derek R. Hower, Sule Ozev, and Daniel J. Sorin. "Self-Detecting and Self-Diagnosing 32-bit Microprocessor Multiplier." *International Test Conference (ITC)*, October 2006.

30. Nathan N. Sadler and Daniel J. Sorin. "Choosing an Error Protection Scheme for a Microprocessor's L1 Data Cache." *International Conference on Computer Design (ICCD)*, October 2006, pages 499-505.

31. Albert Meixner and Daniel J. Sorin. "Dynamic Verification of Memory Consistency in Cache-Coherent Multithreaded Computer Architectures." *International Conference on Dependable Systems and Networks (DSN)*, June 2006, pages 73-82.

32. Fred A. Bower, Derek R. Hower, Mahmut Yilmaz, Daniel J. Sorin, and Sule Ozev. "Applying Architectural Vulnerability Analysis to Hard Faults in the Microprocessor." Poster and 2-page paper at *ACM SIGMETRICS*, June 2006, pages 375-376.

33. Fred A. Bower, Daniel J. Sorin, and Sule Ozev. "A Mechanism for Online Diagnosis of Hard Faults in Microprocessors." *38th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO)*, November 2005, pages 197-208.

34. Albert Meixner and Daniel J. Sorin. "Dynamic Verification of Sequential Consistency." *32nd Annual International Symposium on Computer Architecture (ISCA)*, June 2005, pages 482-493.

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