UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SONY CORPORATION; SONY MOBILE COMMUNICATIONS AB; SONY MOBILE COMMUNICATIONS (USA) INC; AND SONY ELECTRONICS INC.
Petitioner

Patent No. 7,296,121
Issue Date: Nov. 13, 2007
Title: REDUCING PROBE TRAFFIC IN MULTIPROCESSOR SYSTEMS

EXPERT DECLARATION OF PROFESSOR DANIEL J. SORIN

No. IPR2015-158

I. INTRODUCTION

1. I, Professor Daniel J. Sorin, have been retained by counsel for Sony Corporation, Sony Mobile Communications AB, Sony Mobile Communications (USA) Inc., and Sony Electronics Inc. (collectively, "Sony").

2. I submit this declaration in support of Sony's Petition for *Inter Partes* Review of U.S. Pat. No. 7,296,121, No. IPR2015-158.

II. QUALIFICATIONS

3. I hold a Ph.D. in Electrical and Computer Engineering from the University of Wisconsin—Madison (awarded in 2002). My doctoral dissertation focused on checkpointing/recovery of multiprocessors with cache-coherent shared memory.

4. I am an Associate Professor in the Department of Electrical and Computer Engineering at Duke University. Prior to being an Associate Professor, I was an Assistant Professor in the Department of Electrical and Computer Engineering at Duke University (2002-2009), a Research Assistant in the Computer Sciences Department at the University of Wisconsin—Madison (1996-2002), and a Teaching Assistant in the Department of Electrical and Computer Engineering at the University of Wisconsin—Madison (1996-1997).

5. I am the author or co-author of two books: "A Primer on Memory Consistency and Cache Coherence" *Synthesis Lectures on Computer Architecture*, Morgan & Claypool Publishers, 2011; and "Fault Tolerant Computer Architecture" *Synthesis Lectures on Computer Architecture*, Morgan & Claypool Publishers, 2009.

6. I have published over 70 technical articles, including over 20 related to cache coherence technology.

7. I have over 16 years of experience in the design and implementation of cache coherency systems and protocols in multi-processor computer systems.

8. My curriculum vitae more fully describes my education, professional experience, and relevant publications. *See* Sony-1014.

III. MATERIALS CONSIDERED

9. I have reviewed U.S. Pat. No. 7,296,121 (the "'121 Patent") including its claims.

10. I have reviewed U.S. Patent No. 7,698,509 to Koster ("Koster"). I understand Koster is prior art to the '121 Patent.

11. I have reviewed Jeffrey Kuskin, et al., *The Stanford FLASH Multiprocessor*, PROCEEDINGS ON THE 21ST ANNUAL INTERNATIONAL SYMPOSIUM ON

COMPUTER ARCHITECTURE, IEEE (1994) ("Kuskin"). I understand Kuskin is prior art to the '121 Patent.

12. I have reviewed S. Park et al., *Verification of Cache Coherence Protocols by Aggregation of Distributed Transactions*, THEORY OF COMPUTING SYSTEMS 31 (1998) ("Park"). I understand Park is prior art to the '121 Patent.

13. I have reviewed U.S. Patent No. 6,088,769 to Luick ("Luick"). I understand Luick is prior art to the '121 Patent.

14. I have reviewed U.S. Pat. Pub. No. 2002/0073261 ("Kosaraju"). I understand Kosaraju is prior art to the '121 Patent.

IV. PERSON OF ORDINARY SKILL IN THE ART

15. Generally, the '121 Patent is in the field cache coherency in multi-processor computer systems.

16. I understand that the focus of this *Inter Partes* Review is the subject matter of claims 1-3, 8, 11-12, and 14-25 of the '121 Patent. Generally, these claims describe a "probe filtering unit" ("PFU") which increases the efficiency of memory transactions in a point-to-point multi-processor computer system having multiple cache memories. The claims further describe how the PFU receives probes from processing nodes corresponding to memory lines, and how the PFU transmits the probes only to selected ones of the processing nodes with references to probe

filtering information representative of states associated with selected ones of the cache memories.

17. In the 2002–2004 timeframe, a person with ordinary skill in the art with respect to the technology disclosed by the '121 Patent would have a PhD degree in Electrical Engineering, Computer Engineering, or Computer Science or a MS degree and two to three years of industry experience in the area of cache coherency in multi-processor computer systems.

18. Based upon my education and experience, I consider myself to be a person of at least ordinary skill in the field of technology disclosed by the '121 Patent.

V. KOSTER

19. Koster describes a point-to-point multi-processor architecture with a "snoop filter" having a "shadow tag memory" that stores the tags of data stored in the local cache memories of several microprocessors. By having the shadow tag memory, the snoop filter forwards a received broadcast for requested data (by one microprocessor) to a specific other microprocessor only if the shadow tag memory indicates that the other microprocessor has a copy of the requested data.

20. At the time Koster was filed (July 13, 2004), it would have been obvious to one of ordinary skill in the art to implement the "snoop filter" disclosed in

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