UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SONY CORPORATION; SONY ELECTRONICS INC.;
SONY MOBILE COMMUNICATIONS AB; AND
SONY MOBILE COMMUNICATIONS (USA) INC.
Petitioners

v.

MEMORY INTEGRITY, LLC
Patent Owner

U.S. Patent No. 7,296,121

Inter Partes Review Case No. 2015-00158

**MEMORY INTEGRITY, LLC'S APPENDIX OF CLAIMS
IN SUPPORT OF ITS MOTION TO AMEND [37 CFR § 42.121(b)]**

**LISTING OF PROPOSED SUBSTITUTE CLAIMS TO
U.S. PATENT NO. 7,296,121**

26-28: intentionally left blank

29 (contingent proposed substitute claim for claim 19 if Board determines claim 19 is unpatentable):

At least one computer-readable medium having data structures stored therein representative of a probe filtering unit for use in a computer system comprising a plurality of processing nodes interconnected by a first point-to-point architecture, each processing node having a cache memory associated therewith, the probe filtering unit being operable to receive probes corresponding to memory lines from the processing nodes and to transmit the probes only to selected ones of the processing nodes with reference to probe filtering information representative of states associated with selected ones of the cache memories, wherein said states comprise cache coherency states of a cache coherence protocol, and wherein said cache coherence protocol includes at least a modified state, an exclusive state, a shared state, and an invalid state, and wherein said probe filtering unit is coupled to a coherent protocol interface and a non-coherent protocol interface.

30 (contingent proposed substitute claim for claim 20 if Board determines claim 20 is unpatentable):

At least one computer-readable medium having data structures stored therein representative of a probe filtering unit for use in a computer system comprising a plurality of processing nodes interconnected by a first point-to-point architecture, each processing node having a cache memory associated therewith, the probe filtering unit being operable to receive probes corresponding to memory lines from the processing nodes and to transmit the probes only to selected ones of the

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processing nodes with reference to probe filtering information representative of states associated with selected ones of the cache memories, wherein said data structures comprise a simulatable representation of the probe filtering unit, wherein said states comprise cache coherency states of a cache coherence protocol, and wherein said cache coherence protocol includes at least a modified state, an exclusive state, a shared state, and an invalid state, and wherein said probe filtering unit is coupled to a coherent protocol interface and a non-coherent protocol interface.

31 (contingent proposed substitute claim for claim 21 if Board determines claim 21 is unpatentable):

At least one computer-readable medium having data structures stored therein representative of a probe filtering unit for use in a computer system comprising a plurality of processing nodes interconnected by a first point-to-point architecture, each processing node having a cache memory associated therewith, the probe filtering unit being operable to receive probes corresponding to memory lines from the processing nodes and to transmit the probes only to selected ones of the processing nodes with reference to probe filtering information representative of states associated with selected ones of the cache memories, wherein the data structures comprise a simulatable representation of the probe filtering unit, wherein said simulatable representation comprises a netlist, wherein said states comprise cache coherency states of a cache coherence protocol, and wherein said cache coherence protocol includes at least a modified state, an exclusive state, a shared state, and an invalid state, and wherein said probe filtering unit is coupled to a coherent protocol interface and a non-coherent protocol interface.

32 (contingent proposed substitute claim for claim 22 if Board determines claim 22 is unpatentable):

At least one computer-readable medium having data structures stored therein representative of a probe filtering unit for use in a computer system comprising a plurality of processing nodes interconnected by a first point-to-point architecture, each processing node having a cache memory associated therewith, the probe filtering unit being operable to receive probes corresponding to memory lines from the processing nodes and to transmit the probes only to selected ones of the processing nodes with reference to probe filtering information representative of states associated with selected ones of the cache memories, wherein the data structures comprise a code description of the probe filtering unit, wherein said states comprise cache coherency states of a cache coherence protocol, and wherein said cache coherence protocol includes at least a modified state, an exclusive state, a shared state, and an invalid state, and wherein said probe filtering unit is coupled to a coherent protocol interface and a non-coherent protocol interface.

33 (contingent proposed substitute claim for claim 23 if Board determines claim 23 is unpatentable):

At least one computer-readable medium having data structures stored therein representative of a probe filtering unit for use in a computer system comprising a plurality of processing nodes interconnected by a first point-to-point architecture, each processing node having a cache memory associated therewith, the probe filtering unit being operable to receive probes corresponding to memory lines from the processing nodes and to transmit the probes only to selected ones of the processing nodes with reference to probe filtering information representative of states associated with selected ones of the cache memories, wherein said data

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structures comprise a code description of the probe filtering unit, wherein said code description corresponds to a hardware description language, wherein said states comprise cache coherency states of a cache coherence protocol, and wherein said cache coherence protocol includes at least a modified state, an exclusive state, a shared state, and an invalid state, and wherein said probe filtering unit is coupled to a coherent protocol interface and a non-coherent protocol interface.

34 (contingent proposed substitute claim for claim 24 if Board determines claim 24 is unpatentable):

A set of semiconductor processing masks representative of at least a portion of a probe filtering unit for use in a computer system comprising a plurality of processing nodes interconnected by a first point-to-point architecture, each processing node having a cache memory associated therewith, the probe filtering unit being operable to receive probes corresponding to memory lines from the processing nodes and to transmit the probes only to selected ones of the processing nodes with reference to probe filtering information representative of states associated with selected ones of the cache memories, wherein said states comprise cache coherency states of a cache coherence protocol, and wherein said cache coherence protocol includes at least a modified state, an exclusive state, a shared state, and an invalid state, and wherein said probe filtering unit is coupled to a coherent protocol interface and a non-coherent protocol interface.

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