UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of:	Morton et al.	Case Nos. IPR2015-00158
U.S. Patent No.	7,296,121	IPR2015-00159
Issue Date:	Nov. 13, 2007	IPR2015-00163
Appl. Serial No.:	10/966,161	
Filing Date:	Oct. 15, 2004	

Title: REDUCING PROBE TRAFFIC IN MULTIPROCESSOR SYSTEMS

DECLARATION OF VOJIN OKLOBDZIJA, Ph.D. IN SUPPORT OF PATENT OWNER'S RESPONSES PURSUANT TO 37 C.F.R. § 42.120

I, Vojin Oklobdzija,, hereby declare as follows:

1. My name is Dr. Vojin Oklobdzija. I submit this declaration in support of Patent Owner's Responses in IPR2015-00158, -00159, and -00163. I have been asked to offer technical opinions relating to U.S. Patent No. 7,296,121 and the alleged prior art and arguments presented by the Petitioners on the grounds which were instituted, and the reasoning of the Board in the decisions on institution.

2. I received a Dipl. Ing. (equivalent to a Master's in Electrical Engineering in the U.S.) degree in Telecommunications and Electronics in 1971 from the University of Belgrade, Yugoslavia, followed by a Master's in Computer Science from the University of California, Los Angeles in 1978. I received a Ph.D. in Computer Science with a minor in Electronics from the University of California, Los Angeles in 1982.

3. Following my Ph.D. graduation, I spent 9 years at IBM's T.J. Watson Research Center working on microprocessor architecture, development and design. In my career at IBM, I worked on the early development of RISC (Reduced

Instruction Set Architecture Computer) architecture and development of a new processor generation for IBM. Most notably, I worked on the first commercial RISC computer, IBM ROMP, as well as the first super-scalar microprocessor, IBM RS/6000.

4. After leaving IBM, I have held a faculty (Full Professor) position at the University of California, Davis; and visiting positions at the University of California, Berkeley; Sydney University in Australia; EPFL in Switzerland; and others. I have over 20 years of teaching experience, teaching courses in: Computer Architecture, Computer Design, Digital Design, VLSI Circuits as well as advanced post-graduate courses in Computer Architecture and Design. During this time, I served as a consultant with members of the microprocessor industry extensively and was a principal architect in the Siemens/Infineon TriCore processor.

5. After retiring from the academia, I returned back to industry. In 2013, I became a Senior Director of Microprocessor Development at Skyera Inc., a startup company that was subsequently acquired by Hitachi Ltd. While working at Skyera, I lead a team developing an on-chip processor array consisting of a grid or 256 processors, including development of its cache-coherency mechanism and its fast cache memory hierarchy.

6. Currently I am President and CTO of my own startup company, Silicon Analytics Inc. and I also work as a consultant. I am a named inventor on 15 issued U.S. Patents and a similar number of international patents. I have also

authored several books on microprocessor design, including a book titled "Computer Engineering Handbook," published by CRC Press in 2001, which won the CHOICE Outstanding Academic Title Award for 2002, as well as "High Performance Energy Efficient Microprocessor Design" published Springer in 2006. I have attached a true and correct copy of my curriculum vitae as Exhibit 2017, which further sets forth my qualifications.

7. I have reviewed and am familiar with the content of U.S. Patent No. 7,296,121 ("the '121 Patent"). Additionally, I have reviewed all of the prior art which provides the basis for the grounds on which the Board has instituted proceedings in IPR2015-00158, -00159, and -00163, including U.S. Patent Application Publication Number 2002/0053004 to Pong ("Pong"), U.S. Patent No. 7,698,509 to Koster et al. ("Koster"), Jeffrey Kuskin, et al., The Stanford FLASH Multiprocessor, PROCEEDINGS ON THE 21ST ANNUAL INTERNATIONAL SYMPOSIUM ON COMPUTER ARCHITECTURE, IEEE (1994) ("Kuskin"), Michael John Sebastian Smith, APPLICATION-SPECIFIC INTEGRATED CIRCUITS (1997) ("Smith"), and U.S. Patent No. 7,315,919 to O'Krafka et al. ("O'Krafka"). I have also reviewed various other documents which are discussed later herein. I have reviewed these and the other materials from the perspective of one of ordinary skill in the art of the '121 Patent at the time of the '121 Patent's November 4, 2002 effective filing date.

8. I agree with the opinion of Dr. Horst in IPR2015-00159 and -00163, Ex. 1014 ("Horst Decl.") ¶ 8, that one of ordinary skill in the field of cache

coherency as of November 4, 2002 would have a at least a bachelor's degree in electrical engineering, computer engineering, or computer science, and at least two years of experience in the design of multiprocessor systems.

9. I have no financial interest in either party or in the outcome of this proceeding. I am being paid for my work as an expert in these matters on an hourly basis. My compensation is not dependent on the outcome of these proceedings or the content of my opinions. My opinions, as explained below, are based on my education, experience, and background in the fields discussed above, and my review of the materials cited by Petitioners, and the other materials discussed herein.

10. This declaration is organized as follows:

I. Terminology in the claims of the '121 Patent (page 4);

II. Opinions regarding Koster and the Koster combinations (IPR2015-00158 and -00163) (page 22);

III. Opinions regarding Pong and the Pong combinations (IPR2015-00159) (page 34).

I. THE LANGUAGE OF THE CLAIMS OF THE '121 PATENT

A. "States"

11. The term "states" is recited in independent claims 1 and 16 of the '121 Patent as part of the longer phrase "probe filtering information representative of states associated with selected ones of the cache memories." The term "states" is also recited in independent claim 25 in the similar phrase "probe filtering

information . . . representative of states associated with selected ones of the cache memories."

12. Dr. Horst, in IPR2015-00159 and -00163, Ex. 1014 ("Horst Decl."), opines that "states associated with selected ones of the cache memories' would be broad enough to cover 'any modes or conditions of selected ones of the cache memories.'" Horst Decl. ¶ 30. In particular, Dr. Horst opines that "the '121 patent does not limit the term 'state' to a specific type of state, such as standard coherence protocol states." *Id.* ¶ 31. Dr. Horst also points to a definition in the Merriam Webster dictionary, a general purpose dictionary, of state as a "mode or condition of being."

13. I also understand that the Board, in its decisions on institution in IPR2015-00158, -00159, -00163 determined that "state" was not limited to "cache coherence protocol states." Although the Board did not adopt an express construction of the term "state," it held that "the term is not limited to cache coherence protocol states and is broad enough to include the condition of presence—i.e., what is stored in cache memory." *E.g.*, IPR2015-00163, Paper No. 18 at 12.

14. It is my opinion that the constructions adopted by Dr. Horst and the Board are inconsistent with the broadest reasonable construction of the term "state" in the claims of the '121 Patent from the perspective of one of ordinary skill in the art informed by the specification and teachings of the patent. In particular, by not construing "state" as cache coherency states, Dr. Horst and the Board divorce the

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