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Paper 35
Entered: May 19, 2016

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SONY CORPORATION, SONY ELECTRONICS INC.,
SONY MOBILE COMMUNICATIONS AB, and
SONY MOBILE COMMUNICATIONS (USA) INC.,
Petitioner,

v.

MEMORY INTEGRITY, LLC,
Patent Owner.

Case IPR2015-00158
Patent 7,296,121 B2

Before JENNIFER S. BISK, NEIL T. POWELL, and KERRY BEGLEY, *Administrative Patent Judges.*

POWELL, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

A. Background

Sony Corporation, Sony Electronics Inc., Sony Mobile Communications AB, and Sony Mobile Communications (USA) Inc. (collectively, "Petitioner") filed a Petition requesting an *inter partes* review of claims 1–3, 8, 11, 12, and 14–25 (the "challenged claims") of U.S. Patent No. 7,296,121 B2 (Ex. 1001, "the '121 patent"). Paper 1 ("Pet."). On May 21, 2015, we instituted a review (Paper 7, "Institution Decision" or "Inst. Dec.") based upon Petitioner's assertion that claims 19–24 are unpatentable under 35 U.S.C. § 103. Inst. Dec. 35.

This is a Final Written Decision under 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons set forth below, Petitioner has shown by a preponderance of the evidence that claims 19–24 are unpatentable.

B. Related Matters

The parties indicate that the '121 patent is the subject of several proceedings in the United States District Court for the District of Delaware. Pet. 1; Paper 4, 1–2. In addition, other petitions seeking *inter partes* review of the '121 patent have been filed, including IPR2015-00159, IPR2015-00161, IPR2015-00163, IPR2015-00172, IPR2015-01353, and IPR2015-1376. Of these other proceedings at the Office, only IPR2015-00159 and IPR2015-00163 are ongoing.[1]

[1] IPR2015-01353 was terminated and the petitioner in that case was joined to IPR2015-00163. Similarly, IPR2015-01376 was terminated and the petitioner in that case was joined to IPR2015-00159.

C. The Pending Grounds of Unpatentability

We instituted *inter partes* review involving the following grounds of unpatentability:

Ground	Reference(s)	Challenged Claims
§ 103	Koster[2]	24
§ 103	Koster and Kuskin[3]	19–23

Petitioner supports its challenge with declarations executed by Dr. Daniel J. Sorin on November 3, 2014 (Ex. 1013) and on November 28, 2015 (Ex. 1015). Patent Owner relies on a declaration executed by Dr. Vojin Oklobdzija on August 11, 2015 (Ex. 2016).

D. The '121 Patent

The '121 patent relates to accessing data in computer systems that include more than one processor. Ex. 1001, 1:23–24. Specifically, the '121 patent discusses multiple processor systems with a point-to-point architecture—a cluster of individual processors (also referred to as processing nodes) that are directly connected to each other through point-to-point links, each with an associated cache memory. *Id.* at 4:38–40. To increase the number of available processors, multiple clusters may be connected. *Id.* at 4:50–53. Figure 1A is reproduced below.

[2] U.S. Patent No. 7,698,509 B1 (Ex. 1005) ("Koster").
[3] Jeffrey Kuskin et al., *The Stanford FLASH Multiprocessor*, *in* PROCEEDINGS OF THE 21ST ANNUAL INTERNATIONAL SYMPOSIUM ON COMPUTER ARCHITECTURE 302 (1994) (Ex. 1006, "Kuskin").

Figure 1A

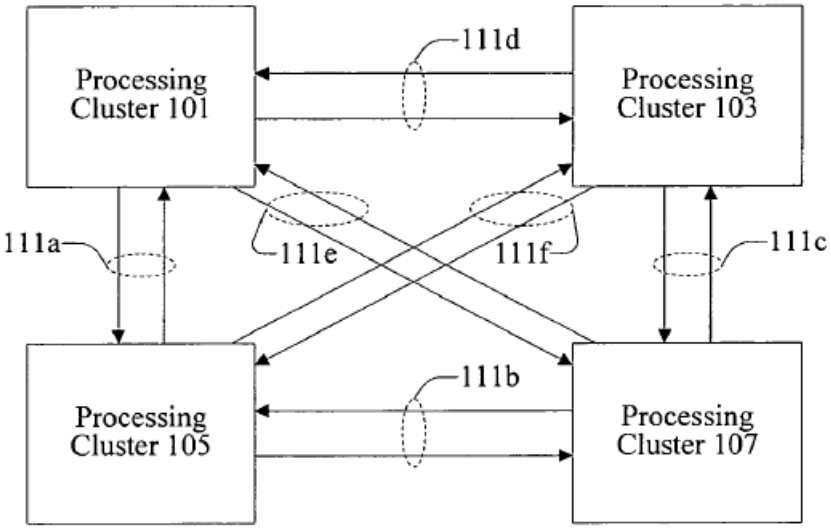

Figure 1A shows an example of a multiple cluster, multiple processor system described by the '121 patent. *Id.* at 6:10–12. Figure 1A includes four processing clusters: 101, 103, 105, and 107, each of which can, in turn, include multiple processors. *Id.* at 6:12–14. The clusters are connected through point-to-point links 111a–f. *Id.* at 6:14–16.

The '121 patent explains that cache coherency problems can arise in such a system, because it may contain multiple copies of the same data. *Id.* at 1:26–38. For example, if the caches of two different processors have a copy of the same data block and both processors "attempt to write new values into the data block at the same time," then the two caches may have different data values and the system may be "unable to determine what value to write through to system memory." *Id.* at 1:37–45. Solutions to cache coherency problems often involve an increase in communication traffic and a resulting decrease in efficiency. *Id.* at 1:23–26, 2:46–48. The '121 patent

discloses "techniques . . . for increasing data access efficiency in a multiple processor system," while also addressing cache coherency. *Id.* at 4:36–38.

The system disclosed by the '121 patent includes a probe filtering unit. *Id.* at 2:52–65. A probe is defined as "[a] mechanism for eliciting a response from a node to maintain cache coherency in a system." *Id.* at 5:45–47. As opposed to a traditional approach of broadcasting probes to all nodes, the probe filtering unit reduces traffic by intercepting the probes and transmitting them only to those nodes that require the information based on probe filtering information, i.e., "[a]ny criterion that can be used to reduce the number of clusters or nodes probed." *Id.* at 2:52–3:5, 14:50–52; *see id.* at 28:29–58, 29:43–46. The probe filtering unit may also accumulate responses from those nodes selected to receive the probes and respond to the node from which the probe originated. *Id.* at 3:5–8, 28:59–67, 29:46–51. Figure 18 of the '121 patent is reproduced below.

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