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set, and disallow the others in the set, from being active or valid. For example, masking an interrupt.

(2) for semiconductor manufacturing, a device used to selectively block photolithographic exposure of sensitized coating used for preventing a subsequent etching process from removing material. A mask is analogous to a negative in conventional photography.

(3) a glass or quartz plate containing information (encoded as a variation in transmittance and/or phase) about the features to be printed. Also called a photomask or a reticle.

mask aligner a tool that aligns a photomask to a resist-coated wafer and then exposes the pattern of the photomask into the resist.

mask biasing the process of changing the size or shape of the mask feature in order for the printed feature size to more closely match the nominal or desired feature size.

mask blank a blank mask substrate (e.g., quartz) coated with an absorber (e.g., chrome), and sometimes with resist, and used to make a mask.

mask linearity the relationship of printed resist feature width to mask feature width for a given process.

mask programming programming a semiconductor read-only-memory (ROM) by modifying one or more of the masks used in the semiconductor manufacturing process.

mask set consists of the dozen or so (varies with process and company) individual masks that are required to complete a MMIC wafer fabrication from start to finish. Examples of masks or mask levels are "first level metal" (defines all the primary metal structure on the circuit), "capacitor top plate" (defines the pattern for the metal used to form the top plate of MIM capacitors), and "dielectric etch" (defines areas where dielectric (insulator) material will be removed after coating the entire wafer with it).

maskable interrupt interrupt that can be postponed to permit a higher-priority interrupt by setting mask bits in a control register. *See also* nonmaskable interrupt.

mass storage a storage for large amounts of data.

massively parallel architecture a computer system architecture characterized by the presence of large numbers of CPUs that can execute instructions in parallel. The largest examples can process thousands of instructions in parallel, and provide efficient pathways to pass data from one CPU to another.

massively parallel processor a system that employs a large number, typically 1000 or more, of processors operating in parallel.

master the system component responsible for controlling a number of others (called slaves).

master boot record a record of the disk containing the first code and table that are loaded at the bootstrap of the computer. It is read even before the partition table sector.

master control relay (MCR) used in programmable logic controllers to secure entire programs, or just certain rungs of a program. An MCR will override any timer condition, whether it be time-on or time-off, and place all contacts in the program to a safe position whenever conditions warrant.

master copy in coherence protocols, the copy of the object that is guaranteed to hold the "correct" contents for the object. Coherence protocols can be designed around the tagging of master copies. The master copy can be read (rather then

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