

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

HUGHES NETWORK SYSTEMS, LLC and
HUGHES COMMUNICATIONS, INC.,
Petitioner,

v.

CALIFORNIA INSTITUTE OF TECHNOLOGY,
Patent Owner.

Case IPR2015-00067
Patent 7,116,710 B1

Before KALYAN K. DESHPANDE, GLENN J. PERRY, and
TREVOR M. JEFFERSON, *Administrative Patent Judges*.

JEFFERSON, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

Hughes Network Systems, LLC and Hughes Communications, Inc. (collectively, “Petitioner”) filed a Corrected Petition requesting an *inter partes* review of claims 1, 3, 4, 5, 6, 15, 16, 20, 21, and 22 of U.S. Patent No. 7,116,710 B1 (Ex. 1001, “the ’710 patent”). Paper 4 (“Pet.”). California Institute of Technology (“Patent Owner”) timely filed a Preliminary Response. Paper 13 (“Prelim. Resp.”). We have jurisdiction under 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted “unless . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” After considering the Petition, the Preliminary Response, and associated evidence, we conclude that Petitioner has not demonstrated a reasonable likelihood that it would prevail in showing unpatentability of all the challenged claims. Thus, we deny institution of an *inter partes* review of claims 1, 3, 4, 5, 6, 15, 16, 20, 21, and 22 of the ’710 patent.

A. Related Proceedings

Petitioner indicates that the ’710 patent is the subject of the proceedings in *California Institute of Technology v. Hughes Communications, Inc.*, No. 13-cv-07245 (C.D. Cal.). Pet. 1–2.

The ’710 patent is also the subject of IPR2015-00068. Additionally, Petitioner indicates that the ’710 patent is related to U.S. Patent No. 7,421,032, U.S. Patent No. 7,916,781, and U.S. Patent No. 8,284,833, which are the subject of IPR2015-00059, IPR2015-00060, IPR2015-00061, and IPR2015-00081. Paper 7, 1–2.

B. The '710 Patent

The '710 patent describes the serial concatenation of interleaved convolutional codes forming turbo-like codes. Ex. 1001, Title. It explains some of the prior art with reference to its Fig. 1, reproduced below.

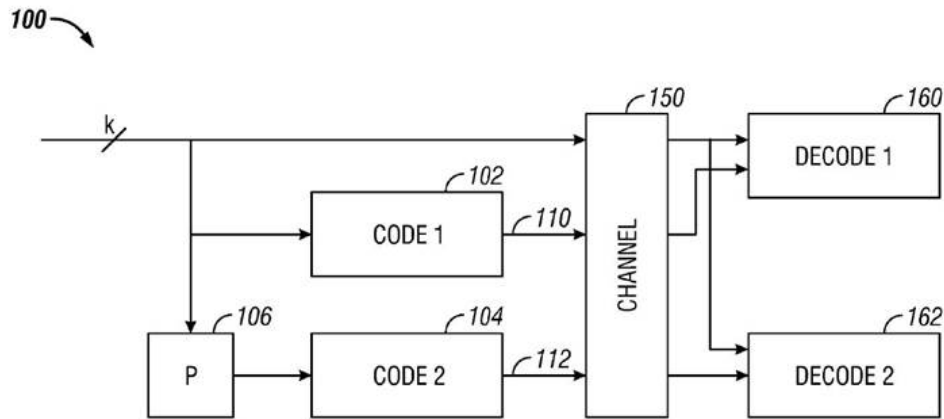


FIG. 1
(Prior Art)

Figure 1 is a schematic diagram of a prior “turbo code” system. *Id.* at 2:14–15. The '710 patent specification describes Figure 1 as follows:

A standard turbo coder 100 is shown in FIG. 1. A block of k information bits is input directly to a first coder 102. A k bit interleaver 106 also receives the k bits and interleaves them prior to applying them to a second coder 104. The second coder produces an output that has more bits than its input, that is, it is a coder with rate that is less than 1. The coders 102,104 are typically recursive convolutional coders.

Three different items are sent over the channel 150: the original k bits, first encoded bits 110, and second encoded bits 112. At the decoding end, two decoders are used: a first constituent decoder 160 and a second constituent decoder 162. Each receives both the original k bits, and one of the encoded portions 110, 112. Each decoder sends likelihood estimates of the decoded bits to the other decoders. The estimates are used to decode the uncoded information bits as corrupted by the noisy channel.

Id. at 1:38–53(emphasis omitted).

A coder 200, according to a first embodiment of the invention, is described with respect to Figure 2, reproduced below.

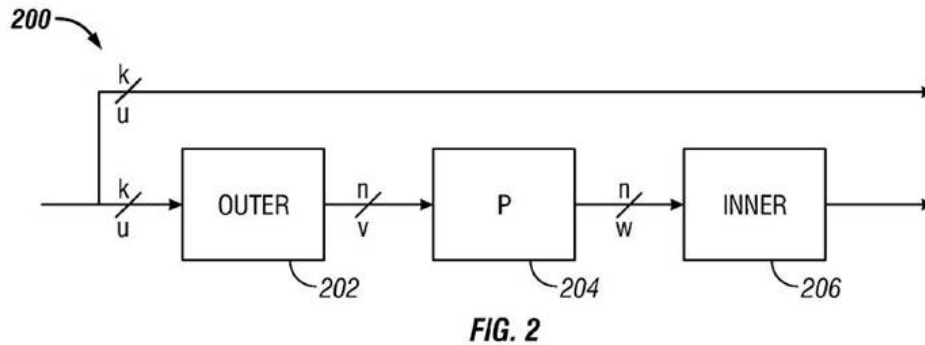


Figure 2 of the '710 patent is a schematic diagram of coder 200. *Id.* at 2:16–17.

The specification states that “coder 200 may include an outer coder 202, an interleaver 204, and inner coder 206.” *Id.* at 2:34–35. It further states as follows.

The outer coder 202 receives uncoded data. The data may be partitioned into blocks of fixed size, say k bits. The outer coder may be an (n,k) binary linear block coder, where $n > k$. The coder accepts as input a block u of k data bits and produces an output block v of n data bits. The mathematical relationship between u and v is $v = T_0 u$, where T_0 is an $n \times k$ matrix, and the rate¹ of the coder is k/n .

The rate of the coder may be irregular, that is, the value of T_0 is not constant, and may differ for sub-blocks of bits in the data block. In an embodiment, the outer coder 202 is a repeater that repeats the k bits in a block a number of times q to produce a block with n bits, where $n = qk$. Since the repeater has an irregular output, different bits in the block may be repeated a

¹ The “rate” of an encoder refers to the ratio of the number of input bits to the number of resulting encoded output bits related to those input bits. See Ex. 1010 ¶ 19.

different number of times. For example, a fraction of the bits in the block may be repeated two times, a fraction of bits may be repeated three times, and the remainder of bits may be repeated four times. These fractions define a degree sequence, or degree profile, of the code.

The inner coder 206 may be a linear rate-1 coder, which means that then-bit output block x can be written as $x=T_1w$, where T_1 is a nonsingular $n \times n$ matrix. The inner coder 210 can have a rate that is close to 1, e.g., within 50%, more preferably 10% and perhaps even more preferably within 1% of 1.

Id. at 2:41–64 (emphasis omitted and footnote added). Codes characterized by a regular repeat of message bits into a resulting codeword are referred to as “regular repeat,” whereas codes characterized by irregular repeat of message bits into a resulting codeword are referred to as “irregular repeat.” The second (“inner”) encoder 206 performs an “accumulate” function. Thus, the two step encoding process illustrated in Fig. 2, including a first encoding (“outer encoding”) followed by a second encoding (“inner encoding”), results in either a “regular repeat accumulate” (“RRA”) code or an “irregular repeat accumulate (“IRA”) code, depending upon whether the repetition in the first encoding is regular or irregular.

Figure 4 of the '710 patent, reproduced below, shows an alternative embodiment in which the first encoding is carried out by a low density generator matrix.

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