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IPR2015-00060; Paper 18
Entered: April 27, 2015

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

HUGHES NETWORK SYSTEMS, LLC and
HUGHES COMMUNICATIONS, INC.,
Petitioner,

v.

CALIFORNIA INSTITUTE OF TECHNOLOGY,
Patent Owner.

Case IPR2015-00060
Patent 7,421,032 B2

Before KALYAN K. DESHPANDE, GLENN J. PERRY, and
TREVOR M. JEFFERSON, *Administrative Patent Judges*.

PERRY, *Administrative Patent Judge*.

DECISION
Denying *Inter Partes* Review
37 C.F.R. § 42.108

INTRODUCTION

A. Background

Hughes Network Systems, LLC and Hughes Communications, Inc. (collectively "Petitioner") filed a Petition to institute an *inter partes* review of claims 1, 8, 10, 18, 19, and 22 of U.S. Patent No. 7,421,032 B2 ("the '032 patent"). Paper 4 ("Pet.").[1] California Institute of Technology ("Patent Owner") timely filed a Preliminary Response. Paper 13 ("Prelim. Resp."). We have jurisdiction under 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted "unless . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." For the reasons given below, we do not institute an *inter partes* review in this proceeding.

B. Related Proceedings

Petitioner states that the '032 Patent (Ex. 1005) is involved in a pending lawsuit titled *California Institute of Technology v. Hughes Communications, Inc.*, No. 13-CV-07245 (CACD) ("the Lawsuit"). *See* Ex. 1015. The Lawsuit includes the following patents: (i) U.S. Patent No. 7,116,710; (ii) U.S. Patent No. 7,421,032; (iii) U.S. Patent No. 7,916,781; and (iv) U.S. Patent No. 8,284,833.

The '032 patent belongs to a patent family also including U.S. Patent No. 7,116,710, U.S. Patent No. 7,916,781, and U.S. Patent No. 8,284,833, which are the subject of related proceedings including IPR2015-00059, IPR2015-00061, IPR2015-00067, IPR2015-00068, and IPR2015-00081.

[1] "Pet." refers to the corrected petition filed October 30, 2014 (Paper 4).

THE ’032 PATENT (Ex. 1003)

A. Background and Context

We understand that error correcting codes are used to communicate information across a noisy communication channel. They enable the recovery of a transmitted message that has become distorted by channel noise. To prepare a message for transmission, it is parsed into groups of message bits that are “encoded” into “codewords” by adding redundant information to them.[2] The codewords are transmitted over the communication channel and are received at another location, where the codewords are “decoded” into the original message. No single coding scheme is optimal for all communication channels. Also, there are design tradeoffs between the use of complex codes, which permits better error correction, and less complex codes, which are easier to decode. This has led to the development of many different encoding/decoding schemes. The ’781 patent describes one such scheme.

B. The ’032 Patent Invention

The ’032 patent describes the serial concatenation of interleaved convolutional codes forming turbo-like codes. Ex. 1003, Title. It explains some of the prior art with reference to its Figure 1, reproduced below.

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[2] For example, input message bits “10011” may be encoded into a codeword “100111” by adding a “parity” bit “1” to the original message.

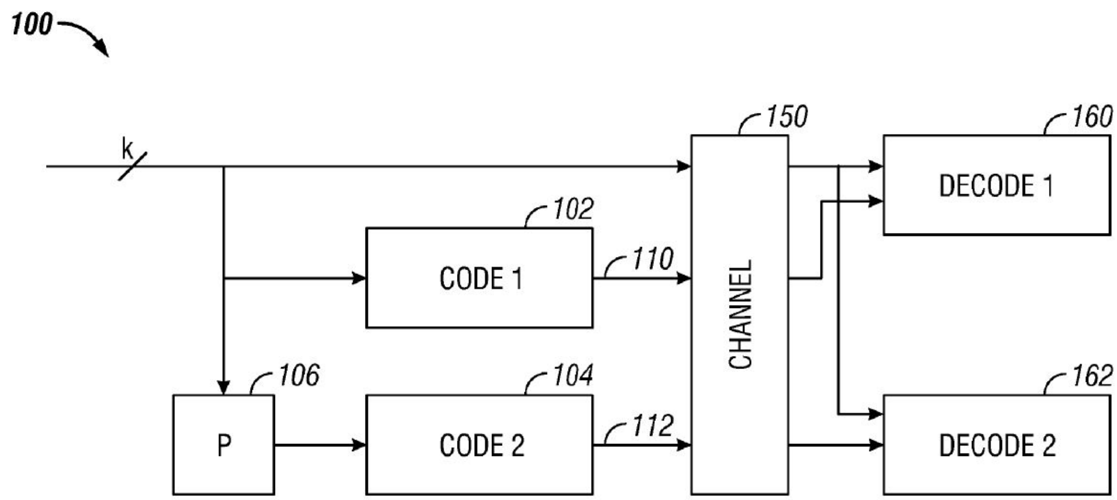

FIG. 1
(Prior Art)

Fig. 1 is a schematic diagram of a prior "turbo code" system. Ex. 1003, 2:16–17. The '032 patent specification describes Figure 1 as follows:

> A block of k information bits is input directly to a first coder 102. A k bit interleaver 106 also receives the k bits and interleaves them prior to applying them to a second coder 104. The second coder produces an output that has more bits than its input, that is, it is a coder with rate that is less than 1. The coders 102, 104 are typically recursive convolutional coders.
>
> Three different items are sent over the channel 150: the original k bits, first encoded bits 110, and second encoded bits 112. At the decoding end, two decoders are used: a first constituent decoder 160 and a second constituent decoder 162. Each receives both the original k bits, and one of the encoded portions 110, 112. Each decoder sends likelihood estimates of the decoded bits to the other decoders. The estimates are used to decode the uncoded information bits as corrupted by the noisy channel.

Ex. 1003, 1:41–56. A coder 200, according to a first embodiment of the invention, is described with respect to Figure 2, reproduced below.

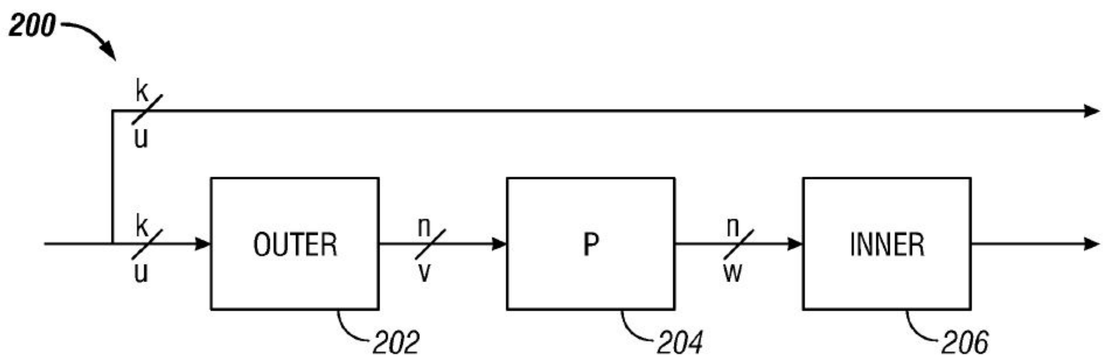

FIG. 2

Figure 2 is a schematic diagram of a coder according to an embodiment.

> The coder 200 may include an outer coder 202, an interleaver 204, and inner coder 206. . . . The outer coder 202 receives the uncoded data [that] may be partitioned into blocks of fixed size, [e.g.] k bits. The outer coder may be an (n,k) binary linear block coder, where n>k. The coder accepts as input a block u of k data bits and produces an output block v of n data bits. The mathematical relationship between u and v is $v=T_0u$, where T_0 is an n x k matrix, and the rate[3] of the coder is k/n.
>
> The rate of the coder may be irregular, that is, the value of T_0 is not constant, and may differ for sub-blocks of bits in the data block. In an embodiment, the outer coder 202 is a repeater that repeats the k bits in a block a number of times q to produce a block with n bits, where n=qk. Since the repeater has an irregular output, different bits in the block may be repeated a different number of times. For example, a fraction of the bits in the block may be repeated two times, a fraction of bits may be repeated three times, and the remainder of bits may be repeated four times. These fractions define a degree sequence or degree profile, of the code.
>
> The inner coder 206 may be a linear rate-1 coder, which means that the n-bit output block x can be written as $x=T_iw$, where T_i is a nonsingular n x n matrix. The inner coder 210 can have a

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[3] The "rate" of an encoder refers to the ratio of the number of input bits to the number of resulting encoded output bits related to those input bits. Ex. 1010 ¶ 19.

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