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**UNITED STATES DISTRICT COURT  
CENTRAL DISTRICT OF CALIFORNIA  
WESTERN DIVISION**

The CALIFORNIA INSTITUTE OF  
TECHNOLOGY,

Plaintiff,

v.

HUGHES COMMUNICATIONS  
INC., HUGHES NETWORK  
SYSTEMS LLC, DISH NETWORK  
CORPORATION, DISH NETWORK  
L.L.C., and DISHNET SATELLITE  
BROADBAND L.L.C.,

Defendants.

Case No. 2:13-cv-07245-MRP-JEM

**ORDER GRANTING IN PART  
AND DENYING IN PART  
DEFENDANTS' MOTION FOR  
SUMMARY JUDGMENT**

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## I. Introduction

Plaintiff California Institute of Technology (“Caltech”) has asserted U.S. Patent Nos. 7,116,710 (“the ’710 patent”), 7,421,032 (“the ’032 patent”), 7,916,781 (“the ’781 patent”), and 8,284,833 (“the ’833 patent,”) against Defendants Hughes Communications, Inc., Hughes Network Systems, LLC, DISH Network Corporation, DISH Network L.L.C., and dishNET Satellite Broadband L.L.C. (collectively, “Hughes”). The Court issued a claim construction order on August 6, 2014. *See Cal. Inst. of Tech. v. Hughes Commc’ns Inc.*, 35 F. Supp. 3d 1176 (C.D. Cal. 2014). The Court denied Hughes’ motion for summary judgment for ineligibility under 35 U.S.C. § 101 on November 3, 2014. *See Cal. Inst. of Tech. v. Hughes Commc’ns Inc.*, No. 2:13-cv-07245, 2014 WL 5661290 (C.D. Cal. Nov. 3, 2014). Hughes now moves for summary judgment of: invalidity of the patents-in-suit on a variety of theories; non-infringement by DISH and dishNET products; and invalidity of Caltech’s damages theory.<sup>1</sup> The Court grants Hughes’ motion as to damages and DISH; the Court denies Hughes’ motion as to the other issues.

## II. Background

17 The asserted claims are method and apparatus claims relating to error  
18 correction.<sup>2</sup> In modern electronic systems, data are stored in the form of bits  
19 having the value “1” or “0.” During data transmission, a random or irregular  
20 fluctuation (known as noise) can occur in the signal and corrupt data. For  
21 example, a transmitter may send a bit with the value “1,” but noise may corrupt  
22 this bit and cause the receiver to read the value as “0.” To mitigate this problem,  
23 electronic systems use error correction. Error correction depends on redundancy,  
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25  
26 <sup>1</sup> Additionally, Hughes also addresses Caltech’s doctrine of equivalents argument. This Court has already barred the introduction of this argument. Therefore, this Order will not discuss Hughes’ objections on this matter.

27  
28 <sup>2</sup> All four patents share a common specification and claim priority to the same patent application U.S. Serial Application No. 09/861,102.

1 which refers to “extra” bits that may be duplicates of original information bits<sup>3</sup> and  
2 are transmitted along with the original bits. These extra bits are not necessary, in  
3 the sense that the original information exists without them, but they serve an  
4 important purpose. Using these extra bits, the receiver can ensure that the original  
5 information bits were not corrupted during transmission.

6 Caltech’s patents are directed to a form of error correction code called an  
7 irregular repeat and accumulate (“IRA”) code. An IRA code operates as follows:  
8 the code can introduce redundancy by repeating (i.e., duplicating) different original  
9 bits irregularly (i.e., a different number of times). These information bits may then  
10 be randomly permuted and combined to form intermediate bits, which are  
11 accumulated to form parity bits. Parity bits reflect the values of a selection of  
12 original information bits. These parity bits are transmitted along with the original  
13 information bits. The receiver ensures that the received original information bits  
14 were not corrupted during transmission. It can do this by modulo-2 adding the  
15 original information bits and parity bits.<sup>4</sup> The receiver knows whether this sum is  
16 supposed to be odd or even. If the sum is supposed to be odd but is instead even,  
17 the receiver will know that an error occurred and can perhaps correct the error  
18 using other information it has received.

19 The benefit of an IRA code is that not all bits are repeated the same number of  
20 times. The repetition of certain bits provides redundancy. Although greater  
21 repetition of every bit would allow for better error correction, it would also force  
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25 <sup>3</sup> The ’032 patent uses the term “message bits” rather than “information bits.” This  
26 Court will generally use the term “information bits” when discussing error  
27 correction.

28 <sup>4</sup> For an explanation of mod-2 arithmetic, see *Modular Arithmetic – An  
Introduction*, Rutgers University,  
<http://www.math.rutgers.edu/~erowland/modulararithmetic.html>.

1 the transmitter to send more bits, decreasing the coding rate and increasing data  
2 transfer time.<sup>5</sup> IRA codes balance competing goals: data accuracy and efficiency.  
3 The asserted claims recite generally encoding and decoding bits in accordance with  
4 an IRA code.

### 5 **III. Standard for Summary Judgment**

6 The Court shall grant summary judgment if there is no genuine dispute as to  
7 any material fact, as supported by facts on the record that would be admissible in  
8 evidence, and if the moving party is entitled to judgment as a matter of law. Fed.  
9 R. Civ. P. 56; *Celotex Corp. v. Catrett*, 477 U.S. 317, 322 (1986); *Anderson v.*  
10 *Liberty Lobby, Inc.*, 477 U.S. 242, 250 (1986). In order to grant summary  
11 judgment, the Court must identify material facts by reference to the governing  
12 substantive law, while disregarding irrelevant or unnecessary factual disputes.  
13 *Anderson*, 477 U.S. at 248. If there is any genuine dispute about a material fact  
14 such that a reasonable jury could return a verdict for the nonmoving party,  
15 summary judgment cannot be granted. *Id.* The Court must view facts and draw  
16 reasonable inferences in favor of the nonmoving party. *Scott v. Harris*, 550 U.S.  
17 372, 378 (2007). If the party moving for summary judgment does not bear the  
18 burden of proof as to a particular material fact, the moving party need only give  
19 notice of the absence of a genuine issue of material fact so that the nonmoving  
20 party may come forward with all of its evidence. *See Celotex*, 477 U.S. at 325.

### 21 **IV. Discussion**

#### 22 **A. Invalidity of '781 patent in View of Divsalar Reference**

23 Hughes argues that the '781 patent is invalid in view of a conference  
24 proceeding, "Coding Theorems for 'Turbo-Like' Codes" ("Divsalar").  
25 Specifically, Hughes argues that independent claim 19 is anticipated by Divsalar  
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27 <sup>5</sup> Coding rate is calculated through the following equation: Coding Rate =  
28 (Original information bits) / (Original information bits + Extra bits). The closer  
the coding rate is to 1, the more efficient it is.

1 and dependent claim 16 is anticipated by and obvious in light of Divsalar. This  
2 Court finds Hughes' argument unpersuasive as to claim 16 and undeveloped as to  
3 claim 19.

4 Divsalar concerns RA codes. It describes an encoder that receives a block of  
5 data, including information bits, and performs an encoding operation using these  
6 information bits in its input. The information bits are repeated and reordered, then  
7 encoded by a rate 1 accumulator. Finally, the encoding operation generates a  
8 codeword.

9 Hughes argues that Divsalar discloses each and every element of claim 19 of  
10 the '781 patent. Claim 19 reads:

11 A method of encoding a signal, comprising:

12 receiving a block of data in the signal to be encoded, the block of data  
13 including information bits; and

14 performing an encoding operation using the information bits as an  
15 input, the encoding operation including an accumulation of mod-2 or  
16 exclusive-OR sums of bits in subsets of the information bits, the encoding  
17 operation generating at least a portion of a codeword, wherein at least two of  
18 the information bits appear in three subsets of the information bits.

19 Further Hughes argues that Divsalar renders obvious claim 16, which ultimately  
20 depends on independent claim 13:

21 A method of encoding a signal, comprising:

22 receiving a block of data in the signal to be encoded, the block of data  
23 including information bits; and

24 performing an encoding operation using the information bits as an  
25 input, the encoding operation including an accumulation of mod-2 or  
26 exclusive-OR sums of bits in subsets of the information bits, the encoding  
27 operation generating at least a portion of a codeword,  
28 wherein the information bits appear in a variable number of subsets.

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