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THE INSTITUTION OF ELECTRICAL ENGINEERS

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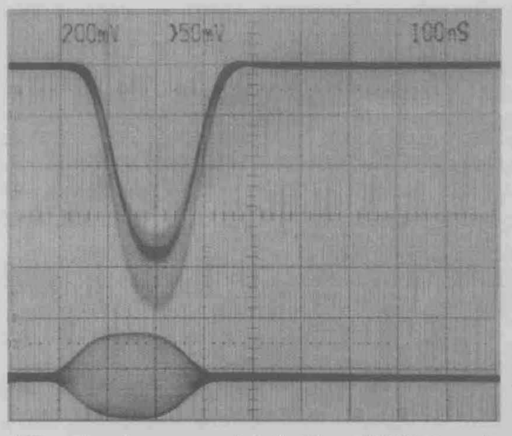
wavelet dilation could be implemented. The half bandwidths of the bandpass filters and their centre frequency spacings are about 650kHz.

Fig. 3 shows the time-frequency plot for a (slowly) frequency-swept input signal. In Fig. 3, where black represents the peak output voltage for each channel, there is good frequency discrimination as the input frequency sweeps over the frequency range of the filter bank. Fig. 4 shows the time-domain response of a single 0.5µm CMOS channel to a $100 mV_{pp}$, 300ns burst at 47MHz.



a

b

Fig. 4 *Time-domain response of single 0.5µm CMOS channel*

a Output signal (200mV/div)
b Input signal (50mV/div)

The order of the lowpass filter in the synchronous receiver determines the bandpass filter characteristic. A single-pole lowpass filter design is easily converted to a two-pole design by adding a capacitor across the differential outputs of the multiplier that drives the lowpass filter. The two-pole lowpass filter design has much steeper skirts, and hence better separation of signals with different frequencies. In Fig. 3, the bandpass filter shape corresponds to the two-pole lowpass filter design.

Since increasing the number of channels can be used to increase system performance, size and power dissipation constraints are important for a continuous wavelet transform circuit. For the 2µm design, the channels were laid out on a 150µm pitch with under 100mW power dissipation per channel and a maximum operating frequency of 50MHz. For the 0.5µm design, the channels were laid out on a 56µm pitch with under 40mW power dissipation per channel and a maximum operating frequency in excess of 100MHz. The total size of the 16-channel 2µm chip was 4750µm by 3100m.

The VCO design is particularly critical, since the VCO needs to have a constant, frequency-independent output voltage, and also needs to be tunable over as large a frequency range as possible. Our VCO design uses diodes to set the output amplitude, triode MOSFET resistors to change the oscillation frequency, and bias current adjustment slaved to the triode resistor setting to compensate for the change in loop gain associated with changing the triode resistor values.

To prevent drifts in the VCO frequencies with changes in temperature, phase-locked loops and external frequency references can be used, as shown in Fig. 1. Where the VCO voltage-frequency characteristic is linear, many VCOs can be biased using a pair of PLLs along with a resistive voltage divider. The PLLs have been successfully implemented, but not yet combined with the continuous wavelet transform circuit. We have demonstrated a 0.5µm CMOS PLL tunable from 64MHz to 77MHz.

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Apparent power transducer for three-phase three-wire system

S. Kusui and M. Kogane

In a newly developed transducer apparent power is measured by using a multiplier, in which the AC component of the output is used. For a three-phase three-wire system, two multipliers are used according to the so-called 'two wattmeter' method. The AC output components are +30° and –30° phase-shifted, respectively, and then the difference is converted to a DC signal which corresponds to the total apparent power.

Introduction: Measurement of electrical apparent power is sometimes necessary in order to take into account the power factor as well as the energy in in the case of large consumers. Various apparent power meters have been developed [1 – 6] using such methods as multiplication of the RMS values of the voltage and the current, or taking the root of the squared sum of the active and reactive powers. An apparent power meter which directly uses the above definition is complicated because RMS AC/DC converters or a reactive power meter and computer are needed.

The authors have noticed that the amplitude of the AC component of the multiplication of the insantaneous voltage and current equals the RMS volt-ampere which is the apparent power. This idea is applied to an apparent power transducer for the three-phase three-wire system which is very popular in Japan. The conventional method needs four multipliers (two for the active power transducer and two for the reactive power transducer) and a calculator to obtain the root of the squared sum of the active and reactive powers. However, the new method needs only two multipliers. Furthermore, if necessary, the active power is easily measured at the same time using the same multipliers. Therefore the configuration is very simple and the cost is very low.

Principle and configuration: Fig. 1 shows the conventional apparent power transducer for a three-phase three-wire system. 1, 2 and 3 are powerlines; L is the load. M_{P1} and M_{P2} are the active power transducers whose outputs P_1 and P_2 are summed by Σ_P to obtain the total power signal P. M_{Q1} and M_{Q2} are the reactive power transducers whose outputs Q_1 and Q_2 are summed by Σ_Q to obtain

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