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United States Patent [19]

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Takeuchi et al.

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[54] **SEMICONDUCTOR MEMORY DEVICE HAVING A PLURALITY OF MEMORY CELL TRANSISTORS ARRANGED TO CONSTITUTE MEMORY CELL ARRAYS**

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[57] ABSTRACT

[21] Appl. No.: **09/008,627**

The semiconductor memory device comprises first and second memory cell rows each constructed by connecting a plurality of memory cell transistors, and third and fourth memory cell rows which are provided to be respectively adjacent to the first and second memory cell rows, such that element separation regions are respectively provided between adjacent memory cell rows. First and second transistors are connected between a drain or a source of the first memory cell row and a drain or a source of the second memory cell row. Gate electrodes of the first and third transistors are connected by a first gate line, and gate electrodes of the second and fourth transistors are connected by a second gate line. The first and second transistors are connected to a data line by a first contact. The third and fourth transistors are connected to a data line by a second contact. A first spacing element is connected between the first and second transistors and a second spacing element is connected between the third and fourth transistors, so that the distance between the first and second contacts is widened. The first contact is provided between the first transistor and the first spacing element. The second contact is provided between the fourth transistor and the second spacing element. The first spacing element is connected through the third gate line to the second spacing element.

[22] Filed: **Jan. 16, 1998**

[30] Foreign Application Priority Data

Jan. 20, 1997 [JP] Japan 9-007262

[51] Int. Cl.⁷ **H01L 29/708**; H01L 21/336; G11C 16/04

[52] U.S. Cl. **257/315**; 365/185.17; 438/258

[58] Field of Search 257/315; 365/185.17; 438/258

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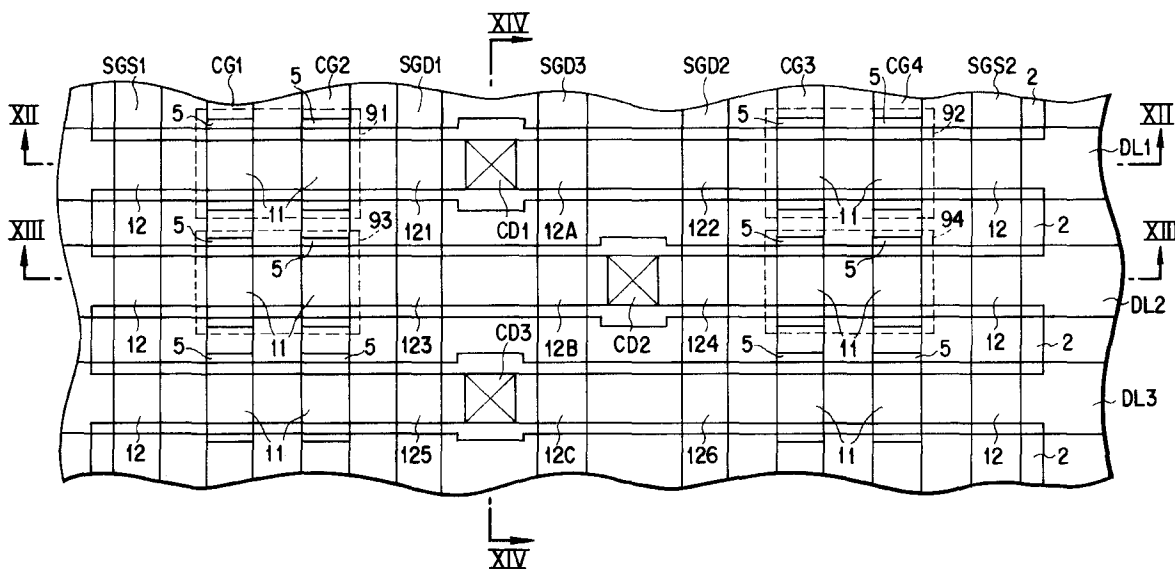
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20 Claims, 31 Drawing Sheets



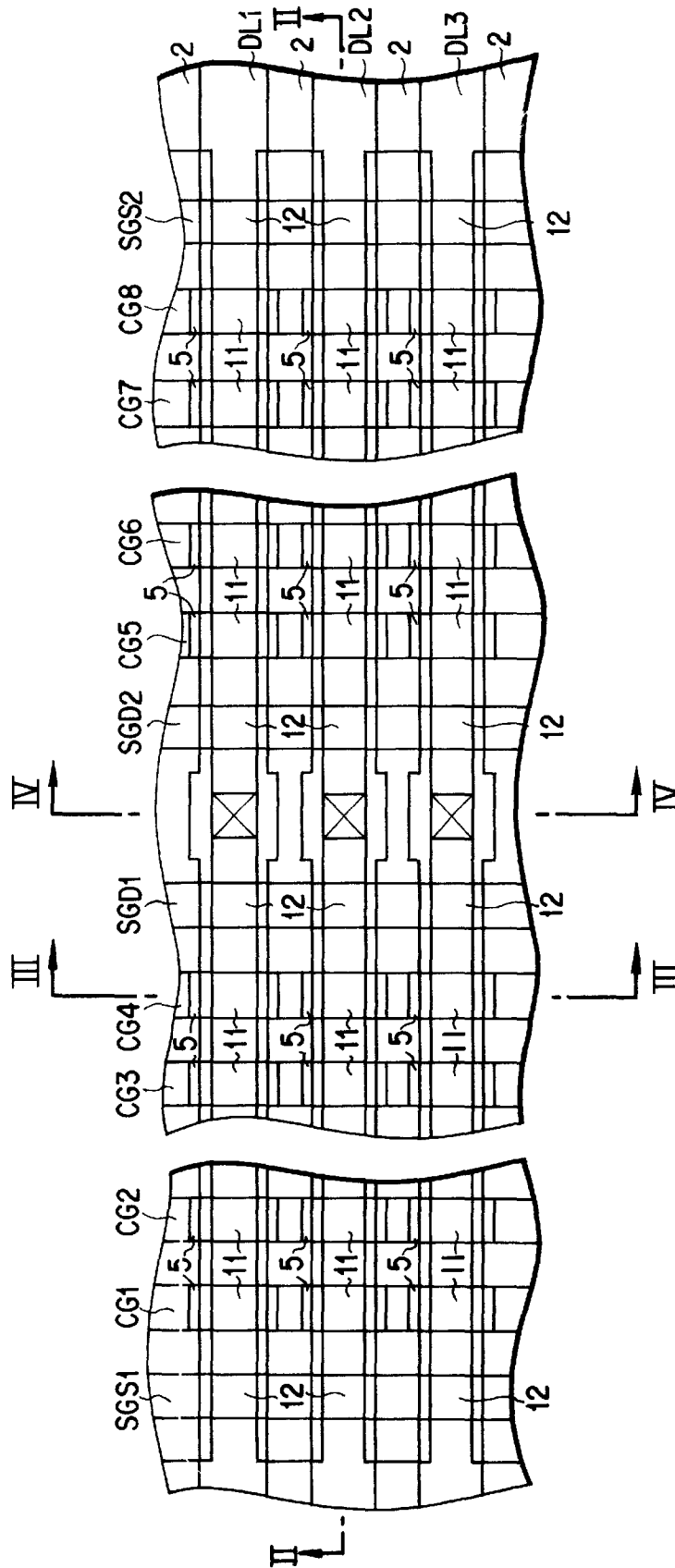
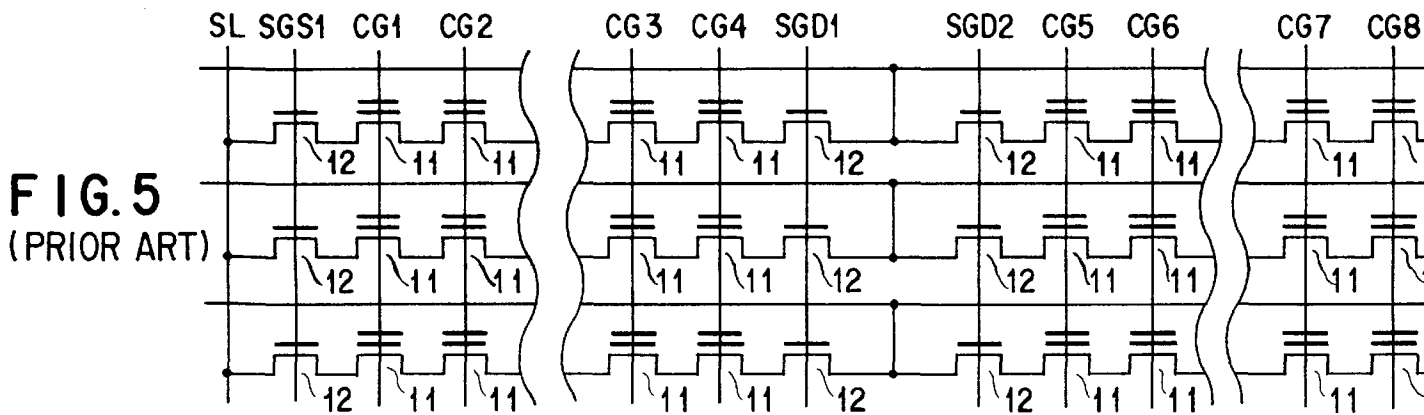
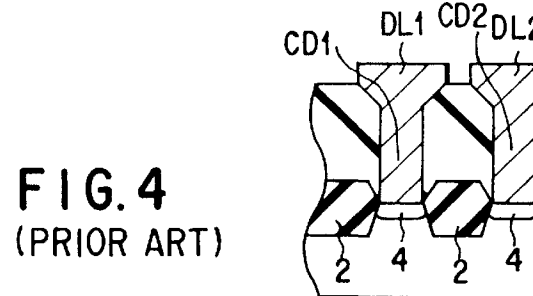
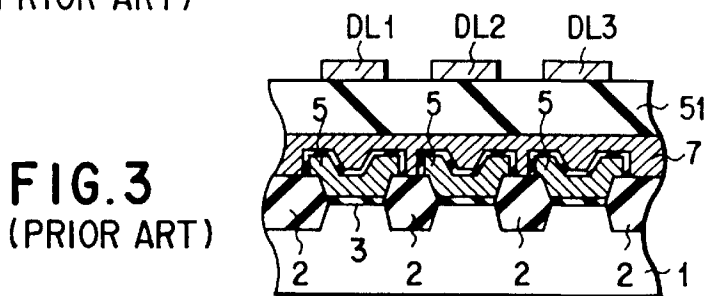
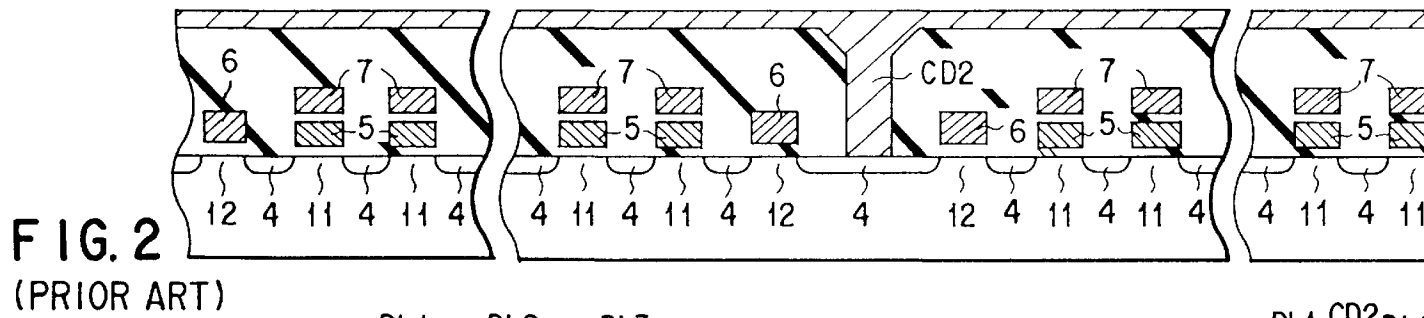


FIG. 1 (PRIOR ART)



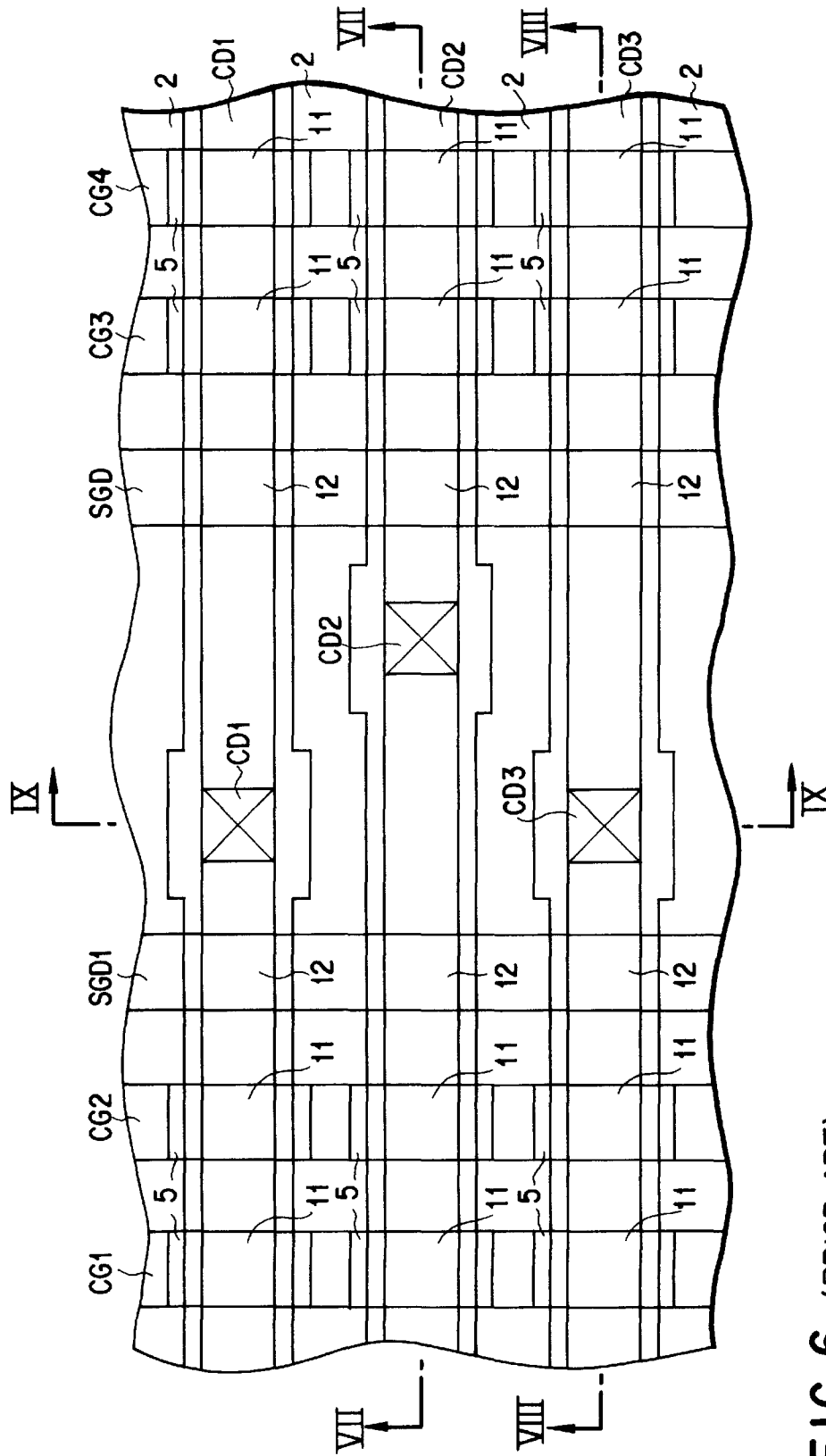


FIG. 6 (PRIOR ART)

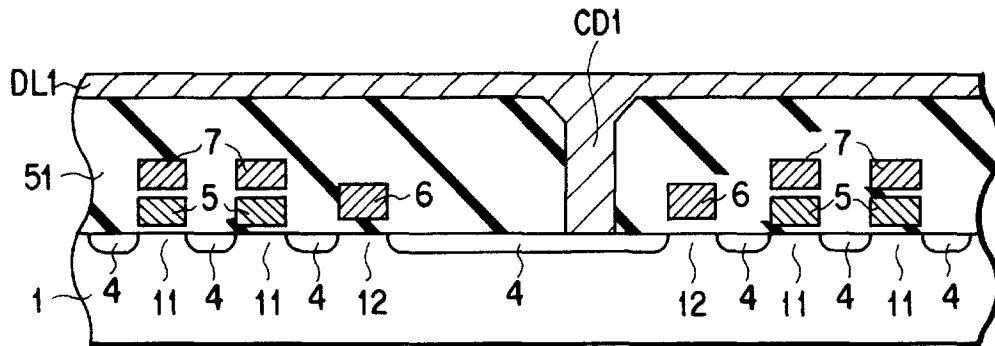


FIG. 7 (PRIOR ART)

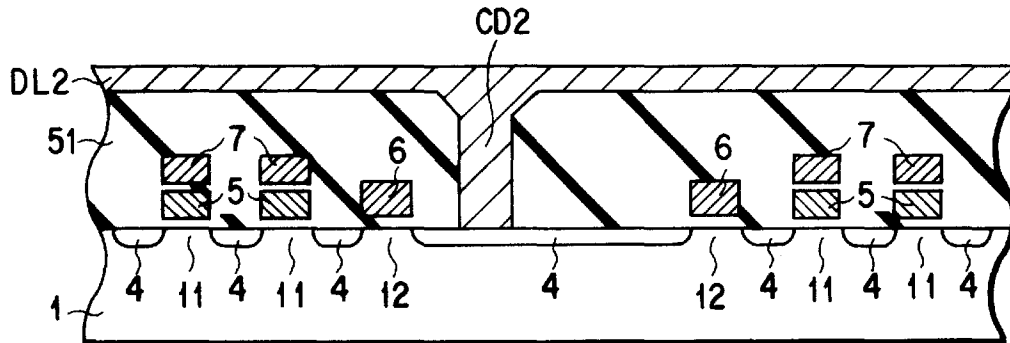


FIG. 8 (PRIOR ART)

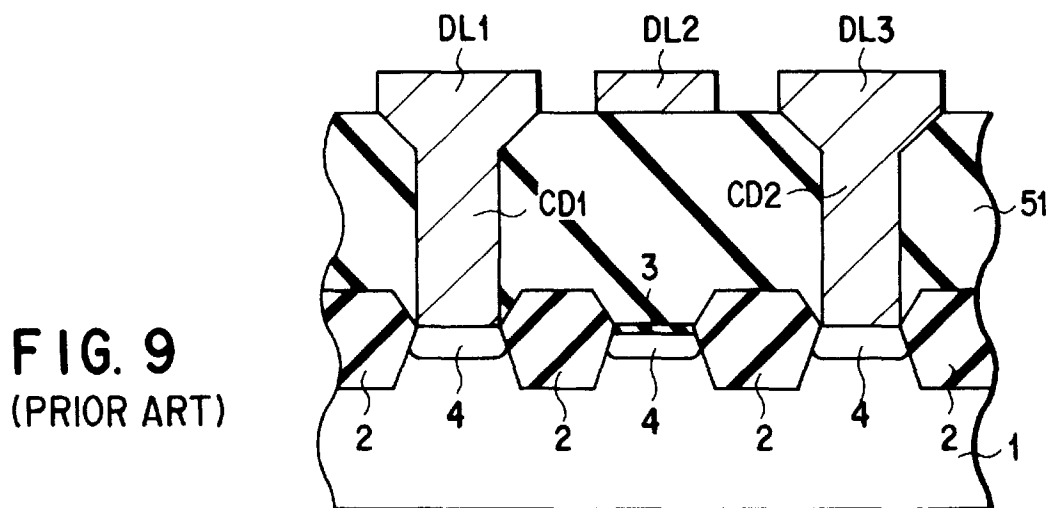


FIG. 9 (PRIOR ART)

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