UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

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SHARP CORPORATION, SHARP ELECTRONICS CORPORATION, and SHARP ELECTRONICS MANUFACTURING COMPANY OF AMERICA, INC.,	:	CASE IPR2015-00021
Petitioners,	:	Patent No. 7,202,843 B2
v.	:	
SURPASS TECH INNOVATION, LLC,	:	
Patent Owner.	:	

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DEPOSITION OF MICHAEL J. MARENTIC

New York, New York

Tuesday, October 6, 2015

9:30 a.m.

Job No.: 94092

Pages: 1 - 167

Reported By: Dana N. Srebrenick, CRR, CLR

Deposition of MICHAEL J. MARENTIC, held at the offices of:

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Pursuant to notice, before Dana N. Srebrenick, CRR, CLR, Notary Public in and for the State of New York.

A P P E A R A N C E S

ON BEHALF OF PETITIONER:

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I N D E X

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E X H I B I T S

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E X H I B I T S (CONT.)

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P R O C E E D I N G S

MICHAEL J. MARENTIC, residing at 22075 White Peaks Drive, Bend, Oregon 97702 having first been duly sworn by the Notary Public of the State of New York, was examined and testified as follows:

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EXAMINATION BY MR. HELGE:

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Q Good morning, Mr. Marentic.

A Good morning.

Q We are here for the deposition in the case of Sharp Corporation, Sharp Electronics Corporation and Sharp Electronics Manufacturing Company of America, Inc. v. Surpass Tech Innovation, LLC, Case No. IPR2015-00021, relating to Patent 7,202,843, and we're here to take your deposition.

Is that your understanding as well?

A It is.

Q Mr. Marentic, you've been deposed before, correct?

A That's correct.

Q Do you know how many times?

A Four to six times.
Q Okay.
A And one of them was a multiple-day deposition.
Q Okay. And at the beginning of each of those depositions, was there some explanation to you of the rules for the deposition?
A Yes, there was.
Q Okay. I will go through the rules for us today, just for clarification. If you have any questions, please let me know. And actually, throughout the day, if you don't understand any question I ask you, please let me know.
Do you agree to do that?
A I do.
Q Thank you.
One of the typical rules is we won't talk over each other.
Do you understand?
A Yes.
Q Thank you.
Can I ask you, are you taking any medications today that would affect your testimony or would affect

or even impair your ability to give true and accurate testimony?

A No.

Q Is there any other reason why you might not be able to give true and accurate testimony today?

A No.

Q Mr. Marentic, you were with us in San Diego and you heard Mr. Lo Cicero read a paragraph from the Office Patent Trial Practice Guide. And I'm going to read that same paragraph here for us today.

That paragraph states, "Once the cross-examination of a witness has commenced, and until cross-examination of the witness has concluded, counsel offering the witness on direct examination shall not: (a) Consult or confer with the witness regarding the substance of the witness' testimony already given, or anticipated to be given, except for the purpose of conferring on whether to assert a privilege against testifying or on how to comply with a Board order; or (b) suggest to the witness the manner in which any questions should be answered."

Do you understand the paragraph as I've just

read it?

A I understand the content.

Q Okay. And do you understand that this paragraph will govern our behavior today until the conclusion of the deposition at the end of the day?

A Yes.

Q And so that prohibition against conferring with your attorneys, it will continue even when I've concluded with my examination and while your attorneys are preparing their rebuttal testimony -- or their rebuttal examination.

Do you understand that?

A Can you explain that?

Q Absolutely. Absolutely.

So I'll be asking questions today.

A Yes.

Q And at some point I'll say, "I have no further questions." And then your attorney will have an opportunity to ask you some questions.

This prohibition against conferring with your attorney continues during that break period, and so they're prohibited from conferring with you and telling

you what questions they're about to ask and guiding you on that.

Does that make sense?

A That makes sense. Thank you.

Q So, Mr. Marentic, just for clarification, am I pronouncing your name correctly, Marentic?

A Correctly, yeah, Marentic.

Q Thank you.

Okay, Mr. Marentic, can I ask you what you did to prepare for today's deposition?

A I read my declaration. I read the Ham patent. I read the '843 Shen patent. I may have reviewed some of the other documents that are cited in my declaration. And met with Mr. Berkowitz a few times.

Q Did you talk to anybody else in preparation for this deposition?

A Briefly, Tony Lo --

MR. BERKOWITZ: Lo Cicero.

A Lo Cicero, yes, came in and briefly --

BY MR. HELGE:

Q I'm going to stop you right there. I'm definitely not asking for the contents of those

discussions. I just want to know the identities of the persons.

A Brian Cormack.

MR. BERKOWITZ: Comack.

A Comack.

So the three --

BY MR. HELGE:

Q The attorneys?

A The three attorneys from Amster, Rothstein & Ebenstein.

Q Did you speak with any colleagues or people that you know from your private practice in your experience as listed on your CV in preparation for this deposition?

A No.

Q Did you speak with any of those people prior to preparing your reply declaration?

MR. BERKOWITZ: Objection to form.

MR. HELGE: That's a good point. Let me clarify that question.

BY MR. HELGE:

Q While you were in the process of preparing

your reply declaration, did you speak to any of the people that you knew from your time in private practice or in any of your employment with -- that's shown on your CV?

A No.

Q Do you recall the last time you reviewed the petition that Sharp filed in this case?

A Not precisely.

Q You reviewed it prior to preparing your reply declaration, right?

A Yes.

Q And when I say "reply declaration," just for clarification, I'm referring to what's been marked in this case as Sharp Exhibit 1010. It's entitled "Rebuttal Declaration of Michael J. Marentic in Support of Petitioner's Reply to Patent Owner's Response. "

A Yes.

Q Was that your understanding when I asked you that question as well?

A Yes.

Q While you were reviewing that petition, did you see any statements or characterizations that you

disagreed with?

A No.

Q So you agreed with everything in the petition?

A Yes. It was logical, straightforward, understandable.

Q So I understand that you weren't involved with this case at that stage, while the petition was filed?

MR. BERKOWITZ: Objection to form.

MR. HELGE: I'll re-ask the question.

BY MR. HELGE:

Q So I understand that you did not file a declaration in support of that petition; is that right?

A That is correct.

Q Looking back at the petition, is there anything that you would have done differently had you been involved with the case at that stage?

MR. BERKOWITZ: Objection. Foundation. Relevance.

A I believe the petition was clear and understandable.

Q And the petition -- or, excuse me.

The theories of the case as expressed in your

reply declaration, those theories are all consistent with the petition, right?

A I believe so, yes.

Q So the petition is technically sound in your opinion?

MR. BERKOWITZ: Object --

A Yes.

MR. BERKOWITZ: Just objection to foundation.

BY MR. HELGE:

Q Mr. Marentic, you've read the petition, right?

A I have read the petition.

Q And you have experience in LCD technology, correct?

A I do.

Q And you understand the '843 patent, correct?

A I do.

Q And you understand the Ham reference, correct?

A I do.

Q Was there anything in the petition that you didn't understand?

MR. BERKOWITZ: Objection to foundation and relevance.

A When I read the petition, it was given to me after the Patent Trial and Review Board had issued their decision. So the patent -- the section that I concentrated on was principally that of Ham, and breezed through the other sections that related to other patents. I principally read Ham -- the Ham section at the end of the petition.

BY MR. HELGE:

Q And you didn't see anything in that section that you disagreed with?

MR. BERKOWITZ: Objection. Foundation.

A Everything there was clear and made sense to me.

BY MR. HELGE:

Q And your theories are consistent with that petition?

MR. BERKOWITZ: Again, same objection. Objection, foundation.

A My analysis is consistent with that.

BY MR. HELGE:

Q So you haven't deviated from those theories of invalidity as expressed in the petition; is that right?

MR. BERKOWITZ: Objection to form. Foundation.

A I agreed with the Ham section of the petition. I find no errors and have no disagreements with it.

BY MR. HELGE:

Q And your theories of invalidity as expressed in your reply declaration are consistent with the petition, correct?

MR. BERKOWITZ: Objection to form. Foundation.

A My declaration is a rebuttal to the patent owner's response and to Mr. Bohannon's written declaration. And those sections where the patent owner or Mr. Bohannon disagree with the petition, I find several of those in error. And that is reported in -- in my rebuttal declaration.

BY MR. HELGE:

Q Mr. Marentic, I'm not trying to trick you. I really just want to understand whether you think that the theories of invalidity expressed in your rebuttal declaration are consistent with the theories of invalidity as expressed in the petition.

Does that make sense?

MR. BERKOWITZ: Objection to form.

A My technical analysis in -- in my rebuttal is consistent with the technical section of Ham in the petition.

BY MR. HELGE:

Q So you haven't presented any new invalidity theories in your declaration; is that right?

MR. BERKOWITZ: Objection to form. Foundation.

A My declaration is a rebuttal to the patent owner's response and Mr. Bohannon's declaration.

BY MR. HELGE:

Q Let's talk about your experience a little bit. You've been deposed, you said, about four to six times; is that right?

A Correct.

Q Were those all patent cases?

A They were.

Q And were those all cases in which you were presented as an expert in either validity areas or infringement areas?

MR. BERKOWITZ: Objection to form.

A The cases that I was deposed for were for patent-related issues in invalidity or infringement.

BY MR. HELGE:

Q And you were presented as an expert on behalf of your party; is that right?

A That is correct.

Q In those cases, did you have to construe claims as part of your role as an expert?

MR. BERKOWITZ: Objection to form.

A In a couple of instances, the claims were construed at a Markman hearing and they were done outside my area of -- well, outside my participation.

Q And so in those cases you were asked to provide an opinion using those constructions, right?

A Correct.

Q Okay. In any of those cases, were you asked to provide an opinion on the proper construction of claim terms?

MR. BERKOWITZ: Objection to form.

A I don't recall any.

BY MR. HELGE:

Q So would you say that this case is the first instance in which you've been asked to provide an opinion on the proper construction of claim terms?

MR. BERKOWITZ: Objection to form. Foundation.

A I don't believe I've been asked to provide claim construction input.

BY MR. HELGE:

Q So let me ask you this: Do you have no opinion on the proper construction of terms at issue in the '843 patent?

MR. BERKOWITZ: Objection to form.

A I took note that the original petition did not ask for any terms to be construed. I note -- noted that the preliminary patent owner's response did not ask for any claims to be construed. And I noticed that the Patent Trial and Review Board chose not to construe any terms.

BY MR. HELGE:

Q So you have no opinion on the construction of any terms; is that right?

MR. BERKOWITZ: Objection to form.

A The terms have not been construed by those prior documents or review board. So there is no claim -- specific claim construction, as I've seen in the past, where this term means this thing and I need to plug in that longer phrase for a word or two. This case has none of that.

BY MR. HELGE:

Q You understand that to establish invalidity of a patent claim, you have to consider each word in that claim, correct?

MR. BERKOWITZ: Objection to form.

A Could you repeat the question?

(Whereupon, the question is read back by the reporter.)

A Yes.

BY MR. HELGE:

Q And to consider each word in that claim, you need to understand what each of those words mean in the claim, correct?

MR. BERKOWITZ: Objection to form.

A That would be by a person -- as read by a person of ordinary skill in the art.

BY MR. HELGE:

Q So to consider each word in the claim, we would need to have the meaning of each word in that claim known as it would be understood by a person of ordinary skill in the art, correct?

MR. BERKOWITZ: Objection to form.

A When the specification and the claims are read together by a person of ordinary skill in the art, every word in the claim should be considered.

BY MR. HELGE:

Q When you just said "when the specification and the claims are read together by a person of ordinary skill in the art," what did you mean by that?

A The claims aren't an isolated item. The specification isn't an isolated item. The two together form the patent with the figures and the claims refer to words or concepts described in the words section of the patent.

Q And by words section of the patent, are you talking about the specification?

A The specification, the abstract, the prior art, the summary, and then the description.

Q Is there any part of the specification that's more important than another part?

MR. BERKOWITZ: Objection to form. Foundation.

BY MR. HELGE:

Q Mr. Marentic, don't answer that question. I'm going to ask that again.

Is there any part of the specification that's more important than another part when you are construing claim terms?

MR. BERKOWITZ: Objection to form.

A I don't know. That sounds like an excellent legal question. That situation didn't come up here so I would need to have some expert legal input to answer that question.

BY MR. HELGE:

Q In your time as an expert, have you developed a standard practice for construing claim terms?

MR. BERKOWITZ: Objection to the form. Foundation.

A As I mentioned earlier, I haven't construed terms -- I haven't construed terms. The court has

construed terms.
BY MR. HELGE:
Q Have you construed terms in any other proceedings before the Patent Trial and Appeal Board?
A No.
MR. BERKOWITZ: Objection to form.
BY MR. HELGE:
Q Did you submit a declaration in support of a petition for inter partes review of Surpass's '550 patent?
MR. BERKOWITZ: Objection to relevance.
A I did.
BY MR. HELGE:
Q And in preparing that declaration, did you provide any opinions on claim construction?
MR. BERKOWITZ: Objection to form.
A I have not read that declaration since it was submitted and don't have a recollection of whether terms were construed or not.
MR. HELGE: I'm going to ask that this be marked with an exhibit label. This is Mr. Marentic's Declaration in Support of Petition for Inter Partes

Review, U.S. Patent No. 7,420,550. It's previously been marked as Sharp Exhibit 1007, but because it was a different case, we can't use that number.

MR. BERKOWITZ: Great.

(Exhibit A, Declaration of Michael J. Marentic in Support of Petition for Inter Partes Review, U.S. Patent No. 7,420,550, marked for identification.)

MR. BERKOWITZ: I just want to object on the record. This is irrelevant and outside the scope. I make an objection to the exhibit that's been marked as Exhibit A.

BY MR. HELGE:

Q Mr. Marentic, I've handed you what is entitled "Declaration of Michael J. Marentic in Support of Petition for Inter Partes Review for U.S. Patent 7,420,550."

Does this document look familiar to you?

A Yes, it does.

Q And what does it look like to you?

A What does it --

Q What does it look like to you?

A It looks like my declaration from the end of

March of this year for the '550 patent that we're not here to talk about today.

Q The cover page, Michael J. Marentic, is that you?

A That is me.

Q Would you please turn to the last page, 76?

Is that your signature on the last page?

A Yes, it is.

Q Can I ask you to please turn to page 22 and please take a moment to read paragraph 66 and 67, and please let me know when you're done.

(Whereupon, witness reads the document.)

BY MR. HELGE:

Q Mr. Marentic, I asked you a few minutes ago, have you construed terms in any other proceedings before the Patent and Trial -- and Appeal Board, and your answer was no.

Having just looked at paragraph 66 and 67, do you stand by that answer?

MR. BERKOWITZ: Objection to form.

And I just want to make a standing objection to relevance and outside the scope, just so I don't have

to keep interrupting.

Go ahead.

A I believe my answer was correct that I gave to you. I don't believe this is claim construction. I believe construed is a more formal ruling from a court that would say "Phrase A means," and then what it is.

BY MR. HELGE:

Q I'm going to read from the first sentence of paragraph 67 of your declaration.

It states here, "I believe that 'insulated with each other' means 'spaced apart from and parallel to each other.'"

Did I read that sentence correctly?

A Yes, you did. There were some quotes in there, but yes, those were the words in there.

Q So maybe there is a disconnect between what I'm saying and what's in your mind.

How would you characterize that sentence, if it's not construing a term?

A That's my understanding of what "insulated with each other" means.

Q Is there a word that we can use today to

characterize this process that you went through so that we're not having a disconnect? I would call it claim construction, but you don't seem to like that. So I just want to know, what word can we use for today for purposes of this deposition so that we understand that what you've done here is what I'm talking about?

MR. BERKOWITZ: Objection to form.

A I still don't believe this is claim construction in trials that I've been involved with.

As to a synthetic term to use, could be almost anything as long as we agree that -- as to what it means. I -- I was reading the patent and there was a term, "insulated with each other," which is used in that patent, and I said what my understanding is.

BY MR. HELGE:

Q Can we call this claim interpretation?

A Or my understanding.

Q Your understanding of what?

A The term insulate -- quote, insulated with each other, quote, in my understanding means, quote, spaced apart from and parallel to each other, close quote.

Q So is this a process for you to decide what you think a claim term means?

MR. BERKOWITZ: Objection to form.

A Again, I haven't read this since March. I don't have a total recall on the intricacies and nuances. I'd like to review it further if we're going to spend more time going over a declaration from last March.

BY MR. HELGE:

Q Mr. Marentic, I'm just getting at the process that you go through to understand what a claim means. All we're looking for is a word to characterize that process.

A My understanding, my experienced understanding.

Q In your reply declaration in the '21 case, did you provide any opinion on your understanding of Claim 4 --

MR. BERKOWITZ: Objection to form.

BY MR. HELGE:

Q -- of the '843 patent?

MR. BERKOWITZ: Sorry to interrupt.

Objection to form.

A I don't know what the '21 case is.

BY MR. HELGE:

Q That would be the case dealing with the '843 patent.

A No. I did not offer any claim construction with respect to the word "generating," for instance.

Q What about any other terms appearing in Claim 4?

A I don't --

MR. BERKOWITZ: Objection to form.

Go ahead.

A I don't believe I've construed any of the claims or any of the phrases or any of the terms.

BY MR. HELGE:

Q When you prepare a declaration for a case before the Patent Trial and Appeal Board, are there parts of the declaration that are more important than other parts?

MR. BERKOWITZ: Objection to form. Foundation.

A Not that I'm aware of.

BY MR. HELGE:

Q So everything in your declaration is in there for a reason; everything's important, correct?

A Correct.

Q You mentioned a few minutes ago that to understand a claim term, you might look at the specification; is that right?

Did I get that right?

MR. BERKOWITZ: Objection to form.

A The claim and the specification help me understand the patent.

BY MR. HELGE:

Q Is there anything else you look at to understand a patent?

A From the first page to the last page, being an engineer, I like figures.

Q Anything else?

A No.

Q You mentioned about being an engineer. Engineers seem to like procedures.

Would you say that you follow the same procedure every time you're trying to understand a

patent?

MR. BERKOWITZ: Objection to form. Foundation.

A I've known a lot of engineers and they're about like humans, all different. Some follow procedures and anything outside the boundary they're uncomfortable with or won't do. And other engineers are just the opposite, can't get them to follow a procedure if their life depended on it. So the generalization that engineers are, kind of equivalent to men are or women are. It's just incorrect.

BY MR. HELGE:

Q So where do you fall in that range? Do you follow the procedures or do you take a different path each time you're trying to understand a patent?

A I follow my process of reading it quickly once, slowly a second time, third, fourth. When certain terms are used in the specification, I will write those in figures. After some number of readings of everything, I feel I generally understand it.

Q And you follow that procedure with every patent that you read?

A Every patent on which I'm an expert witness.

Q So you followed that procedure with the '843 patent; is that right?

MR. BERKOWITZ: Objection to form.

A I followed my read-it-several-times-bring-phrases-into-the-figure process with the '843 patent.

Q And through that procedure you established your understanding of the claims; is that right?

MR. BERKOWITZ: Objection to form.

A By reading the patent and then the claims, I feel I understood the claims.

BY MR. HELGE:

Q And did you provide an opinion on your understanding of those claims in your reply declaration?

MR. BERKOWITZ: Objection to form.

A My reply -- my declaration is a rebuttal to the patent owner's response and to Mr. Bohannon's declaration. In this declaration, I was not asked to provide an opinion as to whether a claim was invalid or not.

And we're talking about the '843 patent, correct?

BY MR. HELGE:

Q Yes.

MR. BERKOWITZ: Should we take a break?

MR. HELGE: Go off the record at 10:19.

(Whereupon, a brief recess is taken.)

MR. HELGE: Back on the record at 10:27.

BY MR. HELGE:

Q Mr. Marentic, you attended Mr. Bohannon's deposition in San Diego; is that right?

A I did.

Q And you heard his testimony that day?

A I did.

Q And you reviewed his declaration as well, right?

A I did.

Q Now, I know you don't agree with his conclusions, but at any point during his deposition, did you wonder whether Mr. Bohannon actually understood LCD technology?

MR. BERKOWITZ: Objection to the form.

A I believe Mr. Bohannon is an expert in LCD drive.

BY MR. HELGE:

Q As of November 17, 2003, how many years of experience did you have in working with flat panel displays, roughly?

A In 2003?

Q That's right.

A I started in '73, so that would be 30 years of flat panel display experience.

Q Would it be fair to say that as of that date, November 2003, your understanding of LCD technology far exceeded that of a recent university graduate with an electrical engineering degree?

MR. BERKOWITZ: Objection to form. Foundation.

A For a bachelor's degree, some universities allow a small dissertation. If one student did a dissertation on LCD, they would be thoroughly knowledgeable. Nevertheless, I would say my experience and knowledge of LCDs would exceed that of a bachelor's degree graduate in electrical engineering.

MR. HELGE: I'm going to ask the reporter to mark the petition for this case as Exhibit B.

(Exhibit B, Petition for Inter Partes Review of U.S. Patent 7,202,843 marked for identification.)

BY MR. HELGE:

Q Mr. Marentic, does this document marked as Exhibit B look familiar to you?

A Yes.

Q And what is this document?

A This is the petition for inter partes review of U.S. Patent '843.

Q And you reviewed this document prior to preparing your reply declaration; is that right?

A I did.

MR. HELGE: I also have an exhibit that we don't need to mark, if it's all right with you, Mark. It's already been designated Sharp Exhibit 1010 in this case.

MR. BERKOWITZ: That's fine.

BY MR. HELGE:

Q Mr. Marentic, I'm going to hand you this document that's marked as Exhibit 1010.

A Okay.

Q And does this document look familiar to you?

A Yes. This is my rebuttal to the patent owner's response and Mr. Bohannon's declaration.

Q And this is the document that we've been referring to today as the reply declaration; is that right?

A No, this is the rebuttal. If you go to my upper page 5, Paper No. 20, patent owner's response, there's a possibility I referred to this as patent owner's reply.

I don't recall the context that I use the word "reply."

Q When we were talking this morning about whether you provided an opinion regarding your understanding of claim terms, claims, we were talking about this document --

MR. BERKOWITZ: Objection --

BY MR. HELGE:

Q -- is that correct?

MR. BERKOWITZ: Objection to form.

A Oh, we've talked about claim terms a couple of times, once in an abstract, once in a '550 declaration and once relative to this.

I -- if you want to -- an answer to a question, would you ask that question?

BY MR. HELGE:

Q Certainly. Well, let's come back to that.

For now, do you -- you recognize this document that's in front of you, is that correct, Sharp Exhibit 1010?

A Yes.

Q And on the cover page it mentions "Rebuttal Declaration of Michael J. Marentic."

Is that you?

A Correct, that is me.

Q Okay. And can you please turn to the last page, page 41 of 41?

A Yes.

Q Is that your signature?

A That is.

Q Can you please turn in this document to page 19 of 41?

Are you there?

A Yes.

Q At the top of that page, there's a header

entitled "Level of Skill in the Art"; is that right?

A Correct.

Q I'm going to ask you to take that page, hold it open, and turn to page 19 of the petition, which has been marked as Exhibit B. We're going to compare these documents.

I have to give you a correction on that. I'm sorry. That may be the wrong page.

No, that is the right page.

So do you have page 19 open in the petition?

A I do.

Q Okay. And can you put that next to page 19 of your rebuttal declaration?

A Yes, I can.

Q Okay. Mr. Marentic, in the petition, which I believe is what you're looking at right now, can you please look at the second-to-last paragraph, beginning with the second sentence? You should see the words "For purposes of the obvious, analyses presented below."

Do you see that sentence?

A Yes.

Q Okay. I'm going to continue to read there.

"Petitioner submits that a person of ordinary skill in the art has an undergraduate degree in electrical engineering or equivalent work experience and would have had two to five years of experience in using or designing driving devices for LCD patents."

Did I read that sentence correctly?

A Yes.

Q Okay. In comparison, let's take a look at page 19 of 41 from your rebuttal declaration, paragraph 42, at the very top of the page. I'm going to read.

"A person of ordinary skill in the art would have had an undergraduate degree in electrical engineering, or equivalent work experience. That person would also have had three or more years of experience designing flat panel display drive electronics and active matrices for LCDs."

Did I read that sentence correctly?

A Yes.

Q Do you believe that these two standards for a person of ordinary skill in the art are the same?

MR. BERKOWITZ: Objection to form.

A The paragraph in my declaration calls out three or more years' experience with an EE degree or equivalent work experience for that knowledge. The petition calls out two to five years' experience designing driving devices for LCD panels. So the years are different.

BY MR. HELGE:

Q The experience is also different; isn't it?

MR. BERKOWITZ: Objection to the form.

BY MR. HELGE:

Q In the petition, it's using or designing driving devices for LCD panels, while in your declaration, it is experience designing flat panel display drive electronics and active matrices for LCDs; isn't that right?

A My definition calls out the three years with flat panel display drive electronics and active matrices and the petition calls out two to five years' experience in using or designing driving devices for LCD panels. So the experience is a little bit different.

Q Sitting here today, do you agree more with your rebuttal declaration or do you agree more with the

standard in the petition?

MR. BERKOWITZ: Objection to form.

A I believe both are equivalent. The years aside, the knowledge that a person would have at that point would be roughly equivalent to these two definitions.

BY MR. HELGE:

Q So it really doesn't matter if the person actually designed driving devices or just used them; is that right?

MR. BERKOWITZ: Objection to the form.

A I believe they would need to use driving devices or design of the driving devices for the LCD panels. One would be purchasing gate drivers, source drivers. The other would be designing gate drivers, source drivers.

BY MR. HELGE:

Q Is that an example of using or is that the only way that you understand a person can use an LCD driving device?

MR. BERKOWITZ: Objection to form.

A Well, what I just said was a -- what I

thought -- reasonably understandable example of using. So, for instance, were someone to use LCD panels in some other product and do nothing more than read the specification, that would not be sufficient. They would have to have intimate knowledge of the drive electronics, the chips, the timing controller, to be a -- a person of ordinary skill in the art.

BY MR. HELGE:

Q At any point either during Mr. Bohannon's deposition or while you were reading his declaration, did you get any sense that he would not meet this standard based on his knowledge?

MR. BERKOWITZ: Objection to form.

A I have no reason to doubt the fact that Mr. Bohannon would meet these criteria.

BY MR. HELGE:

Q Mr. Marentic, we can put away the petition for a little while, and let's just take a look at your declaration. And this is the declaration marked as Exhibit 1010 in this case.

Can you please turn to page 9 of 41, and do you see at the top of that page there is a header

entitled "Legal Standards"?

A Yes.

Q And the paragraphs included under that heading include paragraph 20, 21, 22, 23, on to the next page, 24 and 25; is that right?

A Yes.

Q Without revealing the contents of discussions that you had, would it be correct to say that these legal standards were informed to you by your counsel -- or by counsel for Sharp in this case?

A That is correct.

Q Was there any other source for these legal standards, any other source that you relied upon for these legal standards?

A No.

Q And can I ask you to please read paragraph 22 to yourself and let me know when you've concluded?

(Whereupon, witness reads the document.)

A I've read paragraph 22.

BY MR. HELGE:

Q Would it be fair for me to say that that paragraph is about the process for establishing the

meaning of claim terms?

MR. BERKOWITZ: Objection to form.

A It's one of the components of understanding the claim.

BY MR. HELGE:

Q And what other components are there?

A The whole patent.

Q Can you please clarify your answer when you say "the whole patent"?

A The cover page, the figures, the background, prior art, specification, all the way up to the claims. So in understanding claims, the entire document, the patent, is used also to understand meaning of the claims.

Q And in this rebuttal declaration, do you provide any opinion regarding your understanding of the claims or any terms of the claims?

MR. BERKOWITZ: Objection to form.

A The word "generating," there was -- I believe there was some discussion about the meaning of what generate means, and Mr. Bohannon said the term "generate" means what it means. As a person of ordinary

skill in the art, the word "generating" would be obvious.

I believe that as -- I mean, if we go to the section where there is the term "generating," Claim 4 requires generating a plurality of data impulses. And I believe Ham satisfies the claim. There has been paragraphs written saying that the -- Sharp did not adequately define the term "generate." And I believe the term "generate," as does Mr. Bohannon, is just clear to anyone that meets the skill -- person of ordinary skill in the art.

BY MR. HELGE:

Q So you're not offering a construction for generating; is that right?

MR. BERKOWITZ: Objection to form.

A I am not offering a construction for generating.

BY MR. HELGE:

Q Are you offering a construction for any of the terms in the '843 patent in this rebuttal declaration?

MR. BERKOWITZ: Objection to form.

THE WITNESS: Would you ask the question

again, please?

BY MR. HELGE:

Q Are you offering a construction for any other terms in the '843 patent in this rebuttal declaration?

A No.

Q Mr. Marentic, does your understanding of the legal standards of claim construction go beyond what is stated on pages 9 and 10 of your rebuttal declaration?

MR. BERKOWITZ: Objection.

A My legal understanding of claim construction and, in general, the law, is limited. I'm a technical person.

BY MR. HELGE:

Q So these two pages contain your entire understanding; is that right?

A Yes.

Q Looking solely at paragraphs 20 to 25 in your rebuttal declaration, can you please point to me the legal standard that allows you to look beyond the patent for the meaning of the patent's terms?

Does that question make sense to you?

MR. BERKOWITZ: Objection to the form.

A I don't understand the question.
BY MR. HELGE:
Q Do you recall that you included some exhibits to your declaration?
A There were a couple of exhibits.
Q There were three patents and a Sharp publication; is that right?
A That's correct.
Q What I'm wondering is, in your discussion of the legal standards on page 9 and 10 of this rebuttal declaration, where do these legal standards give you authority to look beyond to those other exhibits for the meaning of the '843 patent's terms?
MR. BERKOWITZ: Objection to form.
A Those other patents did not define any term. They rather confirmed my understanding of the term "transmission rate."
BY MR. HELGE:
Q So you were relying on the accuracy of those other documents for that meaning of transmission rate; is that right?
MR. BERKOWITZ: Objection to form.

A No. I understood what transmission rate meant from my prior experience, and those three patents confirmed my understanding.

BY MR. HELGE:

Q So you weren't concerned whether those documents were accurate?

MR. BERKOWITZ: Objection to form.

A I -- I don't know what accurate means.

BY MR. HELGE:

Q You weren't concerned whether those documents used the term "transmission rate" accurately?

MR. BERKOWITZ: Objection to form.

A Those three patents used the term "transmission rate" as I understand it.

BY MR. HELGE:

Q And is that an accurate use, from your opinion?

MR. BERKOWITZ: Objection to form. Sorry.

A Those three patents used the term "transmission rate" in a fashion that I was accustomed to using.

BY MR. HELGE:

Q And you believed that use is accurate, right, or true?

MR. BERKOWITZ: Objection to form.

A The use of the phrase "transmission rate" in those patents is true to my understanding.

BY MR. HELGE:

Q Generally speaking, if you were reading a patent claim and you came upon a term that could have one of two possible meanings, what procedure would you go through to reconcile the meaning of that term or to understand that term?

MR. BERKOWITZ: Objection to form. Foundation.

A I would reread the patent several times and -- over a course of a couple of days, and I believe I'd resolve any ambiguity that I initially had.

BY MR. HELGE:

Q And you'd read the entire specification, right?

A Yes. I would read the entire patent, front page to back page.

Q In your experience as an engineer, do you read

many journal articles?

A Yes.

Q And is it common for journal articles that you read to include an abstract on the cover page, for example?

A Some do, some don't.

Q What's your understanding of the purpose of an abstract?

A To quickly understand the contents of the entire journal without having to invest the time to plow through the whole journal article.

Q Would you expect every detail from the article to be contained in the abstract?

MR. BERKOWITZ: Objection to form.

A Probably not every detail, but the general points or discoveries or techniques that are being described in the article would be in the abstract.

BY MR. HELGE:

Q Let's talk about abstracts in the context of patents.

Is your understanding of an abstract for a patent any different than what you just explained to me

for a journal article?

MR. BERKOWITZ: Objection to form.

A My understanding of an abstract is as an engineer. So if abstract has some connotation in the legal sense, I'm not aware of that. The abstract, to me, is a summary of the invention.

BY MR. HELGE:

Q If you were reading a patent claim -- I'll withdraw that question.

Let's take a look at a document that I'm going to ask the reporter to mark as Exhibit C.

(Exhibit C, Copy of United States Patent No. 4,464,657, marked for identification.)

BY MR. HELGE:

Q Mr. Marentic, the document that's just been handed to you marked as Exhibit C, do you recognize this document?

A Yes.

Q What is it?

A It's a patent on which I'm a co-inventor.

Q So this is Patent No. 4,464,657, correct?

A Correct.

Q And under the inventors, there's a Michael J. Marentic.

Is that you?

A That is me.

MR. BERKOWITZ: I'll just object that the -- what we just marked as Exhibit C is not relevant and outside the scope of the deposition.

MR. HELGE: And I'll note that this is actually listed in his CV as one of his patents.

BY MR. HELGE:

Q Mr. Marentic, can you please turn to the second-to-last page.

At the bottom of column 11 and the top of column 12, do you see the list of claims that begins on the bottom of column 11?

A That begin with --

Q The list of claims that begins at the bottom of column 11?

A Yes.

Q And do you see that Claim 1 continues from the bottom of column 11 to the top of column 12?

A Yes.

Q I'm going to read this first line in column 12.

The line reads, "Means for providing input waveforms for said driver circuit, said means comprising."

In the very next line, I'm going to read to you, "Means for providing waveforms of different arbitrary lengths."

Did I read that correctly?

A Yes.

Q Okay. Can you please turn to the abstract and tell me if you see the words "waveforms of different arbitrary lengths" in the abstract of this patent?

(Whereupon, witness reads the document.)

A I've read the abstract now. We've gone through the first claim.

Could you ask the question again, please?

BY MR. HELGE:

Q Absolutely. Can you please tell me if you see these words in the abstract, and the words are, "waveforms of different arbitrary lengths."

Are those words in the abstract?

A I don't see those in the abstract.

Q Is it fair for me to say that abstracts may not contain all the details of a claim in exactly the same words, based on what we just read in your patent?

MR. BERKOWITZ: Objection to form.

A The abstract will not always contain all of the elements or all of the nuances of an invention.

BY MR. HELGE:

Q I'm going to hand you, Mr. Marentic, what's been marked as Sharp Exhibit 1011.

Do you recognize this document?

A I do.

Q And what is this document?

A This is my resumé.

Q And this was the document -- or the exhibit that was filed in conjunction with your rebuttal declaration in this case; is that right?

A Yes, it looks to be that document.

Q And if you turn to page 3 of that document, do you see the bottom lists where you have three patents there?

A Yes.

Q And the very last patent in that list is Patent No. 4,464,657; is that right?

A That's correct.

Q And that was the patent we just looked at; is that right?

A Yes, it is.

Q Let's take a look at your experience.

In your very first entry on here on page 1, maybe you can tell me how to say this: Is it QinetiQ?

A No.

Q Can you please tell me how to pronounce that? I apologize.

A QinetiQ.

Q Okay, thank you.

A K-e-n-i-t-i-k, I guess, would be the phonetic.

Q And that experience runs from 2002 to 2011, correct?

A Correct.

Q Can you tell me what you've been doing since 2011?

A I've been not working for a formal company. I've searched out a retirement community, bought a

home -- or remodeled a home, redid some of the landscaping, learned to play pickleball and volunteer at a couple of different events. And as a hobby, I play around with single board computers, have taken a couple of Linux courses. I've got a couple of cloud servers that are only accessible to me. I remain a member of the Society for Information Display and follow the journal -- journals when they come out and, I think once, attended an SID symposium.

Q Thank you.

Now, your CV doesn't list your experience as an expert witness; is that right?

A That is correct.

Q Off the top of your head, can you give me some of the cases that you've been involved with?

A The first case was Matsushita/Panasonic versus Samsung, and there were numerous subsidiaries and U.S. entities, offshore entities. I think if printed it would be about half a page. But generally, Panasonic/Matsushita versus Samsung.

Q And that was a plasma display panel case; is that right?

A That was relating to plasma displays.

There was a second case, Pioneer versus Samsung.

Q And that was also a plasma display panel case; is that correct?

A That was a plasma panel display case.

There was one, Positive Technologies versus -- I think -- Fujitsu, et al., of which one party was Matsushita or Panasonic.

And there was a fourth one that was Rovi versus Toshiba.

The Positive Technologies, that was, as I recall, three LCD panels, or three varied LCD technologies.

Rovi versus Toshiba was text information transmitted in the video stream.

Q So that's four cases.

Are there any others that you haven't mentioned yet?

A Those are the only ones that I recall.

Q So at QinetiQ, from 2002 to 2011, you list here that there were 600 employees?

A Yes.

Q And --

A I worked there for nine years. I initially joined a company called Science and Engineering Associates. There were a couple of small pockets around the United States. They purchased a company called IT -- or a portion of a company called ITS Solutions. And shortly thereafter, the company was re-branded as Apogen, A-p-o-g-e-n. And then Apogen, along with another company, Foster Miller, was purchased by the QinetiQ Company, which is headquartered in the UK.

And during that nine years, I sat at the same desk and had five different business cards, different support for purchasing, different support for contracts, HR. And as we were assimilated in, sometimes we were moved to other divisions. So really, QinetiQ North America was the North American division of the UK company, firewalled off from them, and there were three groups. And we were in the technology solutions group. And in 2011, there was 600 employees in the TSG sector.

Q And did any of those other 600 employees have a good working understanding of LCD technology?

A There was a group in the Boston, formerly known as Foster Miller, that laid claim to some of the earliest patents in LCD technology.

There was another group that moved around the organizational structure that characterizes flat panel displays optically. I think that's Radiant Technology, a leader in the field.

There was many groups, total 20 or 30, in the TSG sector scattered around the United States. There were in fact three in San Diego, where I lived. And we generally didn't know what each other did for a number of reasons.

So I'm -- other than the ones I've mentioned, those are the most visible pockets of flat panel or LCD knowledge that was around.

Q And do you keep in touch with any of those people?

A Yes, a couple of them.

Q In preparing your rebuttal declaration, did you contact any of those people to discuss any issues related to your opinions in the rebuttal declaration?

MR. BERKOWITZ: Objection to form. Relevance.

A I did not contact any of the approximately 600 employees in the QinetiQ TSG sector prior to -- let me rephrase that -- within several months prior to my writing my declaration, nor after, regarding opinions on this matter. When -- as a matter of practice, when I work on a case, I tell no one who the clients are, who it's for or against, what it involves or anything. Occasionally, I'll get questioned why I take a day off, and I would say I'm working as an expert witness. And that's the extent of my -- the management of QinetiQ's knowledge of my activities.

BY MR. HELGE:

Q And does that go as well for the 110 employees at Alien Technology?

MR. BERKOWITZ: Objection to form.

A I've not contacted anyone at Alien for years.

BY MR. HELGE:

Q If you had a technical question in your own work, who would you go to for assistance or questions or even checking of your opinions?

MR. BERKOWITZ: Objection to form.

A If I were involved in a new field and needed

to learn about it, I still go to the old-fashioned library at a university. I have textbooks or journal articles. I may look on Amazon if there's a book on that field and buy it. I may go to used technical bookstores and buy used books and become as knowledgeable as I can about that, to understand that area of expertise. And if I find there's a shortcoming, I'll address that shortcoming by repeating that process. Or if I am working with someone or someone is going to contract with our company to do some work, I'll ask the point of contact for some background material, which is usually provided.

BY MR. HELGE:

Q So in preparing your rebuttal declaration, and specifically in preparing your discussion of the "generating" term and the "controller transmission rate" term, you didn't contact any of the people that you used to work with at any of these companies to check your opinions against what they think?

MR. BERKOWITZ: Objection to form.

A I believe I said prior to writing my declaration I had no contact with any of these people

relative to any of the work on this case or the '550 case.

BY MR. HELGE:

Q I'm going to hand you what's been marked as Sharp Exhibit 1012.

Does this document look familiar to you, Mr. Marentic?

A I believe this is one of the patents that I referred to. Let me look at it.

(Whereupon, witness reads the document.)

A This is one of the documents that I looked at to confirm my understanding of transmission rate.

BY MR. HELGE:

Q To confirm your understanding of the meaning of the word "transmission rate"?

A Yes.

Q And where did you turn to in your rebuttal declaration to check that information?

MR. BERKOWITZ: Objection to form.

MR. HELGE: I'll ask that again.

BY MR. HELGE:

Q You were just reading from your rebuttal

declaration, correct?

A I was checking that this patent is in fact one that -- that the patent number of this exhibit you just handed me is in fact the patent number in my declaration.

Q Okay. And which paragraph in your declaration are you looking at?

A 92.

Q Okay. Do you see in the middle of that paragraph you have the sentence that reads -- and I'll read, "A search of the art confirms that this is the case."

Do you see that sentence?

A Yes.

Q Who conducted that search?

A That search for the patent side was conducted by someone at ARE after --

MR. BERKOWITZ: I'll just caution the witness not to reveal any privileged information. You can answer, you know, who conducted the search, yes or no, but don't reveal any communications.

A The search was conducted by someone at ARE at

my request.
BY MR. HELGE:
Q Did you provide instructions for how to conduct the search?
MR. BERKOWITZ: Again, yes or no. Yes or no answer.
A No.
BY MR. HELGE:
Q Do you know how the search was conducted?
A No.
Q Do you know what terms were used to search?
MR. BERKOWITZ: Objection to form.
A No.
BY MR. HELGE:
Q Do you know how many results were found as a result of the search?
MR. BERKOWITZ: Objection to form.
A No.
BY MR. HELGE:
Q Do you know of any results of the search that were given to you that you later discarded or decided not to use in your declaration?

MR. BERKOWITZ: Objection to form.

Again, caution the witness not to reveal any privileged communications.

A These three were the three that were provided.

BY MR. HELGE:

Q So you don't know the field of the search; is that right?

MR. BERKOWITZ: Objection to the form.

A I don't know how the patents were obtained -- what the search criteria was, how they were obtained. I was provided the three patents. I looked at them. And each of them used the term "transmission rate," which was consistent with my understanding of the term.

BY MR. HELGE:

Q You don't know if those three patents were selected out of ten possible candidates, right?

MR. BERKOWITZ: Objection to the form.

A All I know is I was given those three patents.

BY MR. HELGE:

Q You don't know if it's three out of 100 patents; is that right?

MR. BERKOWITZ: Objection to the form.

A I have no knowledge.
BY MR. HELGE:
Q You don't know if it's three out of a million; is that right?
MR. BERKOWITZ: Same objection to the form.
A I have no knowledge.
BY MR. HELGE:
Q Do you see the two inventors listed at the top of Exhibit 1012?
A Yes.
Q I would say Shichao Ge and Jemm Liang.
Is that okay, a fair pronunciation?
A Yes.
Q Do you know either of these people?
A No.
Q Have you ever talked to them?
A No.
Q Do you know their technical background?
A No.
Q Do you know if they wrote this patent application?
MR. BERKOWITZ: Objection to the form and lack

of foundation.

MR. HELGE: That's the point.

BY MR. HELGE:

Q Do you know if they wrote this document?

MR. BERKOWITZ: Same objections.

A If -- if they wrote --

BY MR. HELGE:

Q This patent?

A -- this patent?

Q Do you know if they wrote it or if their attorneys wrote it?

MR. BERKOWITZ: Objection, foundation. Objection to the form.

A No.

BY MR. HELGE:

Q So you don't know if these are their words or their attorneys' words?

MR. BERKOWITZ: Same objections. Objection to form and foundation.

A I don't know if these are their words or their attorneys' words.

BY MR. HELGE:

Q Do you see on the right --

A In reviewing the patent, I believe the patent owners would have understood and made corrections.

Q But you don't know that for sure, right?

A I do not.

Q Do you see on the right-hand side there's a line for Attorney, Agent Or Firm and it lists Majestic, Parsons, Siebert & Hsue?

A Yes.

Q Do you know any attorneys at that firm?

MR. BERKOWITZ: Objection to the form. Objection to relevance.

A I don't recognize that name. I don't know all the attorneys at that firm.

BY MR. HELGE:

Q Do you know any of the attorneys at that firm?

A I can't say. I don't know who's there. There's a possibility that someone I've worked with at the past is now there.

Q But you don't know for sure?

MR. BERKOWITZ: Objection. Foundation. Relevance.

BY MR. HELGE:

Q But you don't know for sure?

A I don't know for sure if any attorneys that I've worked with are presently at the firm Majestic, Parsons, Siebert & Hsue.

Q Do you know whether either of the inventors or any attorneys at this firm possessed the technical skill that you identify in your rebuttal declaration when this patent application was being prepared?

MR. BERKOWITZ: Objection to form. Foundation.

A As I said earlier, I don't know the inventors and I don't know their background.

BY MR. HELGE:

Q Have you relied upon this patent for any purpose before or after preparing your rebuttal declaration?

MR. BERKOWITZ: Objection to the form.

A I have not relied on this before, during or after the writing of my rebuttal. I cite it only as something that confirms the term "transmission rate" as used with LCDs.

BY MR. HELGE:

Q Did you read this patent in full while preparing your rebuttal declaration?

A I read it quickly once through.

Q In full?

A In -- in full.

Q And you reply -- excuse me. I'll restate that.

You rely upon this patent for the meaning of transmission rate, correct?

MR. BERKOWITZ: Objection to form.

A No.

BY MR. HELGE:

Q What do you rely upon this patent for, then, in your rebuttal declaration?

A It confirms my understanding that transmission rate has been used in other patents and that it means just simply what I know it to mean.

Q And what is that?

A Transmission rate is the percentage of light through a media, and it's simply measured and routinely measured in industry as a light source, a measurement of

the intensity. Put the device under question between the two, measure the lower reading, divide the smaller by the larger and that's the transmission rate, or the more common industry term, transmittance. And if that transmittance is multiplied by a hundred, then you get the percent transmission, which is the most common term used in the optic side and the LCD side.

Q Can you please turn to page 11 of 24 in this document, Mr. Marentic? This is the patent, the Ge patent, Exhibit 1012.

MR. BERKOWITZ: I'm sorry; what --

MR. HELGE: Page 11 of 24.

BY MR. HELGE:

Q And this should be Figure 13; is that what you're seeing on this page as well?

A Yes.

Q Do you see, the second row of figures here, there's a line and the label is "Transmittance"?

Do you see that?

A Yes.

Q Is that the same as transmission rate, from your understanding?

A My understanding is transmittance, transmission rate and percent transmission in this context are interchangeable.

Q So they mean the same thing?

A Yes.

Q Even though the words are different?

A Yes. It's not unusual for different factories, different companies to use a term that is -- means the same, but is slightly different than a competing company.

Q So even in patent context, it's possible for a patent to use two different words to mean the same thing; is that right?

MR. BERKOWITZ: Objection to the form.

A Well, as a layperson, with respect to law, a single term is usually referred to as one thing, but it is possible to have two different terms to mean the same thing.

MR. BERKOWITZ: I need a short break.

MR. HELGE: Sure. We'll go off the record at 11:41.

(Whereupon, a brief recess is taken.)

MR. HELGE: We'll go back on the record at 11:56.

BY MR. HELGE:

Q Mr. Marentic, we talked this morning about the rules for deposition about not talking to your attorney regarding the testimony we've already given and the testimony that we're expected to give.

Do you recall that discussion?

A Yes.

Q Have you talked to your attorney about any of your testimony or anticipated testimony during this break?

A No.

Q How about the previous break?

A No.

Q I noticed you dog-eared a page in that exhibit; that wasn't at the direction of your counsel?

A No. That's my cite, column 10, 22 to 24 in my paragraph 92.

Q Going back to this discussion of the search that was conducted, you don't know if there were any results of the search that were disregarded by counsel

before giving you these three patents; is that right?

MR. BERKOWITZ: Objection to the form.

A I know nothing about how the search was conducted. I was given these three patents and noted that the word "transmission rate" was used.

BY MR. HELGE:

Q So you don't know if there were other results where they used the word "transmission rate" but counsel decided not to give them to you; is that right?

MR. BERKOWITZ: Objection to form.

A I don't know how the search was conducted or how many were found and which ones were provided to me.

BY MR. HELGE:

Q So you don't know if they found patents that used the word "transmission rate" in a manner different than these patents use it?

MR. BERKOWITZ: Objection to the form.

A I don't know that the word "transmission rate" was different in other patents. These three confirm my understanding of transmission rate. It's just a simple percentage of the light going through.

BY MR. HELGE:

Q But if counsel found other results that didn't confirm your understanding, you never saw those results, right?

MR. BERKOWITZ: Objection to the form.

A I didn't see any patents during my declaration writing process that was different from these three.

BY MR. HELGE:

Q Assume with me that there are some patents out there that use the word "transmission rate" in a manner differently than you're using it, a hypothetical discussion here. How many would there need to be using that term in a different way -- well, let me restate this because it's going to get confusing.

If counsel gave you three patents that used transmission rate in a different way, and the three patents that they did give you, they used transmission rate in your way, would that change your opinion on whether you're using it correctly?

MR. BERKOWITZ: Objection to the form.

A I would need to investigate and understand deeper why the term "transmission rate" was different.

BY MR. HELGE:

Q If you found a hundred patents that used transmission rate in a different way in the context of LCD technology, would that change your opinion?

MR. BERKOWITZ: Objection to the form.

A I find it difficult that I would read 100 patents searching for the deeper understanding of transmission rate. If it were different than my understanding, then I would dig deeper and try and understand the nuances that cause it to be different than my understanding.

BY MR. HELGE:

Q Are you aware of the burden of proof in this proceeding?

A I would go to my legal section and parrot it back to you.

Q Why don't you take a look at page 9 of 41, specifically paragraph 21?

A That's where I was going to.

The petitioner must prove invalidity by a preponderance of evidence.

Q And do you have an understanding of what that means --

MR. BERKOWITZ: Objection --

BY MR. HELGE:

Q -- beyond just the words?

MR. BERKOWITZ: Objection to the form.

A It means just slightly more than questionable. A 51 percent factor would be enough to tip the scale.

BY MR. HELGE:

Q And you know that there are three patents that you contend confirm your understanding of the meaning of transmission rate, correct?

A There are three patents that use the term similar to how I understand it.

Q And you don't know how many patents out there use the term differently than how you understand it, right?

MR. BERKOWITZ: Objection to the form.

A I don't know how many patents are out there. I don't know how many patents out there that use the term "transmission rate," and I don't know how many patents use it in a similar way, an identical way, a slightly different way, a radically different way.

BY MR. HELGE:

Q I'm going to hand you what's been marked as Exhibit 1013 in this case.

Mr. Marentic, do you know what this document is?

A It's a patent also referred to as confirming my understanding of transmission rate.

Q And was this document also provided to you by counsel as a result of the search they conducted?

A Yes, it was.

Q Had you seen this patent before that search result was handed to you, provided to you by counsel?

MR. BERKOWITZ: Objection to form.

A I don't recognize this patent as something that I've read or am familiar with.

Q Okay. Let's take a look near the top.

Do you see the listing of the two inventors up there?

A Yes.

Q Do you know either of those inventors?

A I do not.

Q Have you ever talked to either of those two inventors?

MR. BERKOWITZ: Objection to form. Foundation.

A I don't believe or recall that I've talked to either of those.

BY MR. HELGE:

Q Do you know the technical background of either of those inventors?

MR. BERKOWITZ: Objection to the form.

A I do not know what their background is.

BY MR. HELGE:

Q Do you know if these inventors drafted this patent?

MR. BERKOWITZ: Objection to the form. Foundation. Relevance.

A I don't know if these inventors drafted this.

BY MR. HELGE:

Q Do you see, over in the right-hand side, there's a listing for Attorney, Agent Or Firm and it's listed as Blakely Sokoloff Taylor & Zafman?

Do you see that?

A I see that.

Q Do you know any of the attorneys who were

working at that firm when this patent was drafted?

MR. BERKOWITZ: Objection to the form. Foundation. Relevance.

A When this patent was drafted?

BY MR. HELGE:

Q Yes.

A No.

Q You don't know whether the inventors drafted this patent or whether an attorney at that firm drafted the patent; is that right?

MR. BERKOWITZ: Objection to the form.

A I don't know who did the drafting, but would believe the inventors read it and made corrections.

BY MR. HELGE:

Q But you don't know that for sure, right?

A I do not.

Q Do you know if either of the inventors meet your standard for a person of ordinary skill in the art in this case?

MR. BERKOWITZ: Objection to the form.

A No, I do not.

BY MR. HELGE:

Q Do you know if any of the attorneys at this Blakely firm meet your standard for a person of ordinary skill in the art in this case?

MR. BERKOWITZ: Objection to the form.

A If any of the attorneys meet my criteria for a person of ordinary skill in the art, is the question?

BY MR. HELGE:

Q Yes, exactly.

A No, I don't.

Q In paragraph 92 of your declaration --

A Yes.

Q -- the very last three lines of this paragraph, you discuss Exhibit 1013, correct?

A Yes.

Q And in that discussion, there's no appearance of the phrase "control a transmission rate"; is that right?

MR. BERKOWITZ: Objection to the form.

A In my declaration, there is not control a transmission rate.

BY MR. HELGE:

Q Are you aware of whether this patent uses the

phrase "control a transmission rate"?

A Would you please ask the question again?

Q Are you aware of whether this patent uses the term "control a transmission rate"?

A I am not aware of whether this patent uses the term "control a transmission rate" together.

Q When this exhibit was provided to you by counsel, did you read the entire patent?

MR. BERKOWITZ: Objection to the form.

A I quickly read the patent.

BY MR. HELGE:

Q Did you read the entire patent?

A Yes, quickly.

Q When you say "quickly," does that imply that you didn't glean a full understanding of the patent when you read it?

MR. BERKOWITZ: Objection to the form.

A I read it thoroughly enough to understand the contents at the time and to understand when the phrase "transmission rate" came up that it meant the same thing as I understood it to be.

BY MR. HELGE:

Q And during that reading, you didn't notice whether this patent uses the term "control a transmission rate"; is that right?

A Correct.

Q Have you relied upon this Exhibit 1013 for any other purpose since your declaration?

MR. BERKOWITZ: Objection to the form.

A Have I relied on Exhibit 1013 for --

BY MR. HELGE:

Q Any other purpose.

A No.

Q Mr. Marentic, I'm going to hand you what's been marked previously as Sharp Exhibit 1014.

Do you recognize this document?

A I recognize it as the third patent that was cited.

Q When you say "cited," what are you referring to?

A It was referred to in paragraph 93 of my declaration.

Q And on the top of Exhibit 1014, do you see the inventor, Norio Koma?

A Yes.
Q Do you know that person?
MR. BERKOWITZ: Objection to form. Relevance.
A I don't believe I know that person.
BY MR. HELGE:
Q You've never talked to that person?
MR. BERKOWITZ: Objection to form. Relevance.
A Not that I remember.
BY MR. HELGE:
Q For clarification, was this another patent provided to you by counsel as a result of their search?
MR. BERKOWITZ: Objection to the form.
A This was provided to me by attorneys at ARE.
BY MR. HELGE:
Q Do you know anything about the inventor's technical background?
MR. BERKOWITZ: Objection to the form.
A No.
BY MR. HELGE:
Q So you don't know whether this person satisfies your standard for a person of ordinary skill in the art in this case, right?

MR. BERKOWITZ: Objection to the form. Relevance.

A No.

BY MR. HELGE:

Q Do you know if that -- or, excuse me. I'll say it again.

Do you know if that inventor drafted this patent specification?

MR. BERKOWITZ: Objection to the form. Relevance.

A I do not.

BY MR. HELGE:

Q Do you see, on the right-hand side, the Attorney, Agent Or Firm label on this document is listed as Loeb & Loeb, LLP?

Do you see that?

A Yes.

Q Do you know any attorneys who were working at that firm when this application was drafted?

MR. BERKOWITZ: Objection to the form. Relevance.

A The issue date, 1997, I knew no one at Loeb &

Loeb.

BY MR. HELGE:

Q How about in 1994?

A Also no one.

Q Did you read this entire patent when it was provided to you by counsel?

A I did.

Q Did you also read this patent quickly?

A I did.

Q Do you know whether this patent uses the term "control a transmission rate"?

MR. BERKOWITZ: Objection to the form.

A This does use the term "transmission rate of light is controlled."

BY MR. HELGE:

Q And are you reading that from paragraph 93?

A I am.

Q For any of these exhibits -- and I'm going to refer to the three, 1012, 1013 and 1014 -- did you examine file histories for either of these patents?

A I examined no file histories for these three patents.

Q So if there were attorney arguments in the file history about the meaning of transmission rate, you wouldn't know; is that right?

MR. BERKOWITZ: Objection to the form.

A I do not read the prosecution history, so I wouldn't know whether there was or was not arguments over the term "transmission rate."

BY MR. HELGE:

Q Did you read the file history for the '843 patent while preparing your rebuttal declaration?

MR. BERKOWITZ: Objection to the form.

A I looked at it quickly with counsel.

BY MR. HELGE:

Q Did you look at the entire file history?

A I did not go from page to page to page to page through all 240 or 280 pages.

Q Did you look at the notice of allowance?

A Yes.

Q Did you look at anything specific in the notice of allowance?

MR. BERKOWITZ: Objection to the form.

And I just want to caution the witness, to the

extent there's any communications between counsel, that you should be aware not to divulge those.

A I read the entire page.

BY MR. HELGE:

Q Did you read the reasons for allowance that the examiner drafted in the '843 patent's file history?

A The second page -- or the second paragraph in the reason of allowance describes why Claims 1 through 9 were allowed.

Q Okay.

A I have a copy. It was in my binder. I don't memorize this stuff.

Q Do you understand that Claims 1 through 9 include Claim 4, at issue in this case?

A Yes.

Q And do you understand that the examiner thought that Claim 4 was allowed?

MR. BERKOWITZ: Objection to -- were you done? I'm sorry. Did I interrupt you?

MR. HELGE: No, you're fine.

MR. BERKOWITZ: Okay. Objection to the form. Foundation.

A When this patent was allowed, the examiner understood certain items and allowed the nine claims. I believe the examiner is incorrect with respect to Ham, as does the Patent Trial and Review Board. They also believe an error was made, because that's why we're here today.

BY MR. HELGE:

Q What about the examiner's reasons for allowance are incorrect in your view?

A There's a segment of, I think it's Ham, that's quoted a little improperly, and the examiner thought that the '843 patent was unique.

Q So the examiner's error in your view was quoting Ham improperly; is that right?

MR. BERKOWITZ: Objection to the form.

A The paragraph -- and I guess we don't have the notice of allowance in -- as an exhibit. So I'm looking at an exhibit and you're not looking at it, but my understanding is the examiner misunderstood Ham.

BY MR. HELGE:

Q Did the examiner misquote Ham?

That's my question.

MR. BERKOWITZ: Objection to the form.

A Let me look at Ham and let me look at the quote. It will take a while. I'll get you an answer.

BY MR. HELGE:

Q Your testimony just a moment ago is -- I asked you, "What about the examiner's reasons for allowance are incorrect in your view?"

You answered, "There's a segment, I think it's Ham, that's quoted a little improperly." I'm reading that right from the transcript.

I'm asking you right now, is that your view, is that Ham was quoted improperly and that's the error and the reasons for allowance?

MR. BERKOWITZ: Objection to the form.

A The paragraph in the reason of allowance that discusses Ham quotes from paragraph 53. And Ham stops and puts a period after frame. The examiner puts a comma and then quotes some more from the next sentence. It's not a direct quote. It's a reasonable quote. And I believe that is in error, the examiner's decision.

BY MR. HELGE:

Q So you don't think there is an error in the

quotation; is that right?

A There is a change in the quotation, the period and the comma.

Q Does the examiner --

A And the examiner misunderstands Ham.

Q So the examiner misunderstands Ham, but does not misquote it; is that your view?

MR. BERKOWITZ: Objection to the form.

A The quote isn't 100 percent from Ham.

BY MR. HELGE:

Q The portion that is from Ham, is it quoted accurately?

A The first portion, again, I believe it is. And that is Ham shows "apply the normal data to the liquid crystal panel at the initial half period of the frame after supplying modulated data to the liquid crystal display during the latter half of the frame. Thus, a desired brightness level is achieved within the initial frame period" -- or "initial period of the frame." Sorry.

Q And that's accurately taken from Ham?

MR. BERKOWITZ: Objection to the form.

A The segment that I read is from a paragraph in Ham, but the patent of Ham has a period, and that changes -- changes the understanding of the sentence, I believe.

BY MR. HELGE:

Q Is it the first time that you've done a line-by-line comparison between the reasons of allowance and Ham's disclosure?

MR. BERKOWITZ: Objection to the form.

A I believe I've done it a couple of times.

BY MR. HELGE:

Q I'll just note for the record that it took you probably about four minutes to do that comparison.

A I would normally print it out next to each other and compare it. We are in a deposition and I want to be a little more careful.

Q And you said that you were reading from Ham, paragraph 53; is that right?

A I'm reading the -- comparing the reason of allowance, Item 2, Ham, and comparing that to the Ham patent 53.

Q Do you believe that paragraph 53 accurately

reflects the disclosure of Ham?

MR. BERKOWITZ: Objection to the form.

A It's one of the items that describes the total patent of Ham.

BY MR. HELGE:

Q Are there any technical errors in that paragraph?

A It would perhaps benefit from some rephrasing or some punctuation.

Q But there are no technical errors in that paragraph?

A No.

Q So if the petition relies on paragraph 53, it's an accurate reflection of what's disclosed in Ham?

MR. BERKOWITZ: Objection to form.

A It reflects a segment of what Ham describes, perhaps not the best description.

BY MR. HELGE:

Q But it's technically correct, right, in your view?

A In my view, it is technically correct.

MR. HELGE: Want to break for lunch?

MR. BERKOWITZ: Yeah.

MR. HELGE: Go off the record at 12:35.

(Whereupon, a luncheon recess is taken.)

MR. HELGE: We'll go back on the record at 1:32.

BY MR. HELGE:

Q Mr. Marentic, we talked this morning about the prohibition from talking to counsel about your testimony so far and the anticipated testimony.

Has there been any issue with that during this lunch break?

A No.

Q Thank you.

We have not gotten to a couple of the important documents yet. So we are going to now look at -- I'm going to give you a copy of what's been marked as Sharp Exhibit 1005.

Mr. Marentic, do you recognize this exhibit?

A Yes, this is the Ham patent.

Q And have you read the Ham patent recently?

A Yes.

Q How recently?

A Last week.

Q Do you have a good understanding about what Ham discloses?

A I believe so.

Q Can you explain to me, with reference, if you like, to the figure on page 1, how Ham operates or how Ham's driving circuit operates?

MR. BERKOWITZ: Objection to the form.

A You want me to explain how the circuit on the front of the patent operates?

BY MR. HELGE:

Q Sure, according to your understanding.

A The digital data is fed in from the left side of the timing controller. That's marked data. There's also syncs that are provided -- sync signals that are provided for the horizontal and vertical axis. The timing controller, usually abbreviated as TCON, reformats the data and strips out any dummy data pulses or sync pulses and outputs digitally the red, green and blue data that the source desires to be displayed.

That RGB data is sent to two other boxes or sub-circuits depicted in this figure. One, the line

memory where the data goes in and is stored and read out later, or time-shifted. The data modulator is described as a look-up table that looks at the prior frame and the present frame for each pixel and makes a determination on whether the input commanded data should be boosted or whether decreased, or decremented, as its output in the form of AMdata. That's also digital data.

The switch is controlled by a signal from the TCON initially at a frame, tying the data from the data modulator -- it is transmitted through the switch to the data driver or source driver. Those are common industry terms.

And that data and source driver take the digital data from the switch and converts it to an impulse representing a boosted or unboosted signal, based on the prior data, frame data and the present frame data, the look-up table and data modulator.

As the data is presented, there is two signals from the TCON that start the sequence for the gate driver to scan. The scanned lines are occasionally called gate lines, sometimes scan lines. And initially the top-most line is activated when data is present.

Presented data impulses are presented by the data driver to the source lines labeled 55. And the source lines have a certain voltage on them that when the scan pulse turns on the horizontal row of TFTs, they transmit current to charge up the liquid crystal pixel, and that's depicted as the capital C, little L, little C.

When the first line is -- a scanned pulse is completed, there will be a clock pulse to the data driver that will move the gate start bit down one line to the second line and data will be read again from the data modulator through the switch to the data driver and set up for the second line. That series of events of data from the -- I missed a step.

While it's at the first line, the line memory is read out and output to the switch 58. The data driver converts that time-shifted data, still in digital form, the data driver converts that to an analog pulse and those pulses are present at the vertical-going lines 51, the source lines, data lines.

The gate is turned on again and the commanded data that was input to the timing controller stored in

the line memory 59 pass through the switch, converted to an analog signal at 53, is impressed upon the lines 55 and that is -- will charge -- charge up the liquid crystal capacitance to the final commanded value. And then the process will step down from the top of the display to the bottom of the display sequentially.

For each line, there's initially AMdata that is converted to an impulse and applied to the source line. And then, during the second half of the line time, the data from the line memory is used to charge the liquid crystal display and drive it to the input command value. And then that will scan down.

So each horizontal line is presented with two gate pulses and the data is initially AMdata, and the second data impulse is the input data that was input to the timing controller. It sequences to the bottom of the panel and then rolls around to the top.

Q So is my understanding correct that the output from line memory number 59 would be non-overdriven video data?

A That is correct.

Q And during a first sub-frame for a given

pixel, Ham teaches applying overdriven pixel data, and in the second half of the frame period, Ham applies non-overdriven data; is that right?

MR. BERKOWITZ: Objection to the form.

A Ham applies two voltage impulses. First the overdriven, and the second is created from the input data to the LCD timing controller, TCON.

BY MR. HELGE:

Q Is that non-overdriven data?

A That is non-overdriven data.

Q So if Mr. Bohannon is correct, and Claim 4 requires overdriving in both sub-frames, do you agree that Ham does not teach that method of driving the LCD panel?

MR. BERKOWITZ: Objection to the form.

A Could you restate that or repeat that question again?

BY MR. HELGE:

Q Sure. I'll rephrase it.

Let's assume that Mr. Bohannon is correct in that Claim 4 requires overdriving in both the first sub-frame and the second sub-frame of a frame.

Do you agree that Ham does not disclose that driving method?

A I disagree that Claim 4 requires overdrive, but Ham does not teach overdriving for the first half and second half of the frame.

Q And you agree that when evaluating a patent claim validity, you need to look at every term in that claim, right?

MR. BERKOWITZ: Objection to the form.

A When I look at a patent claim after having read the specification, I look at every word in the claim.

BY MR. HELGE:

Q And when you determine or opine that a patent claim is invalid, do you account for every term in the claim?

MR. BERKOWITZ: Objection to the form.

A Well, in this case I was rebutting Mr. Bohannon's opinion, and I disagree that overdrive is required in Claim 4.

BY MR. HELGE:

Q Mr. Bohannon's opinion was based in part on a

construction of control a transmission rate, right?

MR. BERKOWITZ: Hang on a second.

Objection to the form.

A I'm not sure what Mr. Bohannon was thinking. I -- the question's not clear.

BY MR. HELGE:

Q Do you believe that Ham controls a transmission rate by doubling it?

MR. BERKOWITZ: Objection to the form.

A That question doesn't make sense to me.

BY MR. HELGE:

Q In your rebuttal declaration, do you make any statement that Ham controls a transmission rate by doubling it?

MR. BERKOWITZ: Objection to the form.

A Ham doubles the transmission rate?

BY MR. HELGE:

Q That's right. That's the question.

A That makes -- I -- that doesn't make technical sense to me.

Q When you were going through your discussion of Exhibit 1005, you talked about the data modulator. And

I believe -- well, if we look at page 1 of this exhibit, data modulator shows an output of AMdata; is that right?

A That's correct.

Q And can you remind me, please, how you describe AMdata?

A AMdata is the output of a look-up table that Ham describes in one of the figures.

Q And that's digital data, correct?

A That is digital data.

Q Okay. In your discussion of this figure on page 1 of Exhibit 1005, I didn't hear you say anything about the data modulator generating impulses.

MR. BERKOWITZ: Objection to the form.

BY MR. HELGE:

Q Did you intend to?

MR. BERKOWITZ: Sorry.

Object to the form.

A The voltage impulses are generated by the data driver using digital data from the data modulator transmitted through the switch. And this data driver that takes digital data in and converts it to analog voltage pulses is identical to the process that's used

in the '843 patent.
BY MR. HELGE:
Q So you agree that the data modulator of Ham does not generate any impulses; is that right?
MR. BERKOWITZ: Objection to the form.
A The data modulator does not generate analog voltage pulses.
BY MR. HELGE:
Q Does the data modulator output non-overdriven digital data?
A It could. Ham describes a look-up table, and there's a diagonal that is unity gain. So if the prior frame to the present frame had no pixel value change or grayscale change, there would be no emphasis or decrement, no boost or decrease, and the data would just be transmitted through.
Q Is it possible for line memory 59 to output overdriven digital data?
A I believe it is unlikely that the line memory would change the contents of the digital data it receives and then stores and then reads out.
Q And that's because it's just providing a

memory function, right?

A It is performing a line memory function.

Q So in the scenario you just discussed for data modulator 52 where data modulator 52 is outputting non-overdriven data, within that frame, there would be no overdriven data provided to a pixel, right?

A Well, I think we got out of synchronization here.

In general, the data modulator provides overdriven data. But there was a question as to whether the data modulator could provide non-overdriven data. And under the very narrow circumstance where there was a stationary image, so that frame to frame to frame to frame that delta was zero, there would not be an over-boosted signal. But in -- for instance, in a newscaster -- TV image of a newscaster, talking head, the background, that background would not require overdriven data because it would be constant from frame to frame to frame. Only the lips and facial expressions and bobbing head of the newscaster would that data need to be overdriven.

Q So there is a scenario where, in a first

sub-frame, the data is not overdriven and in the second sub-frame, the data is also not overdriven, correct?

A There is a very narrow circumstance when the image is stationary that there is no overdriven data. But the vast majority of the time in video there would be the need to overdrive or underdrive a pixel based on the input-commanded voltage.

Q And data modulator 52, even if it outputs non-overdriven data, it uses that look-up table, correct?

A Yes.

Q But you'll agree that data modulator 52 does not generate two data impulses, right?

MR. BERKOWITZ: Objection to the form.

A The two data impulses are generated with all of the sub-circuits in concert with each other. Each is necessary in a necessary signal path and flow at different times to generate the two impulses. There isn't a single item that generates everything.

This is my understanding of how it works and this is also the Patent Trial and Review Board, their understanding of how Ham works as a collection of sub --

sub-circuits that work together in concert.
BY MR. HELGE:
Q Is your explanation that you've just given me consistent with what you say in your rebuttal declaration?
A It's meant to be, yes.
Q And is it consistent with the theories that were presented in the petition?
MR. BERKOWITZ: Objection to the form.
A Can you be more specific?
BY MR. HELGE:
Q Are you providing any new theories of invalidity either with your testimony today or in the rebuttal declaration? And when I measure new, I'm measuring relative to what was in the petition.
MR. BERKOWITZ: Objection to the form.
A No.
BY MR. HELGE:
Q Let's take a look at Exhibit 1001. This is the Shen patent.
Mr. Marentic, do you recognize this document?
A Yes, I do.

Q What is this document?

A This is the patent that's being reviewed by the Patent Trial and Review Board.

Q And it's U.S. patent 7,202,843, correct?

A That is correct.

Q Have you reviewed this patent recently?

A Yes.

Q How recently?

A A week ago.

Q Do you feel that you understand this patent?

A I believe so.

Q Can you please turn to page 12 of 15? And I'm going to read to you the top of column 1 under the "Field of Invention" header.

It states, "The invention relates to a driving circuit of a liquid crystal display (LCD) panel and its related driving method, and more particularly, to a driving circuit for applying over two data impulses to a pixel electrode within one frame period, and its related driving method."

Did I read that correctly?

A Yes.

Q In your review of this patent, have you come across any disclosed driving circuits?

MR. BERKOWITZ: Objection to the form.

A Driving circuit is a fairly broad term; can you refine that or narrow it down?

BY MR. HELGE:

Q Sure. If you were to look through it in all these figures, do you see any driving circuits disclosed in the figures?

A Again, pretty broad.

Q There's only ten figures.

A I'm aware that there's ten figures. There are a couple of block diagrams, but there's layers of drive electronics. A block diagram --

Q All right, Mr. Marentic, why don't we look at page 2 of 15? This is showing Figure 1.

Is that a driving circuit?

A That is not.

Q Okay. Let's look at page 3, Figure 2.

Is that a driving circuit?

A It is not.

Q Let's look at Figure 3.

Is that a driving circuit?

A That's a block diagram of some of the electronics around an LCD panel.

Q Is it fair to characterize that as a driving circuit?

A It's a driving circuit plus a little.

Q Fair enough.

How about Figure 4; is that a driving circuit?

A Generally, I would not include the signal controller 12 as part of the driving circuit. That takes composite video in and converts it to digital data and some control signals. That I would put outside of drive electronics for a liquid crystal display.

Q Is there anything else on Figure 3 that you'd exclude from driving circuit?

A The position of the blur clear converter is not what I would have expected, but it is where it is.

Q So is it included in the driving circuit or not?

MR. BERKOWITZ: Objection to the form.

A Shen includes it in the driving circuit.

BY MR. HELGE:

Q How about Figure 4; is that a driving circuit?

A Figure 4 is a schematic of rows and columns with interconnected TFTs driving a pixel. I recall that 39 was a pixel.

Q So is that a driving circuit or not?

A That's a component of a driving circuit.

Q Okay. How about Figure 5; does Figure 5 show a driving circuit?

A Figure 5 does not show a driving circuit.

Q How about Figure 6; does it show a driving circuit?

A Figure 6 does not show a driving circuit.

Q How about Figure 7; does Figure 7 show a driving circuit?

A Figure 7 shows one way of -- the block diagram for one way of making a blur clear converter.

Q And you said before that the blur clear converter, according to Shen, was part of a driving circuit, right?

A Yes.

Q Okay. How about Figure 8; does that show a driving circuit?

A Figure 8 is another method of block diagramming a blur clear converter.

Q And as you told me before, a blur clear converter, according to Shen, is part of the driving circuit, correct?

A According to Shen, the blur clear converter is part of a drive circuit.

Q So is it fair for me to say that Figure 7 and Figure 8 represent a first embodiment and second embodiment of a blur clear converter of the driving circuit of Figure 3?

MR. BERKOWITZ: Objection to form.

A Figure 7 and 8 are two block diagrams of the blur clear converter. And if there's a legal connotation to embodiment, I don't understand that.

BY MR. HELGE:

Q You don't understand the legal connotation of embodiment in general?

A Yes. To me, it's Method 1 and Method 2.

Q How about Figure 9; does Figure 9 show a driving circuit?

A Figure 9 does not.

Q How about Figure 10; does that show a driving circuit?

A It does not.

Q So having gone through that, if I can summarize your testimony according to my understanding, you said that Figure 3 shows a driving circuit, although some parts you don't believe necessarily should be included as part of the driving circuit, and that Figure 7 and Figure 8 show two different block diagrams for implementing the blur clear converter. You also say that Figure 4 shows some components of a driving circuit.

Is that an accurate summary of your testimony?

A Reasonably accurate, yes.

Q Did I make any mistakes?

A All of those components are necessary to display video on the LCD panel, so in that respect, they are correct.

Q And in that respect, I have not made any mistakes in summarizing your testimony, correct?

A I don't believe so.

Q Let's take a look back at Figure 3, please,

page 4 of 15.

A Yes.

Q Do you have an understanding of what capital G represents?

And that is traveling from signal controller 12 to blur clear converter 14.

A I'd go and look in the specification.

(Whereupon, witness reads the document.)

A In column 3 at 22, "Processing the composite video signals Sc to separate them into frame signals G and control signals C."

BY MR. HELGE:

Q Okay. Let's stay with column 3. That's helpful.

Is it correct that frame signals G include frame data?

A Yes.

Q And what does the blur clear converter 14 do when it receives control signals C and the frame data included in frame signals G?

MR. BERKOWITZ: Objection to the form.

A The blur clear converter "generates processed

frame signals G. Subsequently, the blur clear converter G and control signals C" -- I'm sorry. I got off a line.

I'm reading column 3, 24, "Subsequently, the blur clear converter 14 continuously receives control signals C and frame data included in the frame signals G and generates processed frame signals G including a plurality of overdriven data according to the frame data."

BY MR. HELGE:

Q So based on what you just read, is it correct that the blur clear converter receives non-overdriven frame data?

A It does.

Q And is it correct that the blur clear converter generates processed frame signals including a plurality of overdriven data?

A There's probably a typo in 27. Or there's an error in Figure 3.

Q So I assume that you mean that the G should include a prime?

A Correct, in line 27.

Q Of column 3?

A Correct.

Q So is it correct that blur clear converter generates a plurality of overdriven data?

A That's what that line says, yes.

Q Is that what the blur clear converter of Figure 7 also does, generate a plurality of overdriven data?

A In column 4, line 58, "The second memory controller 50 controls the second image memory 46 to output two overdriven pixel data, GN, GN(2) to each pixel 36 within one frame period according to the multiplied signal C2 in order to have the source driver apply two data pulses to the specific pixel."

So Figure 7 does output two overdriven pixel data for each pixel.

Q How about Figure 8? And I'll ask the question more specifically: Does the blur clear converter of Figure 8 generate an output plurality of overdriven data?

A In column 5, line 15, "The third image memory 70 to output two overdriven pixel data in each frame

period according to the multiplied signal C2."

So there are two overdriven pixel data in -- that are generated for each pixel in Figure 8.

Q So I believe we've just addressed the fact that Shen discloses in the driving circuit of Figure 3, blur clear converter of Figure 8 and the blur clear converter of Figure 7, in each of those instances, two pieces of overdriven data are output per frame; is that right?

A That's what the Shen patent states, yes.

Q Are you aware -- excuse me.

Are you aware of any driving circuit in the '843 patent that does not output two overdriven pixel data per frame?

A Yes.

Q Okay. Direct me to that.

A Well, the easiest would be Claim 4. We could also -- Claim 4 has nothing with overdriven in it. And as I recall, the summary of the invention...

MR. BERKOWITZ: Is there a question pending?

MR. HELGE: I'm not sure if he's done with his answer.

MR. BERKOWITZ: Oh, I'm sorry.

BY MR. HELGE:

Q Mr. Marentic, do you have anything else to add to that answer?

A Yes, I do.

In paragraph -- or column 2, line 20 to 33 describes a method of "generating a plurality of data impulses for each pixel within every frame period according to the frame data; and applying those data pulses to the liquid crystal device of one of the pixels within one frame period." So that's a -- another description of driving an LCD without overdriven data.

And there's another one just before the claims, column 5, 45, "In contrast to the prior art, the present invention discloses a driving circuit and relating driving method to generate two pieces of pixel data in each frame period for each pixel on an LCD panel and then generate two data impulses according to the two pieces of pixel data and apply them to each pixel within a frame period in order to change the transmission rate of a pixel electrode. Thus, each of the pixels of the LCD panel is applied a plurality of data impulses within

a frame period so that the LCD molecules of the pixels can twist and reach a predetermined gray level within one frame period, and blurring will not occur."

Q Mr. Marentic, I'm going to object to your entire answer as nonresponsive because my question is related to -- I'm going to repeat it: Are you aware of any driving circuit in the '843 patent that does not output two overdriven pixel data per frame?

So I was looking for a driving circuit. And what I'm going to do is point you here -- let's look at column 7 --

MR. BERKOWITZ: I just want to respond to that. Mr. Marentic's answer was perfectly responsive to your question. I completely disagree.

MR. HELGE: Okay. We'll work it out here.

BY MR. HELGE:

Q Let's take a look at column 7, please.

Your first answer was about Claim 4 and you said that Claim 4 has nothing to do with overdriving. My question was about a driving circuit.

Can you please read the preamble from column 7, of Claim 4?

A Claim 4 is a method.

Q Okay. Is that a driving circuit or is it a method?

A Well, the second word is "method."

Q Okay.

MR. HELGE: So my objection stands.

BY MR. HELGE:

Q Let's take a look at -- your second answer was column 2, line 19, under the Summary of Invention. And you read beginning at line 19 running through around line 32.

Can you please read lines 19 and 20 of column 2 to me?

A "Briefly, the present invention provides a method for driving an LCD panel."

Q And in any of the next 12 lines, do you see any discussion of driving circuit?

MR. BERKOWITZ: Objection to the form.

A Well, there's a description of lines and columns and pixel.

BY MR. HELGE:

Q So is your testimony now that that's driving

circuits?

MR. BERKOWITZ: Objection to the form.

A Well, it describes a method. I guess I'm not understanding your question. I'm not trying to be smart or evasive. I don't know what you're looking for.

BY MR. HELGE:

Q When we went through all these figures, you told me that Figure 3, Figure 7 and Figure 8 show either a driving circuit or parts of it. You mentioned Figure 4 as having a pixel. And I went through and you summarized your testimony and you said it was accurate and I didn't make any mistakes.

So what I'm asking you now, are you changing your testimony to say that something from line 20 to line 32 is now a driving circuit?

MR. BERKOWITZ: Objection to the form.

A It describes a method.

BY MR. HELGE:

Q Now let's turn to column 5.

A However, going -- going back, if I -- if I were to take Shen and not want overdriven data, I would take coefficients or software that are present in the

blur clear converter, and if they were additive in nature, I would set that additive value to zero. If they were multiplicative in nature, I would set that coefficient to one. If they were somehow other processed, I would set that processing to a unity gain condition and thereby disable the blur clear converter so that overdrive did not occur, but yet there would be two voltage pulses applied to each pixel within the frame period.

Q So in order to achieve that driving circuit that I'm asking about, you'd have to modify the disclosure of Shen; is that correct?

MR. BERKOWITZ: Objection to the form.

A I would adjust some constants. If this were applied to a couple of different products, there may be some that are larger that have a more viscous liquid crystal viscosity, and those constants in the blur clear converter would need to be adjusted for that larger, more viscous liquid crystal material, versus a small panel with a low viscosity material. So within Shen, the application, you would need to tune the blur clear converter based on the panel that you're working with.

It's common in the industry.

And if I didn't want any blur clear converter overdrive, I would set those coefficients so that the input data equaled the output data. The G and the G prime would be equal, although time-shifted because of the two or three memory banks.

BY MR. HELGE:

Q And all of that's outside of the disclosure of Shen, right?

MR. BERKOWITZ: Objection to the form.

A It would be obvious to someone how to do that. I mean, these -- these circuits require some tuning. That's just part of implementing the circuit.

BY MR. HELGE:

Q Let's look at column 5, line 46 -- well, 45 and 46.

A Okay, I'm not there. Column 5 --

Q Line 45 to 46.

It says there, "In contrast to the prior art, the present invention discloses a driving circuit and relating driving method."

Did I read that correctly?

A Yes.

Q Where in the Shen patent does it disclose that driving circuit?

MR. BERKOWITZ: Objection to the form.

A That would be the block diagram in Figure 3 minus the signal controller, Item 12; Figure 7, the dual memory; and Figure 8, the triple memory.

MR. HELGE: Want to take a break?

MR. BERKOWITZ: Yes.

MR. HELGE: We are going off the record at 2:33.

(Whereupon, a brief recess is taken.)

MR. HELGE: We're back on the record at 2:45.

BY MR. HELGE:

Q Mr. Marentic, in the Shen patent, beginning at column 1, line 13, Description of the Prior Art, and spanning all the lines below that through column 2, line 12.

Do you see that area that I'm focusing on?

A Yes.

Q Basically what I'm focusing on is the entire section entitled "Description of the Prior Art."

Do you see that?

A Correct.

Q Have I accurately identified the column and line numbers for that region?

A I believe so.

Q Is there any instance in this region that uses the phrase "control a transmission rate"?

Please take your time to read if you need to before you answer.

(Whereupon, witness reads the document.)

A The phrase "control a transmission rate" does not appear, to my reading of it.

BY MR. HELGE:

Q You mentioned earlier that if you want to understand a patent, you read the entire specification from page 1 to the end of the claim; isn't that right?

A Correct.

Q So if you were trying to understand the meaning of control a transmission rate as it appears in Claim 4, you would have read the entire patent, right, from page 1 to the end of the claims?

A Correct.

Q And in reading the entire patent, you would have read Section 2, Description of the Prior Art, correct?

A Correct.

Q And you would not have seen control a transmission rate in this section, correct?

MR. BERKOWITZ: Objection to the form.

A The phrase "control a transmission rate" does not appear in prior art.

However, transmission rate, when I first read it, I knew what it was, although the more common term, as I've said before, is the transmittance or the percent transmission.

Q Is it important to you when you're trying to understand a patent whether a claim term appears in the discussion of the background or not?

MR. BERKOWITZ: Objection to the form.

MR. HELGE: I'll rephrase it.

BY MR. HELGE:

Q When you're trying to understand a patent, is it important to you whether a claim term appears in the background section or not?

MR. BERKOWITZ: Objection to the form.

A I'm not sure I've ever mentally thought whether every word in a claim is in the description. Generally, they are, and if they're not and they haven't been construed or a construction given by a court, then it's its plain and ordinary meaning.

BY MR. HELGE:

Q So I want to make sure I understand. I want to know if it's important to you whether a claim term appears in the background section when you're trying to understand a patent. I don't think your answer addressed that topic.

MR. BERKOWITZ: Objection to the form.

A If I'm trying to understand a patent and there are terms in the claim, I am not concerned that those claims are listed in prior art.

BY MR. HELGE:

Q So whether those terms appear in the discussion of the background or the discussion of the prior art or not doesn't matter to you?

MR. BERKOWITZ: Objection to the form.

A I'm not sure I've ever considered that.

BY MR. HELGE:

Q Let's pull up Exhibit A again, please.

MR. BERKOWITZ: Sorry. Why don't you remind me what Exhibit A was?

MR. HELGE: I'm sorry, Exhibit A was the declaration from the '550 patent.

BY MR. HELGE:

Q Let's turn to page 22 of 76.

Mr. Marentic, in paragraph 66, you're providing a discussion of what a claim term means to you; isn't that right?

MR. BERKOWITZ: Objection to the form.

A I have to spend some time looking at this. I haven't looked at it since March.

(Whereupon, witness reads the document.)

A I've read a little bit around the area of paragraph 66 of the '550 patent, which we're not here to discuss today.

Would you ask your question again?

BY MR. HELGE:

Q Is it correct that paragraph 66 is your discussion of what a claim term in the '550 patent means

to you?

MR. BERKOWITZ: Objection to the form.

A It looks like I was discussing a couple of phrases, yes.

BY MR. HELGE:

Q And what they mean to you, correct?

A Yes.

Q And if you focus on the third sentence of paragraph 66, you actually compare the disclosure of the prior art with the disclosure in the first embodiment; don't you?

A That looks to be the case, yes.

Q You told me before that everything that you put in your declaration is important; isn't that right?

MR. BERKOWITZ: Objection to the form.

A Yes.

BY MR. HELGE:

Q So clearly, when you were preparing this declaration, you thought it was important whether the prior art described a concept that you also found in the first embodiment; isn't that right?

MR. BERKOWITZ: Objection to the form.

A In this report, yes, that looks to be the case.

BY MR. HELGE:

Q And in your rebuttal declaration for the '843 patent, you provide no discussion of whether the prior art uses the term that appears in Claim 4; isn't that right?

MR. BERKOWITZ: Objection to the form.

A I don't know if I do or don't. I mean, we've just --

BY MR. HELGE:

Q Well, look --

A -- we just read -- you had me read the prior art of Ham and my mind doesn't work as a look-up table in processing where phrases are coming from.

Q You just read the background for me from the '843 patent. You read the entire thing quietly to yourself, and you admitted that the background section never uses the word "control a transmission rate"; isn't that right?

A That's correct.

Q We just looked at your declaration in the '550

patent case and we just showed that you compare what's in an embodiment with what's described in the prior art.

Didn't you do that?

A It looks like it.

Q And we know that Shen does not use a claim term "control the transmission rate" in the discussion of the background.

So clearly, you couldn't have talked about what's not there, correct?

MR. BERKOWITZ: Objection to the form.

A To me, the transmission rate is one item and controlling the transmission rate is another item. It happens to be a verb, and the verb describes controlling a certain item. So I don't ascribe any profound significance to the fact that there is controlling transmission rate not in the prior art. There is transmission rate in the prior art and there are methods of changing gray levels, which controls transmission rate, that will make pixels brighter or dimmer according to the 256 digital data input grade levels. So the phrase you're lumping together, "control transmission rate," to me, is two separate items. Controlling the

liquid crystal orientation, you would control the voltage across the pixel. There's a number of instances where control is being done according to the commanded input voltage. And one of them is, the transmission rate is simply the amount of light flowing from the back light through the display.

BY MR. HELGE:

Q Let me ask you this: Are you unsure whether you mention the absence of that term in the background?

MR. BERKOWITZ: Objection to the form.

BY MR. HELGE:

Q I should be clearer.

Are you unsure whether you mention in your rebuttal declaration that control a transmission rate does not appear in the background?

MR. BERKOWITZ: Objection to the form.

BY MR. HELGE:

Q Because if you're not sure, we can pull out the rebuttal declaration and clarify.

A We're not talking about the '550 patent?

Q That's right.

A We're talking about the '843 patent?

Q That's right.

A Okay. So in the '843 patent, the question is, is the phrase "controlling transmission rate" anywhere in my rebuttal? Is that your question?

Q My question is -- is whether you recall discussing the fact that that term does not appear in the background of the invention?

MR. BERKOWITZ: Objection to the form.

A I don't recall. You want me to read it now?

BY MR. HELGE:

Q No.

So I'll ask you this: According to the '843 patent, is using two overdriven pixel -- excuse me -- is using two overdriven data pulses one method of controlling a transmission rate?

A That doesn't make sense. Two overdriven data bits of digital data?

If you want to confer with your colleague, you can.

Q So you agree that the '843 patent discloses generating two overdriven data per frame from the blur clear converter, correct?

MR. BERKOWITZ: Objection to the form.

A There are two sets of data, digital data that come out of the blur clear converter, and Shen exclusively refers to those as overdriven data.

BY MR. HELGE:

Q And so Shen also describes converting the overdriven data into data impulses and applying them to the pixel per frame, correct?

A That is correct. That's the function of the source driver, or data driver, performs a digital analog conversion that voltage gets applied to the vertically-oriented source or data lines on the TFT array and cause changes in the molecules, and thereby changes the transmission rate.

Q And is that, according to Shen, a method of controlling the transmission rate?

MR. BERKOWITZ: Objection to the form.

A That is a method of controlling the liquid crystal orientation, which controls the amount of light through the display, which Shen says is transmission rate.

BY MR. HELGE:

Q Let's take a look back at the petition in this case. And I think that was designated as Exhibit B.

Do you have that, Mr. Marentic?

A I do.

Q Okay. Can you please turn to page 3.

On the very first line of pros on this paragraph, it says, "To achieve the desired transmission rate within a single frame, the '843 patent suggests applying two or more overdriven impulses to each pixel within a single frame period as shown below." And the citation is then to column 4, lines 20 to 40 of the '843 patent.

Did I read that correctly?

A I believe so.

Q Do you agree that's what the '843 patent discloses?

MR. BERKOWITZ: Objection to the form.

A That's one of the two drive methods that the '843 discloses.

BY MR. HELGE:

Q Do you disagree with the statement?

MR. BERKOWITZ: Objection to the form.

A That statement is correct, but there is yet another way of driving the LCD that Shen describes, and that's without the overdrive. This is a cite with overdrive.

BY MR. HELGE:

Q Is that other method you just mentioned, without overdriving, is that described in this petition at all; do you know?

MR. BERKOWITZ: Objection to the form.

A I'm not sure. I don't recall. I'd probably go back and look at claim charts in the latter section.

BY MR. HELGE:

Q So we've already talked about some of the disclosure of the '843 earlier this afternoon. And you pointed me to a couple of different disclosures as supporting your belief that there was another method described.

And if I were to ask you right now to do that again, would you identify the same portions of the '843 or is there anything else that you left out previously?

MR. BERKOWITZ: Objection to the form.

A I would look at those same sections.

BY MR. HELGE:

Q On page 16 -- can you turn to page 16 in this petition?

Do you see those two figures in the middle there?

A Yes.

Q Do you see Figure 3 in the left and Figure 5 on the right?

A Yes.

Q And the sentence right above those two figures reads, "Figure 5, reproduced below, right, shows two overdriven pixel data GN+1 and GN+1(2) generated by the blur clear converter 14 for each pixel in the frame period n+1."

Did I read that correctly?

A Yes.

Q Do you agree with that statement?

A Yes. Although graphically they don't look like one is larger than the other. They look about equal amplitude.

Q Can you please turn to page 24.

And do you see the two figures near the top?

A Yes.

Q And according to the sentence right above these figures, "Petitioner states that Figure 6 of the '843 patent is reproduced below, right."

Do you see that where that Figure 6 is shown? It's not labeled as Figure 6.

A Yes, I see that figure.

Q Okay. And do you see the annotations that petitioners have added at the top of that figure?

A I'm looking at the figure. I see those annotations.

Q And during the sub-frame period n+2, do you see the annotation on top that reads "First overdriven data impulse"?

A That's correct.

Q And in sub-frame n+3, do you see it reads "Second overdriven data impulse"?

A I see that annotation.

Q Do you agree that those annotations are correct?

A I'd like to go back a ways and see if this is referring to -- what all this is referring to. There is

some references to Jinda, and I've never read that patent.

Q So you don't know whether Jinda discusses a transmission rate?

A I've never seen or read Jinda.

Q How about the Miyai reference, M-i-y-a-i, which was relied upon in the petition? Did you read that reference at all?

A I have not received that nor read it.

Q So you don't know whether Miyai discusses transmission rate at all?

A No.

Q You don't know whether Jinda or Miyai discuss controlling the transmission rate?

A No. By the time I was asked to review this, the Patent Trial and Review Board had already issued their ruling and only relied upon Ham, so I only studied Ham.

Q Well, I left you hanging on this Figure 6 from the '843 patent. I had asked you if you agreed with the characterization of Figure 6 as including the first overdriven data impulse and the second overdriven data

impulse, and you had said you wanted to take a look back. So I'd like to renew that question and just give you some time to look through it.

A Okay.

(Whereupon, witness reads the document.)

A It looks like it's a comparison of Jinda and Ham. I have no background on Jinda.

BY MR. HELGE:

Q I think it's Jinda and Shen, the '843 patent.

A I'm sorry, yes, Shen.

Q So you agree with the annotations that there's a first driven data impulse applied in sub-frame n+1 and a second overdriven data impulse applied in sub-frame n+3?

MR. BERKOWITZ: Objection to the form.

MR. HELGE: Yeah, I think I misstated.

BY MR. HELGE:

Q Let me restate it, Mr. Marentic.

So you agree with the annotations shown in Figure 6 here on page 24 of the petition where first overdriven data impulse is applied during sub-frame n+2 and second overdriven data impulse is applied in

sub-frame n+3?

MR. BERKOWITZ: I'm going to object to form and also object on relevance.

A I'm not sure which embodiment is being pulled out of the '843 patent, whether it's two non-overdriven impulses or whether it's the overdrive. So I see the words that you've described, and yeah, they're there. Without delving in and reading Jinda and understanding this more, I don't know which technique of driving an LCD the '843 is being culled from.

BY MR. HELGE:

Q Do you have any reason to believe that your counsel were mistaken when they provided that annotation?

MR. BERKOWITZ: Objection to the form. Relevance.

A I didn't read Jinda and I don't know, without spending a lot of time, what was trying to be shown here. The annotations that were added that you've read, I see present, and I don't know if that is referring to Technique 1 from the '843 that applies two impulses per pixel in a frame time or whether it is overdriven

pixels, which is a second technique.
BY MR. HELGE:
Q Can we pull up Shen one more time, please, the '843 patent, and let's look at column 2. I'm going to focus you on column 2, line 16.
I'll read -- go ahead, please.
A I'm there.
Q Would you like to read that sentence for me, please?
A "It is therefore a primary objective of the claimed invention to provide a driving circuit of an LCD panel and its relating driving method to solve the problem mentioned above."
Q And do you know what "problem mentioned above" is referring to?
A It's the slowness of a transition from one transmission rate to a second transmission rate. And if that is slow, with moving video, the molecules can't move quick enough within one frame time and there will be some blurring at the moving edges of the image. Stationary sections of the image used -- or I use the talking head newscaster; there would be no aberration

for the set around the newscaster, only his lips, head, as he bobbles, and torso as he moves about, but the rest of it would be crisp and clear.

Q The sentence also talks about a driving circuit of an LCD panel.

Do you see that?

A It does.

Q And is that the same driving circuits we were talking about earlier?

MR. BERKOWITZ: Objection to the form.

A Well, Shen only has limited descriptions, and we've gone over them, 3, 4, 7 and 8. So that would be the closest with the text corresponding to that to a description of the driving circuit.

BY MR. HELGE:

Q And do you see in this line also it talks about "and its relating driving method"?

A I see those words, yes.

Q "And its relating driving method" refers back to the driving circuit; isn't that right?

MR. BERKOWITZ: Objection to the form. Foundation.

A I'm not sure what that means.
BY MR. HELGE:
Q You're not sure what --
A I think where you're trying to get is Claim 4 has overdriving in it. I think that's your end game with this line of questioning. And I disagree that there's overdrive in Claim 4.
Q And I understand that.
Do you agree that "its relating driving method" refers back to a driving circuit of an LCD panel?
MR. BERKOWITZ: Objection to the form. Foundation.
A If there's a legal concept associated with that, I'm not familiar with it, but in plain and ordinary English, its -- its driving method is one of the primary objectives.
BY MR. HELGE:
Q What does "its" refer to?
MR. BERKOWITZ: Objection to the form. Foundation. Also relevance.
A Its appears to refer to the driving circuit of

an LCD panel that was the object of the invention.
BY MR. HELGE:
Q Mr. Marentic, do you understand anything about the theory of inherency in the context of a validity analysis?
MR. BERKOWITZ: Objection to the form. Foundation. Relevance.
A That's easy: No.
BY MR. HELGE:
Q So you're not relying on inherency to claim that Claim 4 or Claim 8 or Claim 9 of the '843 patent are invalid, are you?
MR. BERKOWITZ: Objection to form.
A I don't understand that question at all. I'm -- I'm the electrical engineer, not the attorney.
BY MR. HELGE:
Q We talked earlier today about the burden of proof, and you read to me a standard called the "preponderance of the evidence."
Do you recall that?
A Yes.
Q Was there any instance in preparing your

rebuttal declaration that you felt you had to weigh evidence?

MR. BERKOWITZ: Objection to form.

A I don't recall any. It was all black and white, straightforward.

BY MR. HELGE:

Q So your opinions aren't based on any sort of weighting one piece of evidence against another; is that right?

MR. BERKOWITZ: Objection to the form.

A Each of the questions that I had when I read the '843 and Ham, the petition, the patent owner's response, Bohannon's response, I understood it to be black and white and didn't need to apply, you know, was I 2 percent off in this analysis or anything like that. It was black and white and straightforward.

MR. HELGE: Why don't we take a five-minute break? Going off the record at 3:31.

(Whereupon, a brief recess is taken.)

MR. HELGE: Going back on the record at 3:46.

BY MR. HELGE:

Q Mr. Marentic, can you go back to your rebuttal

declaration, page 37? This is for the '843 patent.

A 37 of 41? Yes.

MR. BERKOWITZ: Just give me a second to get there.

MR. HELGE: Sure.

BY MR. HELGE:

Q Is it correct that you disagree with Mr. Bohannon's construction for control a transmission rate?

A That is correct.

Q Okay. And you'd commented on that disagreement in paragraphs 89 and 90, correct?

A Yes.

Q Can you please take a look at paragraphs 89 and 90?

As you look through them, please let me know if at any instance you discuss the '843 patent's actual use of that phrase, "control a transmission rate."

MR. BERKOWITZ: Objection to the form.

BY MR. HELGE:

Q Well, I'll take a step back, then.

You're familiar with the '843 patent, correct?

A Correct.

Q Are you aware whether the '843 patent uses the term "control a transmission rate" outside of the claims?

A It doesn't come to me to find it somewhere immediately. It may or may not. I could search through it.

Q But sitting here right now you don't recall whether it actually uses that term in the specification?

A Outside --

Q Of the claims.

A -- of the claims?

No, I don't recall.

Q You don't recall.

And if you look through paragraphs 89 and 90, does that refresh your recollection at all?

MR. BERKOWITZ: Objection to form.

A No, that doesn't refresh my memory as to whether controlling a transmission rate is in this -- in the patent outside the claims or not.

BY MR. HELGE:

Q Okay. But you don't discuss anywhere in here

how the '843 patent actually uses that term in the detailed description, do you?

MR. BERKOWITZ: Objection to the form.

A "That term" being "controlling transmission rate"?

BY MR. HELGE:

Q Yes, sir.

A I -- ask the question again.

Q Sure. In paragraph 89, is there any mention by you of how the '843 patent uses the term "control a transmission rate" outside of the claims?

A Well, there's a couple of times that it's in there, the first one referring to Claim 4.

Q How about the second time?

A I'm citing to other papers.

Q And in paragraph 90, do you discuss how the '843 patent specification outside the claims uses the term "control a transmission rate"?

A Yes.

Q And where does that occur?

A There's a discussion of a couple of cites at the bottom of column 1.

Q And both citations are from column 1 and the top of column 2, correct?

A Correct.

Q Okay. And we -- or actually you read through all of Shen's description of the prior art and you acknowledged that nowhere in that background does Shen use that term, "control a transmission rate"; isn't that right?

MR. BERKOWITZ: Objection to the form.

A I believe that's true, yes.

BY MR. HELGE:

Q And do you agree that column -- excuse me.

Do you agree that the bottom of column 1 and the top of column 2 are contained within the description of the prior art discussion of Shen?

A That is correct.

Q Okay. So both of these citations in paragraph 90 are citations to the description of the prior art of Shen, correct?

A Correct. And the argument is: You can control the transmission rate as they've done since the first liquid crystal display was invented, by applying

different voltages. And that transmission rate is directly related to the voltage across the liquid crystal display. So, to me, "controlling the transmission rate" is not a particularly important term. It is two separate terms, to control, control the voltage across the pixel. That voltage across the pixel causes a certain molecular disturbance in the order of the liquid crystal lattice structure and will cause different amounts of light to go through. So there is a -- you control the voltage, you control the liquid crystal orientation and you end up by controlling the amount of light transmitted, or the transmittance or the percent transmission. Or, as Shen uses the term, "transmission rate." So, to me, transmission rate gets lumped together and control is a separate verb.

And it is possible to control the transmission rate as they did in the prior art, as they did for at least a decade prior, without overdrive. So Mr. Bohannon's argument that a non-overdriven scenario does not control the transmission rate is just false. It's been done for a decade prior to Shen, the '843 patent. You control the transmission rate with a

voltage. The physics behind it is you disturb the LC molecules in the matrix and that changes the amount of light through it. So transmission rate is one thing and controlling is a separate item, and I don't ascribe any significance that controlling the transmission rate together was used in the claim.

Q And so your conclusion about the meaning of that term comes exclusively from your background experience; isn't that right?

MR. BERKOWITZ: Objection to the form.

A The background of transmission rate, transmittance, percent transmission come from my background, and controlling is just a common, ordinary term.

BY MR. HELGE:

Q So that also comes from your background?

A Well, that comes from anyone that speaks English.

Q In your view, you can control a transmission rate simply by changing a voltage, right?

A Correct. The voltage across the pixel.

Q Does it matter whether you reach a target

transmission rate in a certain time period?

MR. BERKOWITZ: Objection to the form.

A Reaching a desired transmission rate is a response issue, separate and distinct. So there is a going from a transmission rate of T1 to a transmission rate of T2. If that is a step function, that might occur quickly if the step were small. It could occur slower if the step was from gray level zero to gray level 255. And the time that it takes is the response time.

BY MR. HELGE:

Q Is that based on -- that explanation that was provided, is that based on your experience as well?

A Background in everything electronics. There's always transition times. Transition time of a clock signal, transmission time of zero to one in a logic circuit, a one to a zero in a logic circuit. Transmission times are separate from transmission rate.

So, for instance, a clock signal might go from zero to 3.3 volts. And there is a boundary where you call it -- at 10 percent of the transition, and then another boundary where you go to 90 percent of the

transmission -- transition voltage of 3.3 volts. And the amount of time that it takes to go from 10 to 90 percent is the transition time for that clock signal, or any logic signal. It's just understood. These things are measured routinely in electrical engineering. And in this patent, the transition time can be measured for the change in transition, transmission rate.

Q So from your view, controlling a transmission rate solely looks at the Y-axis response and has nothing to do with the X-axis time; is that right?

A It's both axes.

Q So to know whether something is controlling a transmission rate requires you to also evaluate the time for changing transmission rates?

MR. BERKOWITZ: Objection to the form.

A The transmission rate is simply a value.

BY MR. HELGE:

Q Is it on the Y-axis?

A It could be plotted on the Y-axis.

Q Okay.

A And it's similar to, say, mortgage rate. The mortgage rate for most banks is 5 percent, and at the

beginning of next month the mortgage rate may go to 10 percent. So the transition time from 5 to 10 percent for the mortgage rate is one month.

If we were talking about percent transmission, going from one value to a second value is measured in time, and the amount of time is going to be dependent on how big that step is. If it were a single gray level step, the eye might not see it at all. If it was full black to full bright, and frame to frame, this white sphere moved across the screen, there might be blurring. And in order to measure that, you would input a black pattern, change it to a white pattern and look at the brightness that comes through the display.

Q Let's focus on one pixel here. If we're going -- if we're looking at one pixel, and we're going from a first transmission rate to a target transmission rate, within a frame.

A Yes.

Q If we cannot reach the target transmission rate within that frame, is that still controlling a transmission rate?

MR. BERKOWITZ: Objection to the form.

A So as I understand, the step is large enough that it can occur in one frame time?

BY MR. HELGE:

Q That's right.

A And the transmission rate is going from one level and not quite getting to a second level?

Q Correct.

A That transmission rate is being controlled.

Q In your view, it's being controlled?

A Yeah.

Q Do you recall we were talking about the reasons for allowance before lunch, the examiner's reason for allowance? And you compared the examiner's reasons for allowance against paragraph 53 of Ham.

Do you recall that?

A Yes.

Q And you compared it line for line, word for word, correct?

A I attempted to.

Q Okay. You identified some punctuation that was different in the two?

A And the lead-in sentence and -- yes.

Q Do you have Ham available to you there, paragraph 53, specifically?

A Yes.

Q Okay. Now, the examiner quoted portions of this paragraph and the reasons for allowance, right?

A Yes.

Q As a matter of fact, I believe the examiner quoted, beginning on the second line of paragraph 53, "apply the normal data to the liquid crystal panel at the initial half period of the frame after supplying of the modulated data to the liquid crystal panel during the later half period of the frame."

Do you recall that being quoted in the reasons for allowance?

A Yes.

Q Okay. Does that correspond with your understanding of what's disclosed in Ham?

MR. BERKOWITZ: Objection to the form.

A That is a sentence that is -- could be helped with some punctuation, but that does describe what is happening in Ham.

BY MR. HELGE:

Q So Ham is applying an overdriven pulse in half of the frame and a non-overdriven pulse in another half of the frame; is that right?

A Correct.

Q And that's how the examiner interpreted Ham as well, right?

MR. BERKOWITZ: Objection to the form. Foundation.

A I don't know how the examiner -- what was in the examiner's head.

BY MR. HELGE:

Q Sure. I understand that.

But the examiner relied upon paragraph 53 to ascribe the reasons why Claims 1 through 9 of Shen were allowable, right?

MR. BERKOWITZ: Objection to the form. Foundation.

A That was one of the items cited in the allowance.

BY MR. HELGE:

Q So as far as we can tell from the reasons for allowance, the examiner had the same understanding of

Ham as you do; isn't that right?

MR. BERKOWITZ: Objection to the form. Foundation.

A I don't know what the examiner had in mind. As I understand, during the first half, there is an impulse applied, and that is from the look-up table, Table 1, page 8 of 11. And that look-up table describes what to do based on the prior frame and the current frame. And that data that is looked up is applied to the source driver and an impulse is generated at the first half of the frame time, and later the commanded input data is applied during the second half of the frame.

BY MR. HELGE:

Q So the paragraph that the examiner cited in the reasons for allowance described that technique as well, right?

MR. BERKOWITZ: Objection to the form.

A They describe it in a little less detail, but they describe an initial half period and a latter half period. Ham, again, the initial half period is modulated data, and later in the frame, the normal data,

or the data that was input to the TCON.
BY MR. HELGE:
Q So the examiner cited to a paragraph that you agree accurately describes Ham, and even in view of that, the examiner allowed Claims 1 through 9?
MR. BERKOWITZ: Objection to the form. Foundation.
BY MR. HELGE:
Q How do you explain that?
A Well, as I said before, paragraph 53 could be helped with some punctuation. The examiner cited that paragraph, allowed it. And, upon Sharp petitioning for a reexamination, the current Patent Trial and Review Board allowed a reexamination, which is why we're here today. So, yes, the original examiner allowed Claims 1 through 9, but the current Patent Trial and Review Board have found the arguments persuasive enough from the petition to allow for the reexam.
BY MR. HELGE:
Q So you have no theory on why the examiner allowed the case?
MR. BERKOWITZ: Objection to the form.

BY MR. HELGE:

Q In the first round?

MR. BERKOWITZ: Objection to the form. Foundation.

A Why the examiner -- no, I have no theory on why the examiner did what he did back in 2001 or whatever the applicable date is. And even today, I have no idea what the examiner is thinking.

MR. HELGE: Your witness.

MR. BERKOWITZ: You have no further questions?

MR. HELGE: No further questions.

MR. BERKOWITZ: I'm going to take ten minutes.

MR. HELGE: I do obviously reserve the right to re-cross.

MR. BERKOWITZ: Understood. I'm just going to take 10 or 15 minutes and come back.

THE VIDEOGRAPHER: Okay. Going off record at 4:10.

- - -

EXAMINATION BY MR. BERKOWITZ:

- - -

Q Mr. Marentic, if you don't mind, can you take

out two documents; that is what we've marked earlier as Exhibit B, and also your declaration that is Exhibit 1010, Sharp Exhibit 1010.

If you could turn to page 19 of Exhibit B. And if you could turn to paragraph 42 of your declaration, which is on page 19 of 41.

A Which paragraph was that?

Q I'm sorry, paragraph 42 of your declaration.

A 42, yes.

Q Do you recall a discussion earlier of the level of skill in the art as described in Exhibit B on page 19 and the level of ordinary skill in the art described in paragraph 42 of Exhibit 1010?

A Yes.

Q And you noted earlier there were some differences between those two levels of skill in the art; is that correct?

MR. HELGE: Objection to form. Leading.

BY MR. BERKOWITZ:

Q You can answer.

A We discussed there were differences in the description of a person of ordinary skill in the art.

Q Did those differences affect your opinions as to the invalidity of the Claims 4, 8 and 9 of the '843 patent?

A No.

Q Okay. I just want you to take a look at the '843 patent for a second. You can put those aside for now.

If you don't mind, turn to Claim 4, which appears on page 15 of 15. And if you don't mind, just read through Claim 4 on your own from -- starting at column 7, line 1 through line 19.

(Whereupon, witness reads the document.)

A Okay, I've reread that.

BY MR. BERKOWITZ:

Q Thank you. In your opinion, are there any terms in Claim 4 that require claim construction?

MR. HELGE: Object to form.

A I don't believe so.

BY MR. BERKOWITZ:

Q Why not?

A The original petition didn't ask for any terms to be construed. The preliminary response by patent

owner did not ask for any terms to be construed. And the decision by the Patent Trial and Review Board also declined to construe any of the terms. And when I read it through, probably the second time, there was nothing that was difficult or out of the ordinary from my experience.

MR. BERKOWITZ: Thank you. I have nothing further.

Wayne?

- - -

EXAMINATION BY MR. HELGE:

- - -

Q Mr. Marentic, I'm just going to ask for clarification on your last answer.

You state, "When I read it through, probably the second time."

What were you referring to when you said "it"?

A The '843 patent in total.

Q And do you know the standard for claim construction or the test for claim interpretation before the Patent Trial and Appeal Board in this proceeding?

MR. BERKOWITZ: Objection to form.

A In my declaration, there is a Section V, Claim Construction: "Patent claims are to be given their 'broadest reasonable' construction in light of the specification as would be read by a person of ordinary skill in the art."

Next paragraph: "I understand that the Petition asserted that Claims 4, 8 and 9 of the '843 patent 'are generally clear on their face, and should be given their broadest reasonable construction in light of the construction'" -- "'in light of the specification of the '843 patent.' Likewise, I understand that, in instituting this proceeding, the Board did not find it necessary to construe any terms of Claims 4, 8 and 9."

BY MR. HELGE:

Q And do you believe you followed that standard in preparing your opinion in your rebuttal declaration?

A I believe I have, yes.

MR. HELGE: No other questions.

MR. BERKOWITZ: Okay.

THE COURT REPORTER: Can you state your orders?

MR. HELGE: We'd like a final copy by this

Friday.

MR. BERKOWITZ: That's fine with us.

THE COURT REPORTER: Do you want rough drafts?

MR. BERKOWITZ: I don't. I just want to state on the record that I want Mr. Marentic to have an opportunity to review his transcript from today and sign.

(Whereupon, at 4:34 p.m., the deposition concluded.)

_____

MICHAEL J. MARENTIC

Subscribed and sworn to
before me this ____ day
of _____, 2015.

_____

Notary Public

CERTIFICATE OF CERTIFIED COURT REPORTER

I, Dana N. Srebrenick, CRR, CLR, Notary Public in and for the State of New York do hereby certify:

That MICHAEL J. MARENTIC, the witness whose deposition is hereinbefore set forth, was duly sworn by me before the commencement of such deposition and that such deposition was taken before me and is a true record of the testimony given by such witness.

I further certify that the adverse party, was represented by counsel at the deposition.

I further certify that the deposition of MICHAEL J. MARENTIC, occurred at the offices of AMSTER ROTHSTEIN & EBENSTEIN LLP, 90 Park Avenue, New York, New York 10016 on Tuesday, October 6, 2015 commencing at 9:30 a.m. to 4:34 p.m.

I further certify that I am not related to any of the parties to this action by blood or marriage, I am not employed by or an attorney to any of the parties to this action, and that I am in no way interested, financially or otherwise, in the outcome of this matter.

IN WITNESS WHEREOF, I have hereunto set my hand and affixed my notarial seal this 9th day of October 2015.

My commission expires:

6/30/16

Dana N. Srebrenick

DANA N. SREBRENICK, CCR, CRR, CLR

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

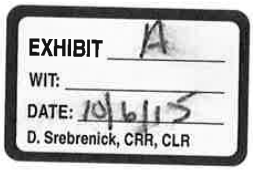
SHARP CORPORATION, SHARP ELECTRONICS CORPORATION, and SHARP ELECTRONICS MANUFACTURING COMPANY OF AMERICA, INC.,
Petitioners

v.

SURPASS TECH INNOVATION LLC,
Patent Owner

Case IPR2015-_____
Patent No. 7,420,550

DECLARATION OF MICHAEL J. MARENTIC IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 7,420,550



600321.1

1. I, Michael J. Marentic, make this declaration in connection with the Petition for *Inter Partes* Review submitted by Sharp Corporation, Sharp Electronics Corporation, and Sharp Electronics Manufacturing Company of America, Inc. (collectively "Petitioners" or "Sharp") for review of Claims 1 through 5 of U.S. Patent No. 7,420,550 to Yuh-Ren et al. ("the '550 Patent"), which is assigned to Surpass Tech Innovation LLC ("Patent Owner" or "Surpass").

2. Throughout this declaration, I refer to exhibit numbers that correspond to the exhibits to the Petition for *Inter Partes* Review for which I provide this declaration.

Scope of My Assignment

3. I have been requested by counsel for Sharp to study the '550 Patent, including its claims and prosecution history, as well as the references specifically referred to in this declaration. I have also been requested by counsel for Sharp to provide my expert opinion regarding the invalidity of Claims 1-5 of the '550 Patent. I further expect to offer an additional declaration in response to any declaration submitted by any expert for the Patent Owner.

Summary of My Opinions

4. It is my opinion that Claims 1-3 of the '550 Patent are invalid as anticipated under 35 U.S.C.§ 102(b) and Claims 4-5 are obvious to a person of ordinary skill in the art under 35 U.S.C. §103(a). Moreover, it is my opinion that in addition to being anticipated, Claims 1-3 are also rendered obvious over prior art.

5. Specifically, I believe that the following are grounds to find Claims 1-5 of the '550 Patent invalid:

a. Claims 1-3 are invalid under 35 U.S.C. § 102(b) as anticipated by Japanese Patent Application Publication No. H08-305322 (Ex. 1002, "the Sharp Reference").

b. Claims 1-3 and 5 are also invalid under 35 U.S.C. § 103(a) as obvious over the Sharp Reference.

c. Claims 1-5 are also invalid under 35 U.S.C. § 103(a) as obvious over the Sharp Reference in view of U.S. Patent No. 6,407,795 to Kamizono, et al. (Ex. 1004, "Kamizono").

d. Claims 1-5 are also invalid under 35 U.S.C. § 103(a) as obvious over U.S. Patent No. 6,081,250 to Shimada et al. (Ex. 1003, "Shimada") in view of Kamizono.

Summary of My Professional Background and Qualifications

6. Exhibit 1008 is my *curriculum vitae* which sets forth my professional background and qualifications. A list of publications that I have authored or co-authored is included.

7. I have many years of experience in the flat panel display industry. I first became involved in the flat panel display industry in 1973, when I began working at the University of Illinois Coordinated Science Laboratories where the AC Plasma Display Panel

("PDP") was invented. During my studies at the University, I was employed as an intern working in the area of plasma display construction and gas discharge physics characterization. I received a B.S. degree in Engineering Physics from the University of Illinois.

8. Upon entering graduate school, I continued my work on the characterization of the gas discharge in the pixels. I received an M.S. degree in Electrical Engineering from the University of Illinois, and wrote my master's thesis on measuring the electron density in an AC PDP.

9. One of my engineering positions was with Interstate Electronics Corporation (IEC) as a design electrical engineer. IEC designed drive electronics, mechanically packaged the display modules, and incorporated them into terminals for harsh, military environments. I designed several distinct versions of drive electronics for PDPs, including one using packaged silicon integrated circuits on flexible circuits, or "chip-on-flex." During this time, I was awarded several patents relating to PDP technologies. I also investigated LCDs and thin film electroluminescent displays for incorporation into military applications.

10. I later formed Plasma Displays, Inc., a single proprietorship consulting corporation. I worked for several clients, one being Bell Laboratories and AT&T at their joint Reading, Pennsylvania facility. This facility was where the original picture phone was developed, the first commercial light emitting diodes ("LEDs") were manufactured, and

AT&T's PDPs were developed and manufactured. I worked on PDP drive electronic design, driver-to-panel interconnect reliability, driver circuit characterization, and yield improvement.

11. I was a founder and Vice President of Plasmaco, a company that acquired IBM's PDP production line in New York. Plasmaco manufactured several types of PDPs, including VGA panels with 640x480 pixels for early notebook computers. Such a panel had 5 driver ICs with 32 outputs per driver for 640 data lines. I also developed larger sized VGA panels with 1280x1024 pixels. Because of the increase in size, we used the same type of driver IC chips but doubled the number of driver ICs (i.e., using 10 driver ICs) in the display. When changing the panel design to increase the size of the panel and/or the number of pixels, it was a common practice to keep the same type of driver IC as the smaller panel, but it was necessary to increase the number of driver ICs to accommodate the added pixels in the larger display.

12. While at Plasmaco, I also developed and manufactured driver chip-on-glass ("COG") technology that passed extreme militarized environmental testing specifications. COG technology put electrode driver integrated circuits onto the glass edges of the PDP. The benefits of using COG technology were that it reduced the physical size and weight of a notebook computer display and increased the operational reliability of the display.

13. At Science Applications International Corporation, I worked on efficient backlights for LCDs, some for direct viewing in sunlight. Commercially available LCDs were

disassembled and repackaged with these backlights. The finished displays were used in cockpit avionics, medical, banking, and FAA towers.

14. At Hitachi, from 1995 to 1999, I managed a technology center that developed technologies relating to the interface between the motherboard and the LCD driver chips for flat panel monitors and notebook displays. I reported directly to the LCD design and manufacturing center in Japan. I had access to future LCD technical details and specifications, and facilitated technology transfer between Silicon Valley firms and Japan management. The Video Electronics Standards Association ("VESA") writes and publishes video standards for the electrical interfacing for displays. I was the chairman of the VESA flat panel display committee, a member of the board of directors, and later the president of the board of directors.

15. While at Philips, from 1999 to 2001, I managed a group of engineers that designed electronics for flat panel displays. My group designed interface timing ICs and video processing circuit boards for monitors and televisions utilizing LCDs. My group also worked with an IC design firm to develop the design of source and gate driver ICs for enhanced performance LCDs having various sizes. The enhanced performance LCDs were developed to provide high brightness and used multiple driver ICs, as well as the COG technology.

16. Philips invested in a tiled LCD display company, and I participated in the technology development using Philips panels. My group designed circuits and assisted with their incorporation into commercial products within Philips' worldwide subsidiaries.

17. Philips purchased the LCD factory of the Korean company LG, and later formed a joint venture called LG-Philips LCD. I was a member of the group of technical advisors that performed the due diligence for Philips for the purchase.

18. At Alien Technology, I was a member of the integrated design team that produced custom drivers made for cholesteric LCD displays, organic LEDs, and polymer dispersed LCDs. My responsibilities were IC product definition for the drivers and system architecture. Driver ICs were fabricated at silicon foundries and formed into small die for mass assembly utilizing Alien's fluidic assembly onto flexible, very low cost displays. Since Alien's products were very small sized, low cost LCDs, they typically involved only a single source driver and a single gate driver, whereas the larger sized LCD panels that I worked on while at Hitachi and Philips had multiple source and gate drivers.

19. I am the named inventor or co-inventor on three U.S. patents in the PDP field.

Materials Considered

20. In forming my opinions, I reviewed the following documents referenced by their exhibit number in the Petition for *Inter Partes* Review of the '550 Patent:

EXHIBIT NO.	DESCRIPTION
1001	U.S. Patent No. 7,420,550 to Shen et al. ("'550 Patent")
1002	Japanese Patent Application Publication No. H08-305322 and Certified English Translation Thereof ("Sharp Reference")
1003	U.S. Patent No. 6,081,250 to Shimada et al. ("Shimada")
1004	U.S. Patent No. 6,407,795 to Kamizono et al. ("Kamizono")
1005	Prosecution History of U.S. Appl. No. 10/929,473
1006	U.S. Patent No. 5,805,128 to Kim et al. ("Kim")
1009	U.S. Patent Application Publication No. US 2003/0048249 A1 to Sekido et al. ("Sekido")

21. I also base this declaration on my knowledge from my 30 years of experience working on liquid crystal display (LCD) and related technologies.

22. I reserve the right to amend or supplement this declaration based upon any reports by any expert(s) for the Patent Owner, or any new documents and/or other information that becomes available.

Compensation

23. I am being compensated at my consulting rate of $250 per hour for my time spent in connection with this case. I am being separately reimbursed for any out-of-pocket

expenses. No part of my compensation is dependent upon the outcome of this proceeding or the nature of the opinions that I express.

Legal Standards

24. To render my invalidity analysis, I have been informed about the legal standards for patent invalidity in *inter partes* review proceedings before the Patent Trial and Appeal Board.

25. Specifically, I understand that the petitioner must prove patent invalidity by a "preponderance of the evidence," that there is no "presumption of validity" in *inter partes* review proceedings, and that claims are to be given their "broadest reasonable" construction in light of the specification as would be read by a person of ordinary skill in the art.

26. I also understand that a patent claim may be invalidated as anticipated if a single prior art reference discloses, either expressly or inherently, each and every element of the patent claim.

27. I also understand that a patent claim may be invalidated by one or more references, either alone or in combination, as being "obvious" to a person of ordinary skill in the art at the time the invention was made.

28. I understand that one way of demonstrating obviousness in the situation where a prior art reference discloses a single element but the claim requires multiple elements is to demonstrate that there are no new and unexpected results from increasing the number of such elements.

29. I further understand that an additional way of demonstrating obviousness is to demonstrate that one or more items of prior art either alone or in combination, contain all of the elements of a claim.

30. It is my understanding that in considering the issue of obviousness, I should consider what a person of ordinary skill in the pertinent art would have known at the time of the invention, as well as what such a person would have reasonably expected to have been able to do in view of that knowledge.

31. I understand that in analyzing the issue of obviousness, I should consider and determine: (1) the scope and content of the prior art; (2) the differences between the prior art and the claims at issue; and (3) the level of ordinary skill in the pertinent art.

32. I further understand that any of the following may provide a "reason" for combining elements known in the prior art: (a) a need or problem known in the field at the time of invention and addressed by the patent; (b) an obvious use of familiar elements beyond their primary purposes; (c) a design need or market pressure to solve a problem; (d) a simple substitution of one known element for another that would provide predictable results; (e) the use of known techniques to improve similar methods or products in the same way; or (f) some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

33. I also understand that claims may be invalid if they are directed to obvious design choices. Specifically, I understand that a patent claim that simply arranges old elements with each performing the same function it had been known to perform is not patentable. The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results.

34. I also understand that certain "secondary considerations" of non-obviousness may be considered, to the extent that they exist. It is my understanding that such secondary considerations include, among others: (a) commercial success; (b) long felt but unsolved needs; and (c) the failure of others. I understand that there must be some connection to the secondary considerations and the claimed invention. I reserve my right to address any evidence or opinions the patent owner may submit on this issue.

THE '550 PATENT

35. I understand that the application leading to the '550 Patent was U.S. Patent Application No. 10/929,473, which was filed on August 31, 2004. For the purposes of my analysis, I assume that the time of the purported invention was August 31, 2004.

36. The '550 Patent relates to an active matrix liquid crystal display (LCD) device and driving circuit for the LCD device. In particular, the '550 Patent describes a specific way of connecting the gate and data lines to the thin film transistors (TFTs) driving pixels in an LCD panel.

LCD Panels and Driving Devices Were Known in the Prior Art

37. As acknowledged in the '550 Patent, active matrix LCD panels and the use of data and gate lines, or source and gate drivers for TFTs in LCD panels were all known in prior art. (Ex. 1001, '550 Patent, Col. 1:23-61, Figs. 1A-1B).

38. As shown below by multiple shaded blocks in annotated Figure 1A of the '550 Patent, the "Prior Art" driving circuit for LCD panels included multiple source drivers 11 and multiple gate drivers 12. (*Id.* at Fig. 1A). The source drivers 11 (purple boxes) provide image signals (i.e., video signals) to an LCD panel 10 through a plurality of data lines 111 (purple lines), while the gate drivers 12 (orange boxes) provide scanning signals (i.e., control signals) to the LCD panel 10 through a plurality of gate lines 121 (orange lines).

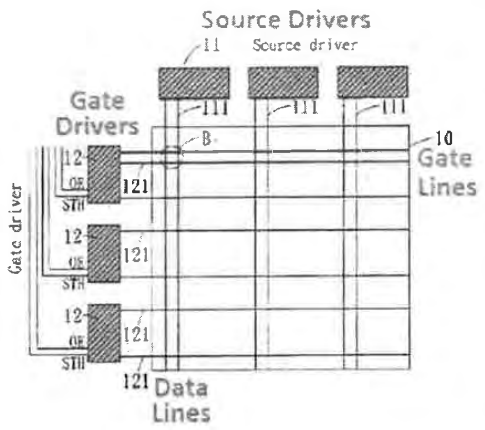


Fig. 1A (Prior Art)

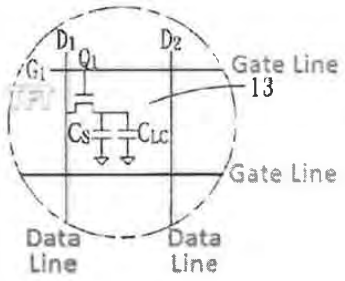


Fig. 1B (Prior Art)

39. As shown above in Figure 1A, prior art LCD panels included data lines 111 and gate lines 121 arranged in a matrix array.

40. According to the '550 Patent, the data lines 111 and gate lines 121 in the "Prior Art" shown in Figures 1A and 1B are "insulated with each other." (Ex. 1001, '550 Patent, Col. 1:45-47).

41. As shown above in Figure 1B, a pixel 13 in this prior art LCD panel is formed within each area enclosed by intersecting data lines (e.g., purple line D_1) and gate lines (e.g., orange line G_1).

42. As the '550 Patent acknowledges, each pixel 13 in prior art LCD panel included a thin film transistor Q_1 (TFT, highlighted in yellow), which is switched on and off by a control signal from the gate driver 12 through a gate line G_1.

43. The source of the TFT Q_1 receives the image signal sent from the source driver 11 through the data line D_1. An output voltage from the TFT Q_1 drives liquid crystal molecules corresponding to the pixel 13 to form an image. (*Id.* at Col. 1:45-57, Fig. 1B).

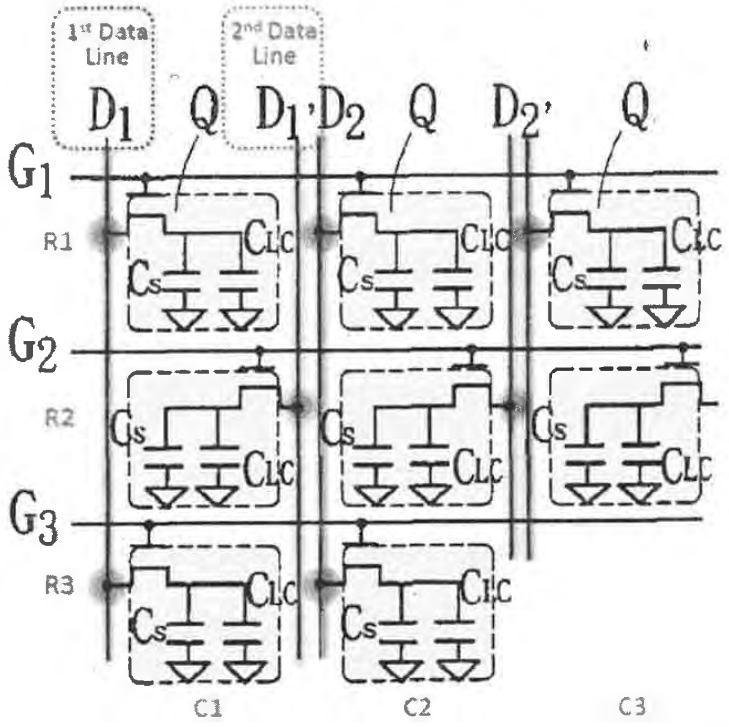
44. The time that an LCD needs to react to the driving voltage output by each TFT is called "response time," and the video quality of an LCD panel is dependent on this response time. In this regard, the video quality may be poor if the LCD response time is too long. (*Id.* at Cols. 1:62-2:41).

The Alleged Invention of the '550 Patent

45. According to the '550 Patent, its "chief object" is to provide an LCD driving circuit having a matrix structure in which the gate and data lines are connected to the TFTs in a specific way that allegedly increases "the response speed" of the LCD. (*Id.* at Col.

3:18-20, 35-40). This configuration is shown in, for example, Figure 4B, which is reproduced below.

'550 Patent Fig. 4B



46. As shown above in annotated Figure 4B, the driving device includes a matrix array formed from rows (R1-R3) and columns (C1-C3) of TFTs (Q). Each TFT in the matrix is associated with a pixel (represented by the dashed rectangles). The driving device further includes a certain number ("N") of gate lines G_i (i=1, 2, ... N), and a certain number ("M") of groups (e.g., pairs) of data lines D_j and $D_{j'}$ (j, j'=(1,1'), (2, 2'), ... (M, M')). For

example, as shown in Figure 4B above, the driving device has three gate lines, G_1, G_2, and G_3, and two groups of data lines ((D_1, $D_{1'}$) and (D_2, $D_{2'}$)).

47. As shown in Figures 4A, 5A, and 6A, the '550 Patent describes a source driver with a limit of 60 Hz but provides no further explanation or specification. Absent in the '550 Patent is the number of drive channels or outputs per source driver and matrix size. One would calculate the number of required driver ICs by dividing the horizontal pixel count by the number of drive channels per data driver. The driving device shown in Figure 4A uses 60 Hz source drivers; it doubles the normal calculated number of source drivers and mounts them on a single glass panel edge. The driving device shown in Figure 5A also uses 60 Hz source drivers; it again doubles the normal calculated number of data drivers, but mounts them on both the top and bottom edges of the panel with an interdigitated column connection. The driving device shown in Figure 6A uses 120 Hz or faster source drivers, mounted on one panel edge, and then adds dual switches to each output channel for driving the paired data electrodes.

48. The '550 Patent does not discuss the benefits or reasons for including a single source driver and a single gate driver on the one hand, and having a set of multiple source and gate drivers on the other hand.

49. Multiple source and gate drivers were commonly used in the prior art, particularly LCD panels as they increased in screen size. In fact, when I was in the LCD industry before the filing date of the '550 Patent, it was a common practice to change the

panel design to increase the size of the panel and/or the number of pixels by simply adding more driver ICs. For example, while the ***small***, low cost LCD panel (which had an equivalent pixel dimension of 7×4) that I worked on at Alien Technology had only a single source driver and a single gate driver, all the ***large sized*** LCD panels (which had pixel dimension of at least 800×600) that I worked on at Philips had multiple driver ICs.

50. Consistent with my experience, U.S. Patent Application Publication No. US 2003/0048249 A1 to Sekido et al. (Ex. 1009, "Sekido"), which was published on March 13, 2003, states that "in order to drive many gate bus lines and the source bus lines on the display circuit board, ***a plurality of the gate drivers and source drivers must*** be connected to the area around the liquid crystal display panel." (Par. [0006]) (emphasis added). Sekido further teaches that increasing the size of the LCD screen will increase the number of driver ICs in the panel. (Par. [0008]). Other prior art references discussed below also teach the use of multiple source and gate drivers for a large sized or high resolution LCD panel.

51. As shown above in Figure 4B, the gate line G_i (e.g., G_1, G_2, and G_3) in each row is connected to the gates of each TFT in that row. However, for each column, the first and second data lines D_j and $D_{j'}$ that form a group of data lines are not connected to all TFTs in that column. Instead, the first data line D_j in each column is connected only to the sources of the TFTs in the ***odd rows*** (see the red boxes in R1, R3, etc.) of that column,

while the second data line $D_{j'}$ in the same column is connected only to the sources of the TFTs in the ***even rows*** (see the green box in R2) that column. (*Id.* at Col. 8:10-31).

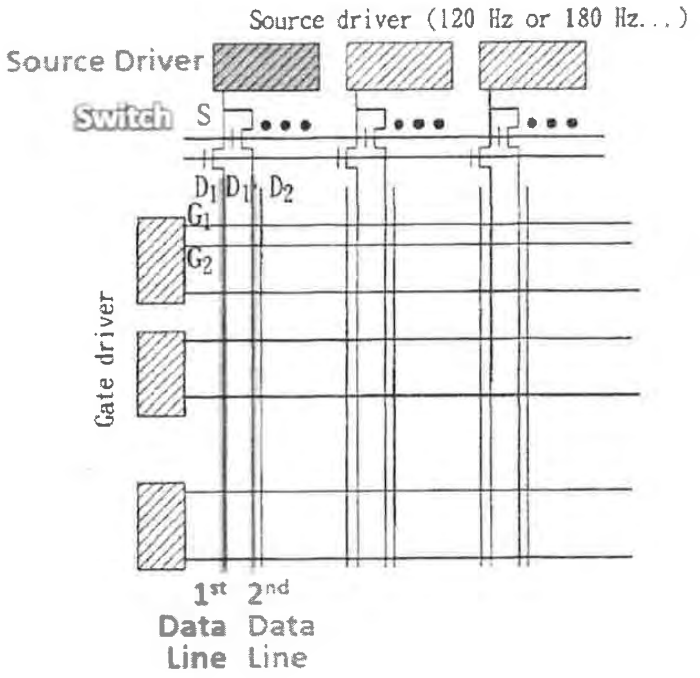
52. For example, referring to the first group of data lines D_1 and $D_{1'}$ (see the red and green lines) in first column (C1) of Figure 4B above, the first data line D_1 (see the red line) is connected to the sources (red dots) of the TFTs in the first and third rows (red boxes in R1 and R3 of the first column C1), while the second data line $D_{1'}$ (green line) is connected to the source (green dot) of the TFT in the second row (green box in R2 of the first column C1). Similarly, for the second pair of data lines (i.e., D_2 and $D_{2'}$) in the second column, the first data line (i.e., D_2) is connected to the sources of the TFTs in the first and third rows (i.e., R1 and R3 of the second column C2), while the second data line $D_{2'}$ is connected to the source of the TFT in the second row (i.e., R2 of the second column C2).

53. According to the '550 Patent, this alternating connection with the Odd Row/Even Row ("Odd Row/Even Row" configuration) reduces the response time of the LCD panel. (*Id.* at Col. 3:35-40). However, the '550 Patent does not explain how this reduction occurs.

54. The gate lines are connected to the gate driver are "insulated with each other;" and the data lines are connected to the source driver and are "insulated with each other." (Ex. 1001, '550 Patent, Col. 8:20-22, Col. 8:29-31). The '550 Patent goes on to explain that a space is provided between the neighboring data lines (e.g., $D_{1'}$ and D_2) to prevent them from short circuiting. (Ex. 1001, '550 Patent, Col. 8:31-36, Fig. 4C).

55. As shown below in annotated Figure 6A, the first and second data lines D_j and $D_{j'}$ (e.g., red and green lines D1 and D1') in each group (i.e., pair) of data lines are connected to the same source driver (purple box), and data is transferred to these data lines by an electronic switch S (highlighted in yellow). (*Id.* at Col. 5:4-8, Col. 8:50-52).

'550 Patent Fig. 6A



56. In addition, all of the source drivers are installed on the same side (e.g., upper side) of the LCD panel. (*See also id.* at Fig. 4A, Col. 8:37-38). The '550 Patent acknowledges that these components were arranged in the exact same way in the "Prior Art" in Figure 1A. (*Id.* at Col. 1:36-45, Fig. 1A).

57. The '550 Patent also states that the gate driver can be "a chip on glass or an integrated gate driver circuit on glass." (*Id.* at Col. 8:53-54). However, the '550 Patent does not define either of these terms, nor does it explain the difference between "a chip on glass" and "an integrated gate driver circuit on glass."

PROSECUTION HISTORY OF THE '550 PATENT

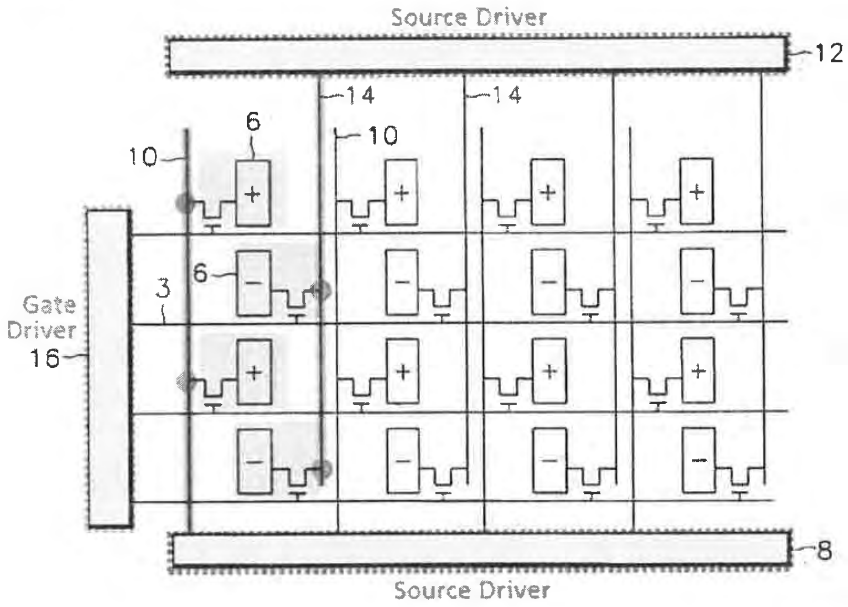
58. I understand that as originally filed, the application for the '550 Patent included claims directed to six different embodiments described in the '550 Patent. I also understand that, in response to a "Restriction Requirement" (Ex. 1005, p. 122), only the claims directed to the "First Embodiment" (i.e., "Species I; Figures 4A-4C") (*Id.* at p. 127) were elected and the claims directed to the other embodiments were canceled.

59. I understand that during prosecution, the application claim corresponding to Claim 1 of the '550 Patent was rejected as anticipated by U.S. Patent No. 5,805,128 to Kim et al. (Ex. 1006, "Kim"). (*See* Ex. 1005, p. 141). This application claim was identical to Claim 1, except that it did not include the last element of Claim 1, namely "the first data lines and the second data lines of each group of data lines are connected with the same source driver." (*See id.* at pp. 31, 152).

60. As shown below, annotated Figure 5 of Kim shows an LCD driving device of matrix structure type including the Odd Row/Even Row configuration, gate lines 3 connected to a gate driver 16, first data lines 10 connected to a data driver 8 on the bottom, and second data lines 14 connected to a data driver 12 on the top. (Ex. 1006, Kim, Col.

3:26-37, Col. 4:28-51, FIG. 5). I note that Figure 5 of Kim shows the Odd Row/Even Row configuration that is virtually identical to the one shown in Figures 5A and 5B of the '550 Patent.

Kim Fig. 5



61. In the prosecution history, I did not find any argument by the applicants disputing the Examiner's position that Kim disclosed ***all elements*** of the rejected claim, including the Odd Row/Even Row configuration and gate driver**s**. Rather, the applicants distinguished the rejected claim over Kim by including an additional claim limitation, namely that "the first data lines and the second data lines of each group of data lines are connected with the same source driver." (Ex. 1005, pp. 152, 156). The claim was subsequently allowed by the Examiner.

62. Even though Figure 5 of Kim does not disclose "the same source driver" limitation, the technique of connecting first and second data lines of each group of data lines with the same source driver in an LCD device was well known in the prior art, including the Sharp Reference and Shimada as discussed below. I understand that none of the Sharp Reference, Shimada, and Kamizono referred to in this declaration was considered by the Examiner during prosecution of the '550 Patent.

CLAIM CONSTRUCTION

63. I understand that in *inter partes* review proceedings, patent claims are to be given their "broadest reasonable" construction in light of the specification as would be read by a person of ordinary skill in the art.

64. Most of the terms of Claims 1-5 of the '550 Patent are clear to me, except for the following terms.

"The first and the second date lines of the first group of date lines"

65. Independent Claims 1 and 2 each recite that "the first and the second **date lines** of the first group of **date lines** are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the first column . . . ." (Ex. 1001, '550 Patent, Col. 19:52-56, Col. 20:13-17) (emphasis added). Nowhere else in the '550 Patent is there any mention or discussion of "date lines." I believe that the term "date lines" in this claim recitation is meant to be "data lines."

"Gate lines . . . insulated with each other" and "data lines . . . insulated with each other"

66. Independent Claims 1 and 2 each recite "a group of N gate lines . . . **insulated with each other**" and "M groups of data lines . . . **insulated with each other**." (Ex. 1001, '550 Patent, Col. 19:44-45, 51-52, Col. 20:5-6, 12-13) (emphasis added). The '550 Patent does not explain what "insulated with each other" means. Rather, the specification uses the same phrase "insulated with each other" when describing the data lines 111 and gate lines 121 shown in the "Prior Art" in Figures 1A and 1B of the '550 Patent (*id.* at Col. 1:45-47), as well as the data lines (D_1, $D_{1'}$, D_2, $D_{2'}$) and the gate lines (G_1, G_2, G_3) shown in Figures 4A-4C of the First Embodiment. (*Id.* at Col. 8:20-22, 29-31).

67. I believe that "insulated with each other" means "spaced apart from and parallel to each other." This is consistent with Figures 1A-1B of the "Prior Art" in the '550 Patent, which show that the data lines 111 are spaced apart from and parallel to each other (thereby "insulated with each other") and the gate lines 121 are likewise spaced apart from and parallel to each other (thereby "insulated with each other"). This is also consistent with all of the figures that describe the First Embodiment of the '550 Patent (e.g., Figs 4A-4C, 5A-5B, 6A-6B), which also show that the data lines (e.g., D_1, $D_{1'}$, D_2, $D_{2'}$) are spaced apart from and parallel to each other (thereby "insulated with each other"), and the gate lines (e.g., G_1, G_2, G_3) are spaced apart from and parallel to each other (thereby "insulated with each other").

"the gate drivers" and the "source drivers"

68. Independent Claims 1 and 2 refer to "gate lines connected to the ***gate drivers***" and "data lines connected to the ***source drivers***." However, the term "source driver" is not mentioned in the specification of the '550 Patent. Rather, the specification refers to "data drivers."

69. Using the broadest reasonable construction, I believe that a person of ordinary skill in the art would construe these terms as written in the plural form, that is, "the gate drivers" refer to more than one gate driver and "the source drivers" refer to more than one source driver.

70. However, the specification, drawings, and prosecution history of the '550 Patent use the terms "source drivers" and "gate drivers" to cover a variety of driving circuits and configurations known at the time of the invention. These are discussed below:

1. **"Gate Drivers" and "Source Drivers" May Refer to Multiple Driving Circuits**

71. In the certain figures in the '550 Patent, the "gate drivers" and "source drivers" are used to refer to multiple driving circuits, as shown in the "Prior Art" (e.g., Fig. 1A of the '550 Patent). As shown in Figure 1A, the "gate driver" and "source driver" each comprise multiple driver circuits (e.g., integrate circuit (IC) chips in the purple and orange boxes).

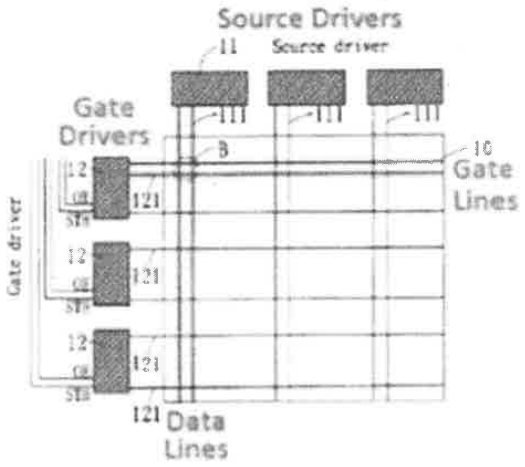


Fig. 1A (Prior Art)

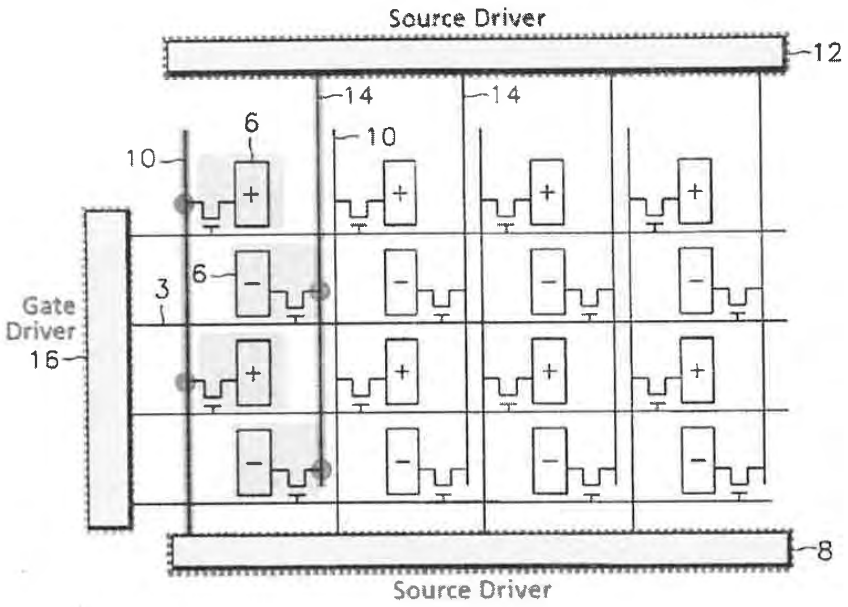
72. At the time that the '550 Patent was filed, it was widely known that such drivers could be implemented using multiple IC chips. Specifically, as LCD displays increase in size with the increased number of pixels, the number of gate lines and data lines likewise increases. However, it becomes difficult, from a packaging and cost perspective, to fabricate a ***single*** chip capable of driving ***hundreds or even thousands*** of data and source lines. Therefore, a person of ordinary skill in the art would use multiple driver IC chips in larger sized LCD panels to keep costs, time and labor down and to simplify packaging.

2. "Gate Drivers" and "Source Drivers" May Refer to A Single Circuit With Multiple Outputs

73. In addition, a person of ordinary skill in the art would understand that "gate drivers" and "source drivers" includes a single circuit (whether an IC or made up of discrete components) having multiple outputs. In that case, a person of ordinary skill in the art would understand that each data or gate line is connected to a separate "driver." This is because

each output provides a unique signal to a data or gate line. This is illustrated, for example, in the Kim reference (Ex. 1006), cited during the prosecution of the '550 Patent (discussed above). As shown below in Figure 5, the gate driver 16 of Kim is depicted as a single circuit block having multiple output lines. The Examiner found that Kim discloses the claimed "gate drivers." (Ex. 1005, p. 141). The applicants did not dispute this. The Examiner and applicants' understanding is consistent with that of a person of ordinary skill in the art at the time of the invention.

Kim Fig. 5



LEVEL OF SKILL IN THE ART

74. A person of ordinary skill in the art would have had an undergraduate degree in electrical engineering, or equivalent work experience. That person would also have had 2

to 5 years of experience designing flat panel display drive electronics, designing active matrices for LCDs, or designing IC drivers.

STATE OF THE ART

75. By the filing date of the '550 Patent in 2004, the LCD display industry had numerous multi-national companies manufacturing LCD displays in volume for various consumer applications like notebook computers, desktop monitors, televisions, pocket entertainment devices, and mobile phones. Competition for market share was fierce, and older LCD issues like limited viewing angle, display brightness, and motion blur were incrementally improved with each product introduction. As the LCD industry grew, so did the support infrastructure for liquid crystal material, substrate glass, polarizer material, backlight modules, light control films, chemicals for color filters, and silicon drive ICs. The LCD manufacturer had multiple supply sources for each of these components.

76. The LCD driver ICs for source and gate drivers were designed by companies in close communication with the panel manufacturers. These ICs use conventional single crystal silicon processing and are manufactured in multiple foundries. The time from driver specification to volume manufacture was on the order of one year. Therefore, panel manufacturers used the ICs that were available at the time of their product introductions.

77. The LCD driver ICs had increasing number of output channels, faster clocking speeds, different logic interfaces, and more features for the display manufacturers. The ICs were sold for COG assembly or Tape Automated Bonding (TAB). The COG method uses an

Anisotropic Conductive Film (ACF) for interconnection between the driver pads and the panel electrodes. The TAB method, along with numerous variations, attaches the driver die to a flexible film with copper traces. The driver outputs are connected to the panel electrodes with ACF, and the logic inputs and power to the driver are connected with ACF or conventional connectors. The display module assembly used COG and TAB extensively since the 1990's. It was also well-known at the time of the filing date of the '550 Patent that an LCD panel must include a glass substrate or other substantially transparent substrate to transmit the light from the backlight to the LCD viewer's eyes. LCD panels modulate the light generated by the backlight assembly and passed through the glass substrate (or other transparent substrate) according to the TFT drive signals. The light exits the LCD surface nearest the viewer and allows the viewer to see the visual image generated based on the electrical input signal.

78. The number and location of source and gate drivers depends on the LCD panel size, pixel size, and other market driven factors. The available drivers could be mounted on a single panel edge or both panel edges. This is true for both the gate axis and the data or source axis. This design change was made as early as the 1970s. When the drivers are attached on opposite panel edges, the interconnection density of connections per linear distance is halved, the driver's power dissipation is spread out, the data clocking rate is halved, peak currents to drivers are distributed more evenly, and the image is more uniform if electrode resistance is an issue across the panel.

79. As of the filing date of the '550 patent, workers in the field of LCD devices were aware of several developments, including:

a. active matrix LCD panels;

b. the Odd Row/Even Row configuration;

c. the use of single or multiple gate drivers and single or multiple source drivers, with the decision to use multiple drivers driven, at least in part, by the size of the LCD panel;

d. the use of chip on glass technology; and

e. the use of integrated driver circuit on glass

SHARP REFERENCE

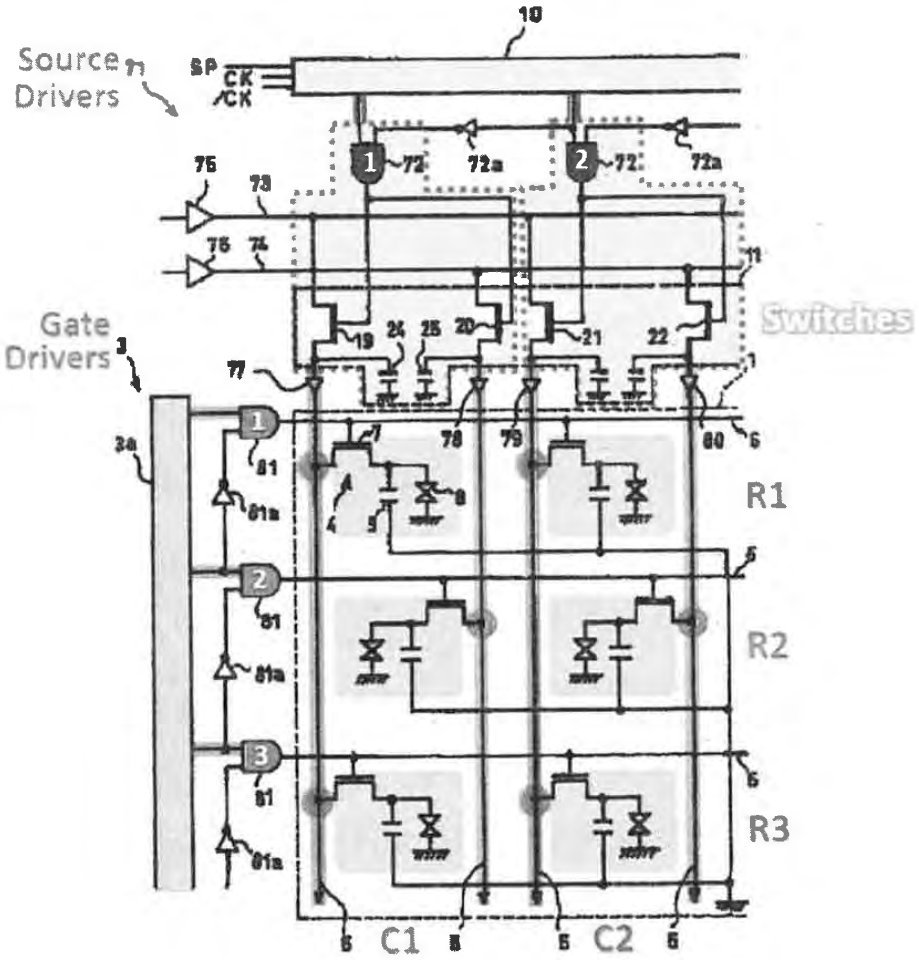
80. The Sharp Reference discloses an LCD device comprising a matrix array of thin film transistors (TFTs) 7, which drive the corresponding array of pixel units 4, as shown below in annotated Figure 10. (Ex. 1002, Sharp Reference, Pars. [0049], [0130], [0140]-[0145], FIG. 10).

81. The Sharp Reference states that its object is to improve image quality by reducing data signal noise and crosstalk (e.g., image blurring) and preventing a "ghost phenomenon" arising from the slow response time. (*Id.*, Par. [0030]).

82. The Sharp Reference also teaches that source driver circuits can be implemented in a certain way (using "driver sample hold method") to solve the problem of

insufficient image data write time arising from increasing the number of pixels in the horizontal scan direction in an LCD panel. (*Id.*, Pars. [0013]-[0019]).

Sharp Reference Fig. 10



83. As shown above in annotated Figure 10, each gate bus line 6 is connected to a gate driver 3. Specifically, each gate bus line 6 is associated with a unique AND circuit 81 (e.g., shaded in orange and labeled as "1"), and gate shift register 3a. In this way, each

gate bus line 6 is individually driven by the output of the unique AND circuit 81. (*Id.*, Pars. [0142]-[0145], FIG. 10).

84. I believe that under the broadest reasonable construction discussed above, a person of ordinary skill in the art would have understood that Figure 10 of the Sharp Reference explicitly shows multiple gate drivers. Specifically, I believe that each gate driver includes gate shift register 3a and an AND circuit 81 connected to an individual gate line 6 because they operate together to generate a non-overlapping gate pulse for each gate line 6. The first gate driver is the AND circuit "1" in communication with shift register 3a; the second gate driver is the AND circuit "2" in communication with shift register 3a; and the third gate driver is the AND circuit "3" in communication with shift register 3a. (*Id.*).

85. Annotated Figure 10 also shows groups of source bus lines 5 connected to the source drivers 71.

86. I believe that under the broadest reasonable construction discussed above, a person of ordinary skill in the art would have understood that Figure 10 of the Sharp Reference explicitly shows multiple source drivers. Specifically, I believe that each source driver includes source shift register 10, AND circuit 72, data signal lines 73, 74, sampling switches 19, 20 (or 21, 22), and sampling capacitors 24, 25 (or 26, 27). The first source driver includes AND circuit 72 (labeled "1") in communication with shift register 10, data signal lines 73, 74, sampling switches 19, 20, and sampling capacitors 24, 25. The second source driver includes AND circuit 72 (labelled "2") in communication with shift register 10,

sampling switches 21 and 22, and sampling capacitors (not numbered). (Ex. 1002, Sharp Reference, Pars. [0131]-[0140], [0145], FIG. 10).

87. As shown above in annotated Figure 10, each set of first source bus line 5 (red) and second source bus line 5 (green) in each column (e.g., C1, C2) is associated with a unique AND circuit 72 (e.g., shaded in purple and labeled as "1" and "2"). This unique AND circuit 72 operates with the associated circuit elements, i.e., source shift register 10, and a unique set of sampling switches (e.g., 19, 20) and sampling capacitors (e.g., 24, 25) to drive the first and second source bus lines (red and green lines) in each group of source bus lines 5. (Ex. 1002, Sharp Reference, Pars. [0131]-[0140], [0145], FIG. 10).

88. For example, for the first source driver in the first column C1, the AND circuit 72 obtains the output of the source shift register 10 and inputs its logical product to the gate terminals of the sampling switches 19 and 20. Meanwhile, data signals from the data signal lines 73 and 74 are respectively input to the source terminals of the sampling switches 19 and 20, and their outputs are respectively held in the sampling capacitors 24 and 25. These held output signals are then input to the first and second source bus lines 5 on both sides of pixel units 4 in the first column C1. For the second source driver in the second column C2, the AND circuit 72 obtains the output of the source shift register 10 and inputs its logical product to the gate terminals of the sampling switches 21 and 22. Meanwhile, data signals from the data signal lines 73 and 74 are respectively input to the source terminals of the sampling switches 21 and 22, and their outputs are respectively held in the sampling

capacitors (not numbered). These held output signals are then input to the first and second source bus lines 5 on both sides of pixel units 4 in the second column C2. (Ex. 1002, Sharp Reference, Pars. [0131]-[0140], [0145], FIG. 10). In this way, each set of first and second source bus lines 5 associated with each column of pixel units 4 are individually driven by a separate source driver. Accordingly, I believe that the Sharp Reference explicitly teaches multiple source drivers.

89. The Sharp Reference also teaches that the gate bus lines 6 are spaced apart from and parallel to each other (i.e., insulated with each other), and that the source bus lines 5 are likewise spaced apart from and parallel to each other (i.e., insulated with each other). (*Id.*, FIG. 10).

90. As shown above in annotated Figure 10, each gate bus line 6 is connected with the gates of all of the TFTs 7 in the row associated with that gate bus line. For example, the first gate line 6 is connected with the gates of all of the TFTs 7 of the first row (R1), the second gate line 6 is connected with the gates of all of the TFTs 7 of the second row (R2), etc. (*Id.*, Par. [0143], FIG. 10).

91. Annotated Figure 10 above also shows the claimed Odd Row/Even Row configuration. In this regard, the first source bus line 5 (red line) and the second source bus line 5 (green line) in each group of data bus lines are respectively connected with the sources of all of the TFTs 7 of the **odd rows** (red boxes in R1 and R3) and **even rows**

(green boxes in R2) of the column (C1, C2) associated with that group of source bus lines, as required by all Claims of the '550 Patent.

92. For example, the first source bus line 5 (red line) of the first group is connected with the sources (red dots) of the TFTs 7 of the first row and third row (see the red boxes in R1 and R3) in the first column C1, while the second source bus line 5 (green line) of the first group is connected with the sources (green dot) of the TFT 7 of the second row (green box in R2) in the first column C1. (*Id.*, Pars. [0131]-[0140], [0145], FIG. 10). The same Odd Row/Even Row configuration is provided in each column (e.g., C2).

93. The benefits of the Odd Row/Even Row configuration were already well known in the prior art, including the Sharp Reference. The Sharp Reference teaches that the Odd Row/Even Row configuration in an LCD Panel prevents adjacent pixel TFTs 7 in the column direction from being turned on simultaneously. This reduces the effect of data signal noise and therefore improves the video quality of the LCD panel. (*Id.*, Pars. [0144]-[0145], [0030]).

94. In this regard, I believe that the benefits of using the Odd Row/Even Row configuration became particularly significant as the size of the LCD panel and/or the number of pixels increased. When LCD screens became large enough to compete against the conventional cathode ray tube (CRT) screens, there was market and design need to improve the video quality of LCD panels. But this required increased number of pixels in an LCD panel and at the same time, a faster way to drive these pixels accurately. The Odd

Row/Even Row configuration was one of the various techniques developed in the prior art to meet this need.

95. As shown in Figure 10, the source drivers 71 for all source bus lines 5 are installed on the same side (e.g., upper side) of the display panel.

96. Figure 10 also shows that the first and the second source bus lines 5 (the red and green lines) in each group of source bus lines are connected with the same source driver. (*Id.*, Pars. [0131]-[0140], FIG. 10).

97. The transfer of data signals from the data signal lines 73, 74 to the first and the second source bus lines 5 (the red and green lines) is switched by sampling switches 19, 20 (or 21, 22) (highlighted in yellow). (*Id.*, Pars. [0134]-[0135], [0137]-[0139], FIG. 10).

THE SHARP REFERENCE ANTICIPATES CLAIMS 1-3

98. As discussed below, I believe that the Sharp Reference explicitly discloses each and every element of Claims 1-3 of the '550 Patent.

99. As shown below in annotated Figure 10, the Sharp Reference teaches an LCD device comprising a matrix array of thin film transistors (TFTs) 7, which drive the corresponding array of pixel units 4. (*Id.*, Pars. [0049], [0130], [0140]-[0145], FIG. 10).

THE SHARP REFERENCE DISCLOSES MULTIPLE GATE DRIVERS

100. As explained above in paragraph 84, I believe that Figure 10 of the Sharp Reference explicitly discloses multiple gate drivers.

101. As shown in Figure 10, gate lines 6 are connected to the corresponding gate drivers 3, as required by Claims 1 and 2.

102. Each gate driver comprises gate shift register 3a, and AND circuit 81. (*Id.*, Pars. [0142]-[0145], FIG. 10).

THE SHARP REFERENCE DISCLOSES MULTIPLE SOURCE DRIVERS

103. As explained above in paragraphs 86-88, Figure 10 also explicitly discloses multiple source drivers.

104. As shown in Figure 10, groups of data lines 5 are connected to the corresponding source drivers 71.

105. Each source driver comprises source shift register 10, AND circuit 72, data signal lines 73, 74, sampling switches 19, 20 (or 21, 22), and sampling capacitors 24, 25 (or 26, 27). (Ex. 1002, Sharp Reference, Pars. [0131]-[0139], FIG. 10).

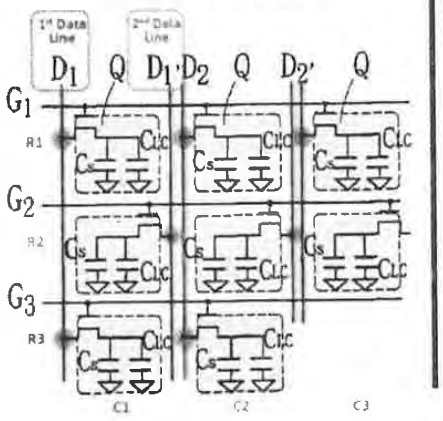
THE SHARP REFERENCE DISCLOSES THAT FIRST AND SECOND DATA LINES IN EACH GROUP OF DATA LINES ARE CONNECTED WITH THE SAME SOURCE DRIVER

106. As required by Claims 1-2, annotated Figure 10 of the Sharp Reference shows that the first and second data lines (e.g., red and green lines 5) in each group of data lines are connected with the ***same*** source driver (e.g., source driver in purple comprising source shift register 10, AND circuit 72, data signal lines 73, 74, sampling switches 19, 20 (or 21, 22), and sampling capacitors 24, 25 (or 26, 27)). (*Id.*, Pars. [0131]-[0140], FIG. 10). As discussed above, during prosecution, Claim 1 of the '550 Patent was allowed over Kim based on this feature.

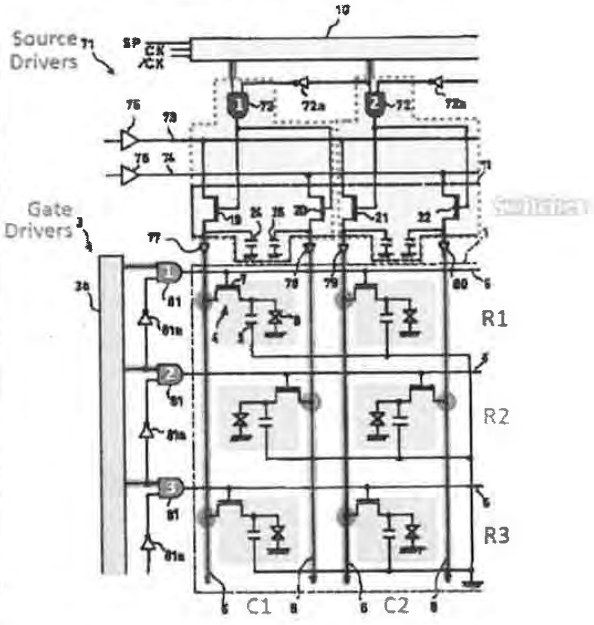
THE SHARP REFERENCE DISCLOSES THAT DATA LINES/GATE LINES ARE INSULATED WITH EACH OTHER

107. As explained above, Figure 10 of the Sharp Reference also shows that the gate lines 6 are "insulated with each other" under the broadest reasonable construction of this term since they are spaced apart from and parallel to each other; and the data lines 5 are likewise insulated with each other as they are spaced apart and parallel to each other. (Ex. 1002, Sharp Reference, FIG. 10). Indeed, the spacing (insulation) between the data and gate lines in the Sharp Reference and the '550 Patent is virtually identical, as shown below in the side-by-side comparison of Figure 4B of the '550 Patent and Figure 10 of the Sharp Reference.

'550 Patent Fig. 4B



Sharp Reference Fig. 10



THE SHARP REFERENCE TEACHES THE ODD ROW/EVEN ROW CONFIGURATION

108. The claimed Odd Row/Even Row configuration of the '550 Patent (shown on the left) is present in the LCD device of the Sharp Reference (shown on the right). (*Id.*, Pars. [0144]-[0145], FIG. 10). Specifically, the first data line 5 (see the red line) is connected to the sources (red dots) of the TFTs (red boxes) in the odd rows (R1 and R3). The second data line 5 (green line) is connected to the sources (green dot) of the TFTs (green boxes) in the even rows (R2). Figure 4B of the later '550 Patent (shown on the left) has the exact same Odd Row/Even Row configuration.

THE SHARP REFERENCE DISCLOSES THAT EACH SOURCE DRIVER IS INSTALLED ON THE SAME SIDE OF THE DISPLAY PANEL

109. Figure 10 of the Sharp Reference also shows that each source driver (e.g., source drivers in purple) is installed on the same side (e.g., upper side) of the display panel (Ex. 1002, Sharp Reference, Pars. [0130]-[0140], FIG. 10), as required by Claim 2.

THE SHARP REFERENCE DISCLOSES SWITCHES FOR DATA TRANSFER

110. Figure 10 of the Sharp Reference shows that data transfer is switched by each sampling switch 19, 20, 21, 22 (*id.*, Pars. [0134]-[0135], [0137]-[0139], FIG. 10), as required by Claim 2.

THE SHARP REFERENCE DISCLOSES A SPACE BETWEEN NEIGHBORING DATA LINES TO PREVENT SHORT CIRCUITING

111. Claim 3, which depends from Claim 2, recites that "there is a space [i.e., a gap] between the neighboring data lines to prevent them from short circuit." Figure 10 of

the Sharp Reference clearly shows a space between the neighboring data lines 5 that prevents short circuiting.

112. Just like in Figure 4B of the '550 Patent, Figure 10 shows that the first data line 5 (red) is on the left side of the pixel TFTs in the first column (C1), and the second data line 5 (green) is on the right side of the pixel TFTs in the first column (C1). This space prevents short circuiting between the first and second data lines.

113. When two neighboring data lines are shown to be spaced apart from each other in the schematic circuit diagrams for an LCD driving device, such as Figure 10 of the Sharp Reference or Figure 4B of the '550 Patent, I expect that there is a sufficient space between these data lines to prevent short circuiting. Otherwise, the LCD driving device would not be operating as described in the reference.

SHARP REFERENCE DISCLOSES EACH AND EVERY ELEMENT OF CLAIMS 1-3

114. The following claim charts summarize where I believe each element of Claims 1-3 is taught by the Sharp Reference:

The Claims Of The '550 Patent	Sharp Reference
1. A liquid crystal display driving device of matrix structure type including:	Sharp Reference discloses a liquid crystal display driving device of matrix structure type (Ex. 1002, Sharp Reference, Pars. [0001]-[0003], [0130], FIG. 10).
a group of thin film transistors with matrix array consisting of N rows and M columns of thin film transistors, wherein each thin film transistor can drive one pixel so that N×M of pixels	Sharp Reference discloses a group of thin film transistors 7 with matrix array consisting of n (e.g., 3) rows and m (e.g., 2) columns of thin film transistors 7, wherein each thin film transistor can drive one pixel unit 4 so that n×m

The Claims Of The '550 Patent	Sharp Reference
can be driven;	(e.g., 3×2) of pixel units can be driven (Ex. 1002, Sharp Reference, Pars. [0049], [0130], [0140]- [0145], FIG. 10).
a group of N gate lines connected to the gate drivers and insulated with each other, wherein the first gate line is connected with the gates of all the thin film transistors of the first row, the second gate line is connected with the gates of all the thin film transistors of the second row . . . and the N^{th} gate line is connected with the gates of all the thin film transistors of the N^{th} row; and	Sharp Reference discloses a group of n (e.g., 3) gate bus lines 6 connected to the gate drivers 3. The first gate driver is the AND circuit "1" in communication with shift register 3a; the second gate driver is the AND circuit "2" in communication with shift register 3a; and the third gate driver is the AND circuit "3" in communication with shift register 3a. The gate lines are insulated with each other by being spaced apart from and parallel to each other. The first gate bus line 6 is connected with the gates of all the thin film transistors 7 of the first row. The second gate bus line 6 is connected with the gates of all the thin film transistors 7 of the second row . . . and the n^{th} (e.g., 3^{rd}) gate bus line 6 is connected with the gates of all the thin film transistors 7 of the n^{th} (e.g., 3^{rd}) row (Ex. 1002, Sharp Reference, Pars. [0142]-[0145], FIG. 10).
M groups of data lines connected to the source drivers and insulated with each other, wherein the first and the second date lines of the first group of date lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the first column, the first and the second data lines of the second group of data lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the second column . . . and the first and the second data lines of the M^{th} group of data lines	Sharp Reference discloses m (e.g., 2) groups of source bus lines 5 connected to the source drivers 71. The first source driver includes AND circuit 72 (labeled "1") in communication with shift register 10, data signal lines 73, 74, sampling switches 19, 20, and sampling capacitors 24, 25. The second source driver includes AND circuit 72 (labelled "2") in communication with shift register 10, sampling switches 21 and 22, and sampling capacitors (not numbered). The groups of data lines are insulated with each other by being spaced apart from and parallel to each other. The first and the second source bus lines 5 of the first group of source bus lines are respectively connected

The Claims Of The '550 Patent	Sharp Reference
are respectively connected with the sources of the all thin film transistors of the odd and the even rows of the M^{th} column, and	with the sources of all the thin film transistors 7 of the odd and the even rows of the first column. . . . The first and the second source bus lines 5 of the m^{th} (e.g., 2^{nd}) group of source bus lines are respectively connected with the sources of the all the thin film transistors 7 of the odd and the even rows of the m^{th} (e.g., 2^{nd}) column (Ex. 1002, Sharp Reference, Pars. [0131]-[0140], [0145], FIG. 10).
the first data lines and the second data lines of each group of data lines are connected with the same source driver.	Sharp Reference discloses that the first source bus lines 5 and the second source bus lines 5 of each group of source bus lines are connected with the same source driver 10, 72, 73, 74, 19, 20, 24, 25 (or 10, 72, 73, 74, 21, 22, 26, 27) (Ex. 1002, Sharp Reference, Pars. [0131]-[0140], FIG. 10).
2. The liquid crystal display device of matrix structure type including:	See Claim 1 above.
a group of thin film transistors with matrix array consisting of N rows and M columns of thin film transistors, wherein each thin film transistor can drive one pixel so that N×M of pixels can be driven;	See Claim 1 above.
a group of N gate lines connected to the gate drivers and insulated with each other, wherein the first gate line is connected with the gates of all the thin film transistors of the first row, the second gate line is connected with the gates of all the thin film transistors of the second row . . . and the N^{th} gate line is connected with the gates of all the thin film transistors of the N^{th} row; and	See Claim 1 above.
M groups of data lines connected to the source drivers and insulated with	See Claim 1 above.

The Claims Of The '550 Patent	Sharp Reference
each other, wherein the first and the second date lines of the first group of date lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the first column, the first and the second data lines of the second group of data lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the second column . . . and the first and the second data lines of the M^{th} group of data lines are respectively connected with the sources of the all thin film transistors of the odd and the even rows of the M^{th} column,	
wherein the first data lines and the second data lines of each group of data lines are connected with the same source driver,	See Claim 1 above.
each source driver is installed on the same side of the display panel and	Sharp Reference discloses that the first source driver(AND circuit 72 (labeled "1") in communication with shift register 10, data signal lines 73, 74, sampling switches 19, 20, and sampling capacitors 24, 25) and the second source driver (AND circuit 72 (labelled "2") in communication with shift register 10, sampling switches 21 and 22, and sampling capacitors (not numbered)) are installed on the same side (e.g., upper side) of the display unit 1 (Ex. 1002, Sharp Reference, Pars. [0130]-[0140], FIG. 10).
the data transfer is switched by an electronic switch.	Sharp Reference discloses that the data transfer is switched by each sampling switch 19, 20, 21, 22 (Ex.1002, Sharp Reference, Pars. [0134]-[0135], [0137]-[0139], FIG. 10).
3. The liquid crystal display driving	Sharp Reference discloses that there is a space

The Claims Of The '550 Patent	Sharp Reference
device of matrix structure type as claimed in claim 2, wherein there is a space between the neighboring data lines to prevent them from short circuit.	between the neighboring data lines 5. These spaces prevent the data lines from short circuiting. (Ex. 1002, Sharp Reference, FIG. 10).

115. Accordingly, it is my opinion that Claims 1-3 of the '550 Patent are anticipated by the Sharp Reference.

THE SHARP REFERENCE RENDERS CLAIMS 1-3 AND 5 OBVIOUS TO A PERSON OF ORIDNARY SKILL IN THE ART

116. As discussed above, it is my opinion that the Sharp Reference explicitly discloses each and every element of Claims 1-3 of the '550 Patent, including the claimed source and gate drivers, and thus anticipates Claims 1-3.

117. I believe that no reasonable person of ordinary skill in the art would have interpreted the Sharp Reference as disclosing only a single source driver and a single gate driver in Figure 10.

118. Even under such a tenuous and narrow interpretation of the Sharp Reference, I believe that Claims 1-3 would be obvious to a person of ordinary skill in the art.

THERE IS NO UNEXPECTED RESULT FROM USING MULTIPLE SOURCE AND GATE DRIVERS IN AN LCD PANEL INSTEAD OF A SINGLE SOURCE DRIVER AND A SINGLE GATE DRIVER

119. I understand that one way of demonstrating obviousness in the situation where a prior art reference discloses a single element but the claim requires multiple

elements is to demonstrate that there are no new and unexpected results from increasing the number of such elements.

120. The duplication of the source and gate drivers shown in Figure 10 of the Sharp Reference simply allows more pixels to be added when increasing the size of the LCD panel. The addition of source and gate drivers would not change the way the LCD Panel of the Sharp Reference operates in the Odd Row/Even Row configuration. Accordingly, no unexpected results would be produced from duplicating the source and gate driver circuits (i.e., adding more drivers) shown in Figure 10 of the Sharp Reference.

121. The prior art was abundant with examples of larger sized LCD panels using multiple source and gate drivers. In fact, when I was working in the LCD industry prior to the filing date of the '550 Patent, it was a routine industry practice to change the panel design to increase the size of the panel and/or the number of pixels by simply adding more driver ICs. For example, while the ***small***, low cost LCD panel (which had an equivalent pixel dimension of 7×4) that I worked on at Alien Technology had only a single source driver and a single gate driver, the ***large sized*** LCD panels (which had pixel dimension of at least 800×600) that I worked on at Philips used multiple driver ICs. Using additional source and gate drivers in connection with increasing the size of the panel or the number of pixels in an LCD panel was a well-known and readily available design option.

122. Consistent with my experience and as discussed above, the prior art reference (Ex. 1009) states that "in order to drive many gate bus lines and the source bus

lines on the display circuit board, ***a plurality of the gate drivers and source drivers must*** be connected to the area around the liquid crystal display panel." (*Id.*, Par. [0006]) (emphasis added). Sekido further teaches that increasing the size of the LCD screen will increase the number of the driver ICs. (*Id.*, Par. [0008]).

123. As explained in the Sharp Reference, its use of the Odd Row/Even Row configuration improves the image quality of an LCD panel with the increased number of pixels by reducing the effect of data signal noise. (Ex. 1002, Sharp Reference, Pars. [0144]-[0145], [0030]).

124. Hence, I believe that duplication of source and gate drivers for a larger sized LCD device would have involved only routine skill in the art and does not produce any unexpected result.

125. The '550 Patent fails to demonstrate or even suggest any new and unexpected results stemming from having more than one source driver circuit and more than one gate driver circuit in the claimed LCD driving device. The '550 Patent includes no explanation of the difference between having a single source driver and a single gate driver and having multiple source and gate drivers in the LCD device.

126. In fact, the '550 Patent interchangeably uses the singular ("source driver"/"gate driver") and plural ("source drivers"/"gate drivers") to describe these components. (*See* Ex. 1001, '550 Patent, Col. 8:21 ("[T]here are N gate lines connected to

gate driver . . . ." (emphasis added)); *see also id.*, Figure 1A and Col. 1:36-45 (using the singular terms "data driver 11" and "gate driver 12")).

127. In addition, during prosecution of the '550 Patent, the applicants did not dispute the Examiner's finding that Figure 5 of Kim (Ex. 1006), which shows a ***single*** block for gate driver 16, meets the gate driver**s** limitation of Claims 1 and 2. (Ex. 1005, p. 156).

128. Even if, contrary to my opinion, Patent Owner contends that the Sharp Reference does not disclose the claimed "source drivers" and "gate driver," I believe that it would nevertheless have been obvious to a person of ordinary skill in the art to modify the LCD driving device of the Sharp Reference to include additional source and gate driver circuits in addition to what are shown in Figure 10.

129. It is my opinion that at a minimum, Claims 1-3 of the '550 Patent are obvious over the Sharp Reference.

THE SHARP REFERENCE DISCLOSES INTEGRATED GATE DRIVER CIRCUIT

130. Claim 5 requires that the "gate driver is an integrated gate driver circuit installed on glass." However, this would have also been obvious in view of the Sharp Reference.

131. The Sharp Reference teaches that the gate driver, the source driver, and the display unit consisting of a plurality of pixel units in an LCD device can be formed monolithically on the same substrate in an LCD panel to "to improve the drive force of the pixel transistor that accompanies larger screen size, and to reduce the drive IC mounting

costs and the like." (Ex. 1002, Sharp Reference, Claim 6, Pars. [0160], [0172]-[0173], [0008], [0020], [0036], [0045]). Since the gate drivers are formed monolithically on the same substrate as the pixel TFTs, the result is an integrated gate driver circuit installed on the same substrate as the pixel TFTs.

132. Moreover, It was well-known at the time of the filing date of the '550 Patent that an LCD panel must include a glass substrate or other substantially transparent substrate to transmit the light from the backlight to the LCD viewer's eyes. LCD panels modulate the light generated by the backlight assembly and passed through the glass substrate (or other transparent substrate) according to the TFT drive signals. The light exits the LCD surface nearest the viewer and allows the viewer to see the visual image generated based on the electrical input signal.

133. The use of a glass substrate was the preferred choice, especially in an LCD panel having a large number of pixels. Compared to other transparent materials, glass is cheaper, provides a smoother surface, and is also more resistant to a high temperature required for processing TFTs in an LCD panel. In addition, a glass substrate protects liquid crystal materials and TFTs in the LCD panel from moisture. In my experience, LCD panels with a large number of pixels using TFTs all included glass substrates.

134. Thus, I believe that it would have been obvious to a person of ordinary skill in the art that the integrated gate driver circuit taught by the Sharp Reference is installed on a glass substrate in an LCD panel since the use of glass substrate is one of small number of

widely known design options for an LCD panel having the light transmitted from the backlight. Since this technology was widely understood and available at the time the '550 Patent was filed, I believe that a person of ordinary skill in the art would have been successful in forming an integrated gate driver circuit on a glass substrate.

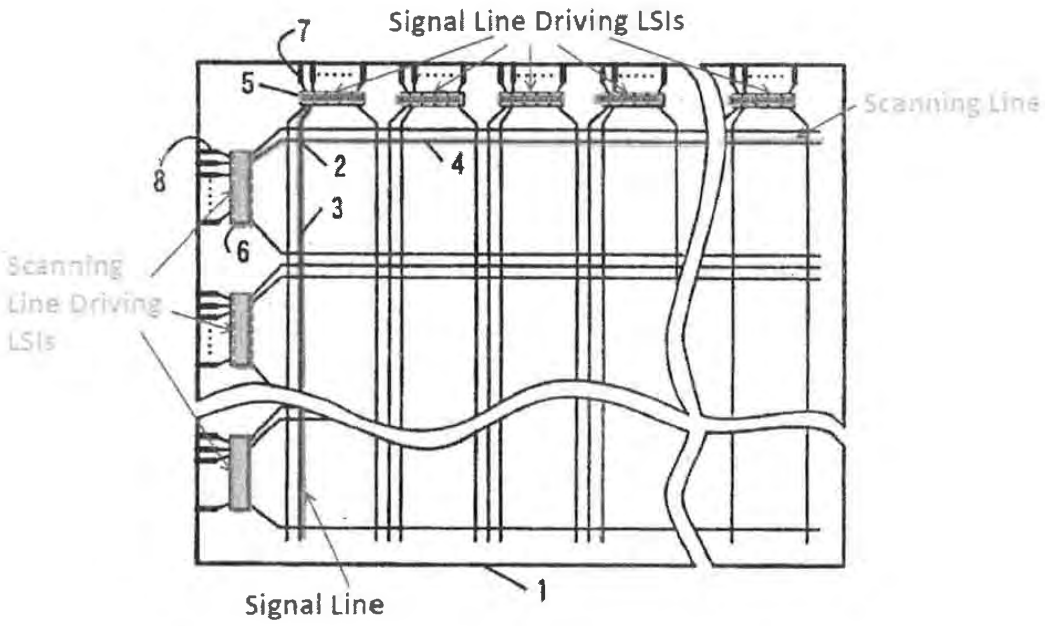
135. Accordingly, it is my opinion that Claim 5 of the '550 Patent is also obvious over the Sharp Reference.

KAMIZONO

136. Kamizono describes an active matrix LCD for a video monitor such as a television receiver or a computer display, and teaches fabricating circuits that are suitable for a large sized LCD panel. (Ex. 1004, Kamizono, Abstract, Col. 1:5-7, Col. 3:1-36).

137. As shown below in annotated Figure 15, Kamizono teaches an LCD panel 1 having data lines ("signal lines 3") connected to multiple source driver ICs ("signal line driving LSIs 5") and gate lines ("scanning lines 4") connected to multiple gate driver ICs ("scanning line driving LSIs 6"). A pixel is located at the intersection 2 between a data line 3 and a gate line 4. The pixels are arranged in the image display region of the LCD panel, while the driving LSIs are arranged in the non-image display region of the panel. (*Id.*, Col. 2:5-13, Cols. 5:51-6:20, FIG. 15). The source driver ICs 5 send data signals to operate TFTs and pixels via data lines 3, while the gate driver ICs 6 send voltage pulse to the gates of TFTs via gate lines 4.

Kamizono Fig. 15



138. Kamizono further teaches that while a "small sized" LCD panel has "a few (2 or 3) of the [driving] LSIs," a "large-screen" LCD panel uses more driving LSIs, such as 4 or 5 scanning line driving LSIs and 10 or more signal line driving LSIs. (*Id.*, Col. 9:19-20, Col. 11:53-64, FIGS. 5, 9, and 15).

139. Kamizono also teaches that for an LCD device having an "increased screen size," these multiple source or gate drivers ("liquid crystal driving LSIs") are commonly mounted as a semiconductor chip by a chip-on-glass (COG) method or a tape automated bonding (TAB) method. According to Kamizono, the COG method is preferred over the TAB

method because of the operational reliability and reduction of the overall product size provided by the COG method, which is consistent with my experience. (*Id.*, Col. 1:12-58).

140. I understand chip-on-glass (COG) to be a method of attaching single-crystal silicon die or Large Scale Integrated (LSI) circuits directly on the glass substrate of the LCD panel. The benefits of using COG are increased reliability, smaller LCD module size, and less weight. The silicon die are designed and fabricated by conventional silicon wafer processes. The die are electrically connected to the panel either through wire bonding or using Anisotropic Conductive Film (ACF). ACF is a type of plastic that contains metalized spheres. The density of the spheres in the film prevents adjacent sphere to sphere connection but connects the die output pads to the panel electrode pads through the thin plastic film.

141. Kamizono further teaches that an LCD panel 1 can be a poly-Silicon TFT panel and the source and gate drivers can be mounted on the panel in the non-image display area of the panel ("a spare area other than a display area of the liquid crystal panel 1"). (*Id.*, Col. 13:50-55). Since the gate drivers are formed on the same substrate as the pixel TFTs, the result is integrated gate driver circuit installed on the same substrate as the pixel TFTs.

CLAIMS 1-5 ARE OBVIOUS OVER THE SHARP REFERENCE IN VIEW OF KAMIZONO

142. I reiterate my opinion discussed above that the Sharp Reference expressly discloses each and every element of Claims 1-3, including the claimed source and gate drivers, and thus anticipates Claims 1-3.

143. Again, to the extent that the Patent Owner argues that the Sharp Reference discloses only a single source driver and a single gate driver in Figure 10, no reasonable person of ordinary skill in the art would agree.

MODIFICATION OF THE LCD DRIVING DEVICE OF THE SHARP REFERENCE TO INCLUDE MULTIPLE SOURCE AND GATE DRIVERS OF KAMIZONO WOULD HAVE BEEN WITHIN THE SKILL OF A PERSON OF ORDINARY SKILL IN THE ART AND WOULD HAVE PRODUCED NO UNEXPECTED RESULT

144. Kamizono teaches the use of multiple source driver ICs 5 and multiple gate driver ICs 6 to send signals through data lines and gate lines in an LCD device. Indeed, Figure 15 of Kamizono is virtually identical to Figure 4A of the '550 Patent.

145. For the reasons discussed below, it is my opinion that even under such a misreading of the Sharp Reference, it would still have been obvious to a person of ordinary skill in the art to combine the teachings of the Sharp Reference and Kamizono to arrive at the LCD driving device of Claims 1-5 of the '550 Patent.

146. The Sharp Reference and Kamizono are in the same field of LCD display technology. They both disclose active matrix LCD devices and are both directed to improving the performance of a large sized LCD panel. The Sharp Reference teaches that source drivers can be implemented in a certain way (e.g., using "driver sample hold

method") to solve the problem of insufficient image data write time arising from increasing the number of pixels in in an LCD panel. (Ex. 1002, Sharp Reference, Pars. [0013]-[0019]). Kamizono teaches that a "large-screen" LCD panel uses more source and gate driver LSIs than a "small sized" LCD panels would use. (Ex. 1004, Kamizono, Col. 9:19-20, Col. 11:53-64, FIGS. 5 and 9). Because both references addressed the same design needs for larger sized LCD panels, I believe that a person of ordinary skill in the art making the source and gate driving circuit for a large-screen LCD panel would have been motivated to combine the teachings of the Sharp Reference and Kamizono.

147. The technique of using multiple gate and source drivers has been used to improve Kamizono's larger sized LCD panels. The source drivers and the Odd Row/Even Row configuration taught in the Sharp Reference also improve the larger sized LCD panels. Hence, a person of ordinary skill in the art would recognize that Kamizono's technique would improve similar devices, such as larger sized LCD panels of the Sharp reference, in the same way. In my opinion, using multiple source and gate driver ICs as taught in Kamizono in the LCD panel of the Sharp Reference is well within the level of ordinary skill in the art, particularly since Figure 10 of the Sharp Reference is configured to have separate circuitry drive data through each gate line and each pair of data lines and Kamizono likewise shows separate circuit (i.e., source drivers 5 and data drivers 6).

148. Based on my experience and knowledge, I believe that modifying the LCD driving device of the Sharp Reference to include the multiple source and gate driver ICs of

Kamizono would not produce unexpected result, but would merely lead to a predictable result, since such a modification simply allows more pixels to be added to increase the size of the LCD panel without changing the way LCD Panel operates.

149. Kamizono teaches the use of multiple source and gate drivers (as does the Sharp Reference), and the Sharp Reference discloses all of the other limitations of Claims 1-3, as shown in the claim charts provided above. Moreover, for the reasons discussed above, there was a clear motivation to combine these references. Thus, to the extent that the Patent Owner argues that the Sharp Reference does not teach multiple source and gate drivers, which is contrary to my opinion discussed above, I believe that, at a minimum, Claims 1-3 of the '550 Patent would be obvious over the Sharp Reference in view of Kamizono.

KAMIZONO DISCLOSES A CHIP ON GLASS

150. Dependent Claim 4 requires that the gate driver is a chip installed on glass.

151. Kamizono teaches that the use of a chip-on-glass is the preferred way of implementing the gate drivers for a large sized LCD panel. (Ex. 1004, Kamizono, Col. 1:12-58).

152. Based on my experience and knowledge, I believe that using the chip on glass of Kamizono for the gate driver in the LCD device of the Sharp Reference would not produce any unexpected result and would not affect, for example, the Odd Row/Even Row configuration in the LCD device of the Sharp Reference.

153. Based on my experience and knowledge, I believe that a person of ordinary skill in the art would recognize that Kamizono's technique of using a chip on glass for the gate driver to improve a large screen LCD panel (e.g., increasing the operational reliability and reducing the overall product size--see Ex. 1004, Kamizono, Col. 1:12-58) can be also used to improve the large screen LCD panel of the Sharp Reference in the same way.

154. A person of ordinary skill in the art making a large-screen LCD panel would have been motivated to combine the teachings of the Sharp Reference and Kamizono to arrive at Claim 4.

THE SHARP REFERENCE DISCLOSES INTEGRATED GATE DRIVER CIRCUIT

155. Claim 5 requires that the gate driver is an integrated gate driver circuit installed on glass. As discussed above, this would have been obvious in view of the Sharp Reference.

156. The Sharp Reference teaches that the gate driver, the source driver, and the display unit consisting of a plurality of pixel units in an LCD device can be formed monolithically on the same substrate in an LCD panel to "to improve the drive force of the pixel transistor that accompanies larger screen size, and to reduce the drive IC mounting costs and the like." (Ex. 1002, Sharp Reference, Claim 6, Pars. [0160], [0172]-[0173], [0008], [0020], [0036], [0045]). Since the gate drivers are formed monolithically on the same substrate as the pixel TFTs, the result is integrated gate driver circuit installed on the same substrate as the pixel TFTs.

157. Moreover, as discussed above, it was well-known at the time of the filing date of the '550 Patent that an LCD panel must include a glass substrate or other substantially transparent substrate to transmit the light from the backlight to the LCD viewer's eyes. LCD panels modulate the light generated by the backlight assembly that passes through the glass substrate (or other transparent substrate) according to the TFT drive signals. The light exits the LCD surface nearest the viewer and allows the viewer to see the visual image generated based on the electrical input signal.

158. Again, the use of a glass substrate was the preferred choice, especially in an LCD panel having a large number of pixels. Compared to other transparent materials, glass is cheaper, provides a smoother surface, and is also more resistant to a high temperature required for processing TFTs in an LCD panel. In addition, a glass substrate protects liquid crystal materials and TFTs in the LCD panel from moisture. In my experience, LCD panels with a large number of pixels using TFTs all included glass substrates.

159. Thus, I believe that it would have been obvious to a person of ordinary skill in the art that the integrated gate driver circuit taught by the Sharp Reference is installed on a glass substrate in an LCD panel since the use of glass substrate is one of small number of widely known design options to make an LCD panel and to have the light transmitted from the backlight.

THE COMBINATION OF THE SHARP REFERENCE AND KAMIZONO TEACHES ALL ELEMENTS OF CLAIMS 1-5

160. The following claim charts summarize where I believe each element of Claims 1-5 is taught by the combination of the Sharp Reference and Kamizono:

The Claims Of The '550 Patent	Sharp Reference in View of Kamizono
1. A liquid crystal display driving device of matrix structure type including:	Sharp Reference discloses a liquid crystal display driving device of matrix structure type (Ex. 1002, Sharp Reference, Pars. [0001]-[0003], [0130], FIG. 10).
a group of thin film transistors with matrix array consisting of N rows and M columns of thin film transistors, wherein each thin film transistor can drive one pixel so that N×M of pixels can be driven;	Sharp Reference discloses a group of thin film transistors 7 with matrix array consisting of n (e.g., 3) rows and m (e.g., 2) columns of thin film transistors 7, wherein each thin film transistor can drive one pixel unit 4 so that n×m (e.g., 3×2) of pixel units can be driven (Ex. 1002, Sharp Reference, Pars. [0049], [0130], [0140]- [0145], FIG. 10).
a group of N gate lines connected to the gate drivers and insulated with each other, wherein the first gate line is connected with the gates of all the thin film transistors of the first row, the second gate line is connected with the gates of all the thin film transistors of the second row . . . and the N^{th} gate line is connected with the gates of all the thin film transistors of the N^{th} row; and	Sharp Reference discloses a group of n (e.g., 3) gate bus lines 6 connected to the gate drivers 3. The gate lines are insulated with each other by being spaced apart from and parallel to each other. The first gate bus line 6 is connected with the gates of all the thin film transistors 7 of the first row. The second gate bus line 6 is connected with the gates of all the thin film transistors 7 of the second row . . . and the n^{th} (e.g., 3^{rd}) gate bus line 6 is connected with the gates of all the thin film transistors 7 of the n^{th} (e.g., 3^{rd}) row (Ex. 1002, Sharp Reference, Pars. [0142]-[0145], FIG. 10). Kamizono discloses scanning lines 4 connected to multiple scanning line driving LSIs 6 in an LCD panel (Ex. 1004, Kamizono, Col. 2:5-13, Cols. 5:51-6:20, FIG. 15).

The Claims Of The '550 Patent	Sharp Reference in View of Kamizono
M groups of data lines connected to the source drivers and insulated with each other, wherein the first and the second date lines of the first group of date lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the first column, the first and the second data lines of the second group of data lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the second column . . . and the first and the second data lines of the M^{th} group of data lines are respectively connected with the sources of the all thin film transistors of the odd and the even rows of the M^{th} column, and	Sharp Reference discloses m (e.g., 2) groups of source bus lines 5 connected to the source drivers 71. The groups of data lines are insulated with each other by being spaced apart from and parallel to each other. The first and the second source bus lines 5 of the first group of source bus lines are respectively connected with the sources of all the thin film transistors 7 of the odd and the even rows of the first column. . . . The first and the second source bus lines 5 of the m^{th} (e.g., 2^{nd}) group of source bus lines are respectively connected with the sources of the all the thin film transistors 7 of the odd and the even rows of the m^{th} (e.g., 2^{nd}) column (Ex. 1002, Sharp Reference, Pars. [0131]-[0140], [0145], FIG. 10). Kamizono discloses signal lines 3 connected to multiple signal line driving LSIs 5 in an LCD panel (Ex. 1004, Kamizono, Col. 2:5-13, Cols. 5:51-6:20, FIG. 15).
the first data lines and the second data lines of each group of data lines are connected with the same source driver.	Sharp Reference discloses that the first source bus lines 5 and the second source bus lines 5 of each group of source bus lines are connected with the same source driver 10, 72, 73, 74, 19, 20, 24, 25 (or 10, 72, 73, 74, 21, 22, 26, 27) (Ex. 1002, Sharp Reference, Pars. [0131]-[0140], FIG. 10).
2. The liquid crystal display device of matrix structure type including:	See Claim 1 above
a group of thin film transistors with matrix array consisting of N rows and M columns of thin film transistors, wherein each thin film transistor can drive one pixel so that N×M of pixels can be driven;	See Claim 1 above
a group of N gate lines connected to	See Claim 1 above

The Claims Of The '550 Patent	Sharp Reference in View of Kamizono
the gate drivers and insulated with each other, wherein the first gate line is connected with the gates of all the thin film transistors of the first row, the second gate line is connected with the gates of all the thin film transistors of the second row . . . and the N^{th} gate line is connected with the gates of all the thin film transistors of the N^{th} row; and	
M groups of data lines connected to the source drivers and insulated with each other, wherein the first and the second date lines of the first group of date lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the first column, the first and the second data lines of the second group of data lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the second column . . . and the first and the second data lines of the M^{th} group of data lines are respectively connected with the sources of the all thin film transistors of the odd and the even rows of the M^{th} column,	See Claim 1 above.
wherein the first data lines and the second data lines of each group of data lines are connected with the same source driver,	See Claim 1 above
each source driver is installed on the same side of the display panel and	Sharp Reference discloses that the first source driver(AND circuit 72 (labeled "1") in communication with shift register 10, data signal lines 73, 74, sampling switches 19, 20, and sampling capacitors 24, 25) and the second

The Claims Of The '550 Patent	Sharp Reference in View of Kamizono
	source driver (AND circuit 72 (labelled "2") in communication with shift register 10, sampling switches 21 and 22, and sampling capacitors (not numbered)) are installed on the same side (e.g., upper side) of the display unit 1 (Ex. 1002, Sharp Reference, Pars. [0130]-[0140], FIG. 10).
the data transfer is switched by an electronic switch.	Sharp Reference discloses that the data transfer is switched by each sampling switch 19, 20, 21, 22 (Ex.1002, Sharp Reference, Pars. [0134]-[0135], [0137]-[0139], FIG. 10).
3. The liquid crystal display driving device of matrix structure type as claimed in claim 2, wherein there is a space between the neighboring data lines to prevent them from short circuit.	Sharp Reference discloses that there is a space between the neighboring data lines 5. These spaces prevent the data lines from short circuiting. (Ex. 1002, Sharp Reference, FIG. 10).
4. The liquid crystal display driving device of matrix structure type as claimed in claim 2, wherein the gate driver is a chip installed on glass.	Kamizono discloses that a liquid crystal driving LSI is commonly mounted as a semiconductor chip by a chip-on-glass (COG) method. (Ex. 1004, Kamizono, Col. 1:12-58).
5. The liquid crystal display driving device of matrix structure type as claimed in claim 2, wherein the gate driver is an integrated gate driver circuit installed on glass.	Kamizono discloses LCD driving circuits that form an integrated structure with a poly-Silicon TFT panel. (Ex. 1004, Kamizono, Col. 13:50-55).

161. Accordingly, it is my opinion that Claims 4-5 of the '550 Patent are also obvious over the Sharp Reference in view of Kamizono.

CLAIMS 1-5 ARE OBVIOUS OVER SHIMADA IN VIEW OF KAMIZONO

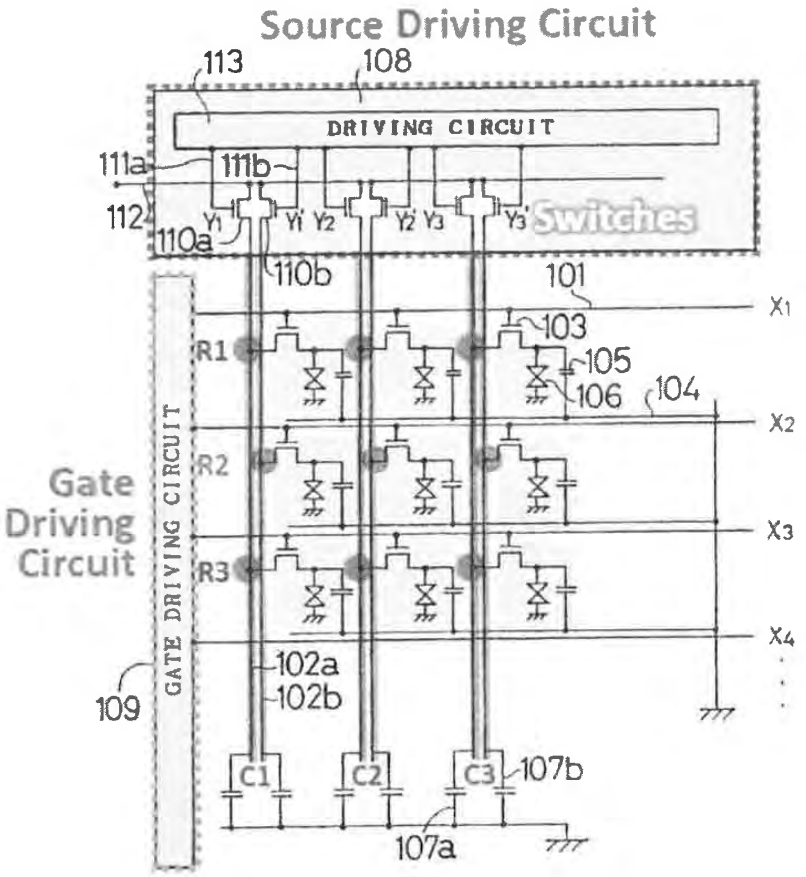
162. As explained below, it is my opinion that Claims 1-5 of the '550 Patent are also obvious over Shimada in view of Kamizono.

SHIMADA

163. As shown below in annotated Figure 4, Shimada teaches an LCD device comprising a matrix array of thin film transistors (TFTs) 103, which drive the corresponding array of pixels 106. (Ex. 1003, Shimada, Col. 4:31-63, Fig. 4).

164. Like the Sharp Reference and Kamizono, Shimada addresses the technical problems arising from increasing the size of the LCD panel and the number of pixels, such as line delay. (*Id.* at Cols. 2:35-3:63). Shimada states that its object is to "reduce the effect of signal delay on display quality" of the LCD device, thereby improving image quality. (*Id.* at Col. 2:66-67).

Shimada Fig. 4



165. As shown in Figure 4, a group of gate bus lines 101 (X_1, X_2, X_3, . . .) is connected to the gate driving circuit 109, and each gate bus line is connected with the gates of all of the TFTs 103 in the row associated with that gate bus line. For example, the first gate line X_1 is connected with the gates of all of the TFTs 103 of the first row (R1), the

second gate line X_2 is connected with the gates of all of the TFTs 103 of the second row (R2), etc. (*Id.* at Col. 4:31-40, Fig. 4).

166. Shimada also teaches that the gate bus lines 101 (X_1, X_2, X_3, . . .) are spaced apart from and parallel to each other (i.e., insulated with each other). (*Id.*, Fig. 4).

167. Figure 4 also shows groups of data bus lines 102a, 102b (the red and green lines) connected to the ***same*** source driving circuit 108. I understand that this was the basis for allowance of Claim 1 by the Patent Office. Figure 4 also shows that the data bus lines (e.g., 102a, 102b) are spaced apart from and parallel to each other (i.e., insulated with each other). (*Id.*, Col. 4:31-40, Fig. 4).

168. As shown above in Figure 4 of Shimada, the first data bus line 102a (red line) and the second data bus line 102b (green line) in each group of data bus lines are respectively connected with the sources of all of the TFTs 103 of the **odd rows** (red boxes in R1 and R3) and **even rows** (green boxes in R2) of the column (C1, C2, C3) associated with that group of data bus lines, as required Claims 1-5 of the '550 Patent.

169. For example, the first data bus line 102a (red line) of the first group is connected with the sources (red dots) of the TFTs 103 of the first row and third row (see the red boxes in R1 and R3) in the first column (C1), while the second data bus line 102b (green line) of the first group is connected with the sources (green dot) of the TFT 103 of the second row (green box in R2) in the first column (C1). (*Id.* at Col. 4:41-63, Fig. 4). The same Odd Row/Even Row configuration is provided in each column (e.g., C2 and C3).

170. Shimada teaches that this Odd Row/Even Row configuration reduces the effect of signal delay caused by the increased number of pixels, thereby improving the video quality of the display of a larger-sized LCD panel. (*Id.* at Cols. 2:34-3:2, Col. 5:49-66).

171. As shown in Figure 4, the source driving circuit 108 for all data bus lines is installed on the same side (e.g., upper side) of the display panel.

172. Figure 4 also shows that the transfer of video signals from the video signal line 112 to the first and the second data bus lines 102a, 102b is switched by the switches 110a, 110b. (*Id.* at Col. 4:41-51, Fig. 4).

IT WOULD HAVE BEEN OBVIOUS TO COMBINE SHIMADA'S LCD DEVICE WITH KAMIZONO'S TEACHING OF MULTIPLE SOURCE AND GATE DRIVERS

173. The LCD device of Shimada discloses all of the key elements of Claims 1-3 of the '550 Patent, including the Odd Row/Even Row configuration.

174. Kamizono discloses source drivers 5 and gate drivers 6. (Ex. 1004, Kamizono, Col. 2:5-13, Cols. 5:51-6:20, FIG. 15).

175. As discussed below, I believe that it would have been obvious to a person of ordinary skill in the art at the time the '550 Patent was filed to combine the teachings of Shimada and Kamizono to arrive at the LCD driving device of Claims 1-3.

176. Shimada and Kamizono are in the same field of LCD display technology. They both disclose active matrix LCD devices and are both directed to improving the performance of a large screen LCD panel. Shimada states that increasing the number of pixels causes undesirable line delay and teaches the Odd Row/Even Row configuration in a

larger sized LCD device to reduce the effect of signal delay on display quality of the LCD device. (Ex. 1003, Shimada, Cols. 2:35-3:63). Kamizono teaches that a "large-screen" LCD panel uses more source and gate driver LSIs than a "small sized" LCD panels would use. (Ex. 1004, Kamizono, Col. 9:19-20, Col. 11:53-64, FIGS. 5 and 9). Because both references addressed the same design need for larger sized LCD panels, I believe that a person of ordinary skill in the art making the source and gate driving circuit for a large-screen LCD panel would have been motivated to combine the teachings of Shimada and Kamizono to arrive at Claims 1-3.

177. Based on my experience and knowledge, I believe that modifying the LCD driving device of Shimada to include the multiple source and gate driver ICs of Kamizono would not produce unexpected results, since such a modification simply allows more pixels to be added to increase the size of the LCD panel. This modification would not change the way Shimada's LCD panel operates in the Odd Row/Even Row configuration.

178. In addition, I believe that a person of ordinary skill in the art would recognize that Kamizono's technique of including multiple source and gate drivers to improve a large screen LCD panel can also be used to improve the large screen LCD panel of Shimada in the same way. This would be well within the level of ordinary skill in the art.

179. Indeed, the prior art was replete with examples of larger sized LCD panels using multiple source and gate drivers. In fact, when I was working in the LCD industry prior to the filing date of the '550 Patent, it was a routine industry practice to change the panel

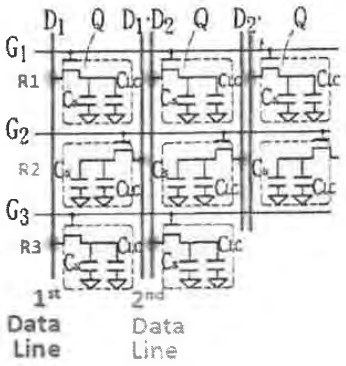
design to increase the size of the panel and/or the number of pixels by simply adding more driver ICs. For example, while the ***small***, low cost LCD panel (which had an equivalent pixel dimension of 7×4) that I worked on at Alien Technology had only a single source driver and a single gate driver, the ***large sized*** LCD panels (which had pixel dimension of at least 800×600) that I worked on at Philips used multiple driver ICs. Using additional source and gate drivers in connection with increasing the size of the panel or the number of pixels in an LCD panel was a well-known and readily available design option.

180. Consistent with my experience, the prior Sekido reference (Ex. 1009) states that "in order to drive many gate bus lines and the source bus lines on the display circuit board, ***a plurality of the gate drivers and source drivers must*** be connected to the area around the liquid crystal display panel." (Ex. 1009, Sekido, Par. [0006]) (emphasis added). This prior art further teaches that increasing the size of the LCD screen will increase the number of the driver ICs. (*Id.*, Par. [0008]).

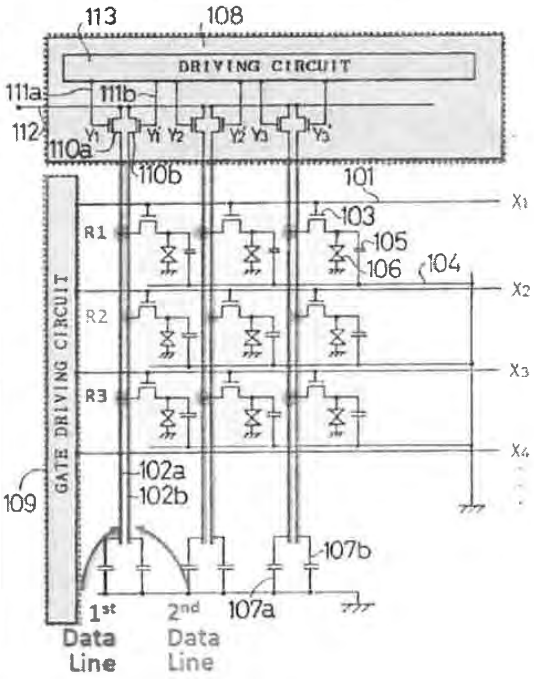
181. Accordingly, I believe that it would have been obvious to a person of ordinary skill in the art to modify the LCD driving device of Shimada to include the multiple source and gate drivers shown in Kamizono and connect them to the data lines (e.g., 102a, 102b) and the gate lines (X_1, X_2, X_3, X_4) of Shimada, respectively.

182. Moreover, as discussed below, Shimada teaches all of the other limitations of Claims 1 and 2 of the '550 Patent.

'550 Patent Fig. 4B



Shimada Fig. 4



SHIMADA DISCLOSES THE ODD ROW/EVEN ROW CONFIGURATION

183. As shown above in annotated Figure 4, Shimada discloses the claimed Odd Row/Even Row configuration of the '550 Patent (shown on the left). (Ex. 1003, Shimada, Col. 4:41-63, Fig. 4).

184. Specifically, the first data line 102a (see the red line) is connected to the sources (red dots) of the TFTs (red boxes) in the odd rows (R1 and R3). The second data line 102b (green line) is connected to the sources (green dot) of the TFTs (green boxes) in the even rows (R2). Figure 4B of the later '550 Patent has the same Odd Row/Even Row configuration.

185. Like the '550 Patent, Shimada teaches that this Odd Row/Even Row configuration reduces the effect of signal delay on the quality of the display, thereby improving image quality. (*Id.* at Cols. 2:66-3:2).

SHIMADA DISCLOSES THAT FIRST AND SECOND DATA LINES IN EACH GROUP OF DATA LINES ARE CONNECTED WITH THE SAME SOURCE DRIVER

186. As shown above in Figure 4 of Shimada, the first and second data lines (e.g., 102a (red line) and 102b (green line)) in each group of data lines in are connected with the ***same*** source driver 108 (*Id.* at Col. 4:41-51, Fig. 4), as required by Claims 1 and 2. I understand that this was the basis for allowance of Claim 1 during prosecution.

SHIMADA DISCLOSES THAT EACH SOURCE DRIVER IS INSTALLED ON THE SAME SIDE OF THE DISPLAY PANEL

187. As shown above in Figure 4 of Shimada, each source driver 108 is installed on the same side of the display panel (*id.* at Col. 4:41-46, Fig. 4), as required by independent Claim 2.

SHIMADA DISCLOSES AN ELECTRONIC SWITCH FOR DATA TRANSFER

188. As shown above in Figure 4 of Shimada, data transfer is switched by an electronic switch 110a, 110b (*id.*), as required by independent Claim 2.

SHIMADA DISCLOSES THAT GATE LINES/DATA LINES ARE INSULATED WITH EACH OTHER

189. In addition, Shimada teaches that the gate lines 101 (X_1, X_2, X_3, . . .) are "insulated with each other" under the broadest reasonable construction since they are shown to be spaced apart from and parallel to each other. Likewise, Shimada teaches that

the data bus lines (e.g., 102a, 102b) are insulated with each other as they are spaced apart from and parallel to each other. (*Id.* at FIG. 4).

190. Because Shimada and Kamizono combine to disclose all of the elements of Claims 1 and 2, and further because there was a clear motivation for a person of ordinary skill in the art to combine these references, I believe that Claims 1 and 2 are obvious over Shimada in view of Kamizono.

SHIMADA DISCLOSES A SPACE BETWEEN THE NEIGHBORING DATA LINE TO PREVENT SHORT CIRCUITING

191. Claim 3, which depends from Claim 2, recites that "there is a space [i.e., a gap] between the neighboring data lines to prevent them from short circuit." Figure 4 of Shimada clearly shows that there is a space between the neighboring data lines (e.g., between 102a and 102b) that prevents short circuiting.

192. When two neighboring data lines are shown to be spaced apart from each other in the schematic circuit diagram for an LCD driving device, such as Figure 4 of Shimada, I expect that there is a sufficient space between these data lines to prevent short circuiting. Otherwise, the LCD driving device would not be operating as described in the reference.

KAMIZONO DISCLOSES A CHIP ON GLASS

193. Dependent Claim 4 requires that the gate driver is a chip installed on glass.

194. Kamizono teaches that the use of a chip-on-glass is the preferred way of implementing the gate drivers for a large sized LCD panel. (Ex. 1004, Kamizono, Col. 1:12-58).

195. Shimada and Kamizono are in the same field of LCD display technology. They both disclose active matrix LCD devices and are both directed to improving the performance of a large screen LCD panel. Shimada states that increasing the number of pixels causes undesirable line delay and teaches the Odd Row/Even Row configuration in a ***larger sized*** LCD device to reduce the effect of signal delay on display quality of the LCD device. (Ex. 1003, Shimada, Cols. 2:35-3:63). Kamizono teaches that a "large-screen" LCD panel uses more source and gate driver LSIs than a "small sized" LCD panels would use. (Ex. 1004, Kamizono, Col. 9:19-20, Col. 11:53-64, FIGS. 5 and 9). Because both references addressed the same design need for larger sized LCD panels, I believe that a person of ordinary skill in the art making the gate drivers for a large-screen LCD panel would have been motivated to combine the teachings of Shimada and Kamizono to arrive at Claim 4.

196. Based on my experience and knowledge, I believe that using the chip on glass of Kamizono for the gate driver in the LCD device of Shimada would not produce any unexpected result and would not affect, for example, the Odd Row/Even Row configuration in Shimada's LCD device.

197. Based on my experience and knowledge, I believe that a person of ordinary skill in the art would recognize that Kamizono's technique of using a chip on glass for the gate driver to improve a large screen LCD panel (e.g., increasing the operational reliability and reducing the overall product size) can be also used to improve the large screen LCD panel of Shimada in the same way.

198. Accordingly, a person of ordinary skill in the art making a large-screen LCD panel would have been motivated to combine the teachings of Shimada and Kamizono to arrive at Claim 4.

199. Accordingly, it is my opinion that Claim 4 is also obvious over Shimada in view of Kamizono.

KAMIZONO DISCLOSES INTEGRATED GATE DRIVER CIRCUIT

200. Claim 5 requires that the gate driver is an integrated gate driver circuit installed on glass.

201. Kaminozo teaches that an LCD panel can be a poly-Silicon TFT panel and the source and gate drivers can be mounted on the panel in a spare area other than the display area of the panel (i.e., forming an integrated structure with the LCD panel). (Ex. 1004, Kamizono, Col. 13:50-55). Since the gate drivers are formed on the same substrate as the pixel TFTs, the result is integrated gate driver circuit installed on the same substrate as the pixel TFTs.

202. Moreover, as discussed above, it was well-known at the time of the filing date of the '550 Patent that an LCD panel must include a glass substrate or other substantially transparent substrate to transmit the light from the backlight to the LCD viewer's eyes. LCD panels modulate the light generated by the backlight assembly and passed through the glass substrate (or other transparent substrate) according to the TFT drive signals. The light exits the LCD surface nearest the viewer and allows the viewer to see the visual image generated based on the electrical input signal.

203. The use of a glass substrate was the preferred choice, especially in an LCD panel having a large number of pixels. Compared to other transparent materials, glass is cheaper, provides a smoother surface, and is also more resistant to a high temperature required for processing TFTs in an LCD panel. In addition, a glass substrate protects liquid crystal materials and TFTs in the LCD panel from moisture. In my experience, LCD panels with a large number of pixels using TFTs all included glass substrates.

204. Thus, I believe that it would have been obvious to a person of ordinary skill in the art that the integrated gate driver circuit taught by Kamizono is installed on a glass substrate in an LCD panel since the use of glass substrate is one of small number of widely known design options to make an LCD panel and to have the light transmitted from the backlight.

205. As discussed above, because Shimada and Kamizono addressed the same design need for larger sized LCD panels, I believe that a person of ordinary skill in the art

making the gate drivers for a large-screen LCD panel would have been motivated to combine the teachings of Shimada and Kamizono to arrive at Claim 5.

206. Based on my experience and knowledge, I believe that using the integrated gate driver circuit on glass of Kamizono for the gate driver in the LCD device of Shimada would not produce any unexpected result and would not affect, for example, the Odd Row/Even Row configuration in Shimada's LCD device.

207. Accordingly, it is my opinion that Claim 5 of the '550 Patent is also obvious over Shimada in view of Kamizono.

THE COMBINATION OF SHIMADA AND KAMIZONO TEACHES ALL ELEMENTS OF CLAIMS 1-5

208. The following claim charts summarize where I believe each element of Claims 1-5 is taught by the combination of Shimada and Kamizono:

The Claims Of The '550 Patent	Shimada in View of Kamizono
1. A liquid crystal display driving device of matrix structure type including:	Shimada discloses a liquid crystal display driving device of matrix structure type (Ex. 1003, Shimada, Col. 1:8-10, Col. 4:31-67, Figs. 4, 7).
a group of thin film transistors with matrix array consisting of N rows and M columns of thin film transistors, wherein each thin film transistor can drive one pixel so that N×M of pixels can be driven;	Shimada discloses a group of thin film transistors 103 with matrix array consisting of N (e.g., 3) rows and M (e.g., 3) columns of thin film transistors 103, wherein each thin film transistor can drive one pixel 106 so that N×M of pixels can be driven (Ex. 1003, Shimada, Col. 4:31-63, Fig. 4).
a group of N gate lines connected to the gate drivers and insulated with each other, wherein the first gate line is connected with the gates of all the	Shimada discloses a group of N gate lines 101 (e.g., X_1, X_2, X_3, . . .) connected to the gate driver (e.g., gate driving circuit 109) and insulated with each other by being spaced apart

The Claims Of The '550 Patent	Shimada in View of Kamizono
thin film transistors of the first row, the second gate line is connected with the gates of all the thin film transistors of the second row . . . and the N^{th} gate line is connected with the gates of all the thin film transistors of the N^{th} row; and	from and parallel to each other. The first gate line X_1 is connected with the gates of all the thin film transistors 103 of the first row. The second gate line X_2 is connected with the gates of all the thin film transistors 103 of the second row . . . and the N^{th} gate line X_N is connected with the gates of all the thin film transistors 103 of the N^{th} row. (Ex. 1003, Shimada, Col. 4:31-40, Figs. 4, 7). Kamizono discloses scanning lines 4 connected to multiple scanning line driving LSIs 6 in an LCD panel (Ex. 1004, Kamizono, Col. 2:5-13, Cols. 5:51-6:20, FIG. 15).
M groups of data lines connected to the source drivers and insulated with each other, wherein the first and the second date lines of the first group of date lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the first column, the first and the second data lines of the second group of data lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the second column . . . and the first and the second data lines of the M^{th} group of data lines are respectively connected with the sources of the all thin film transistors of the odd and the even rows of the M^{th} column, and	Shimada discloses M (e.g., 3) groups of data lines 102a, 102b connected to the source driver (e.g., the source driving circuit 108) and insulated with each other by being spaced apart from and parallel to each other. The first and the second data lines 102a, 102b of the first group of data lines are respectively connected with the sources of all the thin film transistors 103 of the odd and the even rows of the first column. The first and the second data lines 102a, 102b of the second group of data lines are respectively connected with the sources of all the thin film transistors 103 of the odd and the even rows of the second column . . . and the first and the second data lines 102a, 102b of the M^{th} group of data lines are respectively connected with the sources of the all thin film transistors 103 of the odd and the even rows of the M^{th} column (Ex. 1003, Shimada, Col. 4:41-63, Fig. 4). Kamizono discloses signal lines 3 connected to multiple signal line driving LSIs 5 in an LCD panel (Ex. 1004, Kamizono, Col. 2:5-13, Cols. 5:51-6:20, FIG. 15).

The Claims Of The '550 Patent	Shimada in View of Kamizono
the first data lines and the second data lines of each group of data lines are connected with the same source driver.	Shimada discloses that the first data lines 102a and the second data lines 102b of each group of data lines are connected with the same source driver 108 (Ex. 1003, Shimada, Col. 4:41-63, Fig. 4; *compare with* Ex. 1001, '550 Patent, Fig. 6A).
2. The liquid crystal display device of matrix structure type including:	Shimada discloses a liquid crystal display driving device of matrix structure type (Ex. 1003, Shimada, Col. 1:8-10, Cols. 4:31-5:15, Figs. 4, 7).
a group of thin film transistors with matrix array consisting of N rows and M columns of thin film transistors, wherein each thin film transistor can drive one pixel so that N×M of pixels can be driven;	Shimada discloses a group of thin film transistors 103 with matrix array consisting of N (e.g., 3) rows and M (e.g., 3) columns of thin film transistors 103, wherein each thin film transistor can drive one pixel 106 so that N×M of pixels can be driven (Ex. 1003, Shimada, Col. 4:31-63, Fig. 4).
a group of N gate lines connected to the gate drivers and insulated with each other, wherein the first gate line is connected with the gates of all the thin film transistors of the first row, the second gate line is connected with the gates of all the thin film transistors of the second row . . . and the N^{th} gate line is connected with the gates of all the thin film transistors of the N^{th} row; and	Shimada discloses a group of N gate lines 101 (e.g., X_1, X_2, X_3, . . .) connected to the gate driver (e.g., gate driving circuit 109) and insulated with each other by being spaced apart from and parallel to each other. The first gate line X_1 is connected with the gates of all the thin film transistors 103 of the first row. The second gate line X_2 is connected with the gates of all the thin film transistors 103 of the second row . . . and the N^{th} gate line X_N is connected with the gates of all the thin film transistors 103 of the N^{th} row (Ex. 1003, Shimada, Col. 4:31-40, Figs. 4, 7). Kamizono discloses scanning lines 4 connected to multiple scanning line driving LSIs 6 in an LCD panel (Ex. 1004, Kamizono, Col. 2:5-13, Cols. 5:51-6:20, FIG. 15).
M groups of data lines connected to the source drivers and insulated with	Shimada discloses M (e.g., 3) groups of data lines 102a, 102b connected to the source driver

The Claims Of The '550 Patent	Shimada in View of Kamizono
each other, wherein the first and the second date lines of the first group of date lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the first column, the first and the second data lines of the second group of data lines are respectively connected with the sources of all the thin film transistors of the odd and the even rows of the second column . . . and the first and the second data lines of the M^{th} group of data lines are respectively connected with the sources of the all thin film transistors of the odd and the even rows of the M^{th} column,	(e.g., the source driving circuit 108) and insulated with each other by being spaced apart from and parallel to each other. The first and the second data lines 102a, 102b of the first group of data lines are respectively connected with the sources of all the thin film transistors 103 of the odd and the even rows of the first column. The first and the second data lines 102a, 102b of the second group of data lines are respectively connected with the sources of all the thin film transistors 103 of the odd and the even rows of the second column . . . and the first and the second data lines 102a, 102b of the M^{th} group of data lines are respectively connected with the sources of the all thin film transistors 103 of the odd and the even rows of the M^{th} column (Ex. 1003, Shimada, Col. 4:41-63, Fig. 4). Kamizono discloses signal lines 3 connected to multiple signal line driving LSIs 5 in an LCD panel (Ex. 1004, Kamizono, Col. 2:5-13, Cols. 5:51-6:20, FIG. 15).
Wherein the first data lines and the second data lines of each group of data lines are connected with the same source driver,	Shimada discloses that the first data lines 102a and the second data lines 102b of each group of data lines are connected with the same source driver 108 (Ex. 1003, Shimada, Col. 4:41-63, Fig. 4; *compare with* Ex. 1001, '550 Patent, Fig. 6A).
each source driver is installed on the same side of the display panel and	Shimada discloses that each source driver 108 is installed on the same side (e.g., upper side) of the display panel (Ex. 1003, Shimada, Col. 4:41-46, Fig. 4).
The data transfer is switched by an electronic switch.	Shimada discloses that the data transfer is switched by an electronic switch 110a, 110b (Ex. 1003, Shimada, Col. 4:41-46, Fig. 4).

The Claims Of The '550 Patent	Shimada in View of Kamizono
3. The liquid crystal display driving device of matrix structure type as claimed in claim 2, wherein there is a space between the neighboring data lines to prevent them from short circuit.	Shimada discloses that there is a space between the neighboring data lines 102a, 102b (Ex. 1003, Shimada, Figs. 4, 7).
4. The liquid crystal display driving device of matrix structure type as claimed in claim 2, wherein the gate driver is a chip installed on glass.	Kamizono discloses that a liquid crystal driving LSI is commonly mounted as a semiconductor chip by a chip-on-glass (COG) method. (Ex. 1004, Kamizono, Col. 1:12-58).
5. The liquid crystal display driving device of matrix structure type as claimed in claim 2, wherein the gate driver is an integrated gate driver circuit installed on glass.	Kamizono discloses LCD driving circuits that form an integrated structure with a poly-Silicon TFT panel. (Ex. 1004, Kamizono, Col. 13:50-55).

209. Accordingly, it is my opinion that Claims 1-5 of the '550 Patent are also obvious over Shimada in view of Kamizono.

210. At this time I am not aware of any arguments and evidence of "secondary considerations" that would render the claims of the '550 Patent non-obvious with respect to my opinions set forth herein on the issue of obviousness. Should Patent Owner present such evidence, I reserve the right to respond to such evidence and arguments.

I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true. I further declare that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of the Title 18 of the United States Code.

Dated: March 20, 2015

By: Michael J. Marentic

Michael J. Marentic

600321.1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re	:	U.S. Patent No. 7,202,843
Filed	:	January 8, 2004
Issued	:	April 10, 2007
Inventor(s)	:	Yung-Hung Shen et al.
Assignee	:	Surpass Tech Innovation LLC
Title	:	DRIVING CIRCUIT OF A LIQUID CRYSTAL DISPLAY PANEL AND RELATED DRIVING METHOD
Trial No.	:	To Be Assigned
Panel:	:	To Be Assigned

Attorney Docket No.: 77331-4

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Patent Trial and Appeal Board
United States Patent and Trademark Office
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Alexandria, VA 22313-1450

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 7,202,843

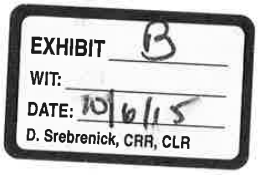

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TABLE OF AUTHORITIES

EXHIBIT LIST

EXHIBIT NO.	DESCRIPTION
1001	U.S. Patent No. 7,202,843 to Shen et al. ("'843 Patent")
1002	U.S. Patent Application Publication No. 2002/0044115 ("Jinda")
1003	Japanese Laid Open Application Publication JPH0662355A ("Miyai") and Certified English Translation Thereof
1004	U.S. Patent Application Publication No. 2001/0038369 ("Adachi")
1005	U.S. Patent Application Publication No. 2004/0196229 ("Ham")
1006	Prosecution History of U.S. Appl. No. 10/707,741
1007	Select Documents from the Prosecution History of European Patent Application No. 03029643.8
1008	Select Documents from the Prosecution History of Japanese Laid-Open Patent Publication No. 4199655 and Certified English Translation Thereof

I. INTRODUCTION

Pursuant to 35 U.S.C. §§ 311-319 and 37 C.F.R. § 42, Sharp Corporation ("Petitioner" or "Sharp") respectfully petitions for *Inter Partes* Review ("IPR") of Claims 1, 4, 8 and 9 of U.S. Patent No. 7,202,843 ("the '843 Patent," Ex. 1001), which is assigned to Surpass Tech Innovation LLC ("Patent Owner" or "Surpass"). As demonstrated below, there is a reasonable likelihood that Petitioner will prevail in establishing that at least one of the Claims challenged in this Petition is unpatentable based on the prior art discussed below. Accordingly, institution of an IPR and initiation of trial is respectfully requested.

Liquid crystal display ("LCD") panels were well known in the prior art long before the '843 Patent was filed. A typical LCD display contains a matrix of pixels, each of which contains a liquid crystal device (or pixel electrode). An LCD panel produces images by manipulating the light transmission rate (or transmittance) of the liquid crystal in each pixel.

One well known problem with LCD displays is blurring of moving images. Blurring occurs when the liquid crystal is unable to change its light transmission rate fast enough between sequential video frames. To illustrate, video signals commonly have a frame rate of 60 frames/second (i.e., 60 discrete images are displayed every second). As such, to display all sixty images within one second, a pixel would ideally be able to reach a desired transmission rate within one 60th of a second. In other words, the "response time" of the pixel should be equal to, or less than, the frame period of the video signal. If a pixel is unable to obtain a desired transmission rate within a specified time (i.e., the response time

is too slow), the image may appear blurry to the viewer. This defect is particularly pronounced in video signals containing a high degree of motion (e.g., sporting events).

The '843 Patent discloses and claims driving circuits and methods that purportedly improve the response time of an LCD panel, which in turn results in reduced blurring and improved picture quality. Specifically, the '843 Patent discusses and claims two techniques for improving the response time and resultant image quality of LCD displays: (1) "overdriving" the signal data; and (2) increasing the frequency of the signal data (e.g., doubling the frequency of the signal from 60 frames/second to 120 frames/second).

"Overdriving" involves applying a higher or a lower data impulse (i.e., voltage) to the pixel electrode. This voltage boost forces the liquid crystal material to react more quickly, thereby improving the image quality and reducing blurring. The '843 Patent admits that this overdriving technique is the "***[s]ame as the prior art.***" (Ex. 1001, '843 Patent, Col. 4:17-19 (emphasis added)).

The '843 Patent alleges that, while capable of improving response time and reducing blurring to some extent, overdriving alone does not adequately address blurring. According to the '843 Patent, in the prior art, only a ***single overdriven impulse*** was used in a single frame period, and as a result, the desired transmission rate would not be reached within a single frame. (*See id.* at Col. 2:7-12). As can be seen below, the overdriven signal (C2) of the "prior art" is purportedly unable to reach the desired transmission rate (T2) in a single frame period (N) because the response time is too slow.

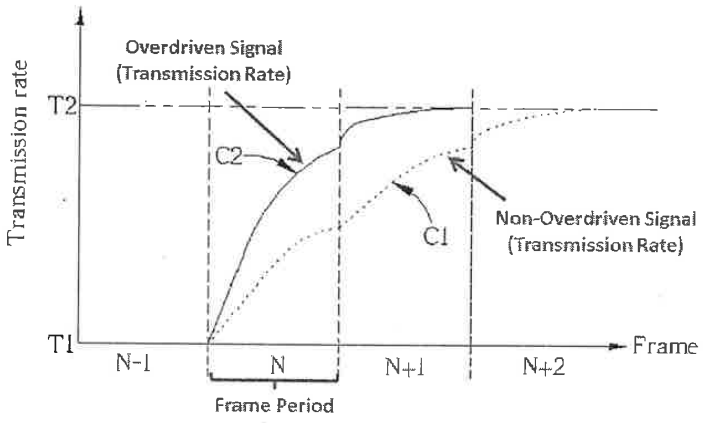
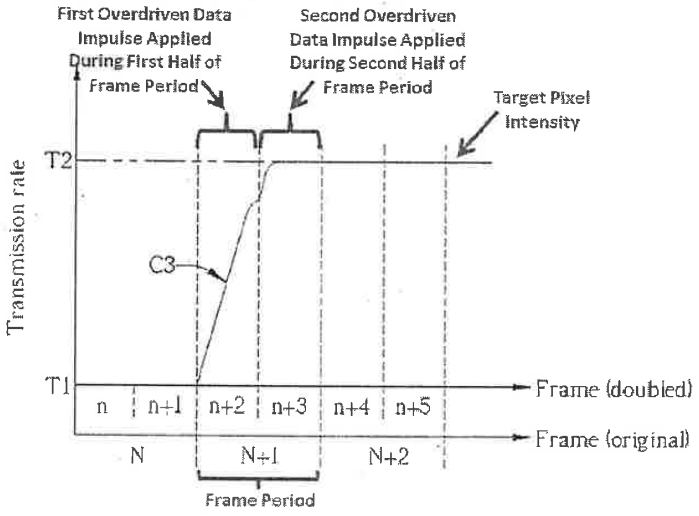


Fig. 2 Prior art

To achieve the desired transmission rate within a single frame, the '843 Patent suggests applying ***two or more overdriven impulses*** to each pixel within a single frame period, as shown below. (*Id.* at Col. 4:20-40). This technique is commonly referred to as increasing the "refresh rate" of the display (e.g., from 60 Hz to 120 Hz). In the embodiment shown in Figure 6 of the '843 Patent (annotated and reproduced below), the "original" frame rate is "doubled" (see n+2 and n+3), such that two overdriven data impulses are applied in each single frame period (see N+1).



Claim 1 requires the use of (1) overdriven pixel data and (2) the generation of a plurality of data impulses within a single frame, whereas Claims 4, 8, and 9 only require the latter. Both of these concepts were known in the prior art. For example, as shown below, U.S. Patent Application Publication Nos. 2002/0044115 to Jinda and 2001/0038369 to Adachi (both assigned to Sharp) disclose these concepts:.

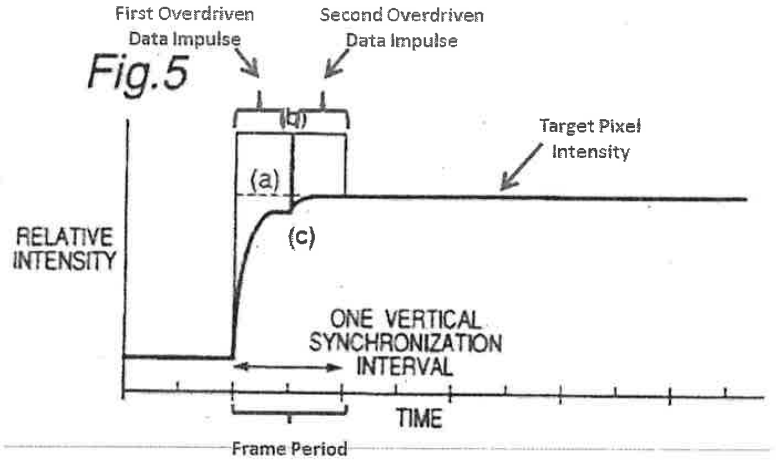


Figure 5 of Jinda

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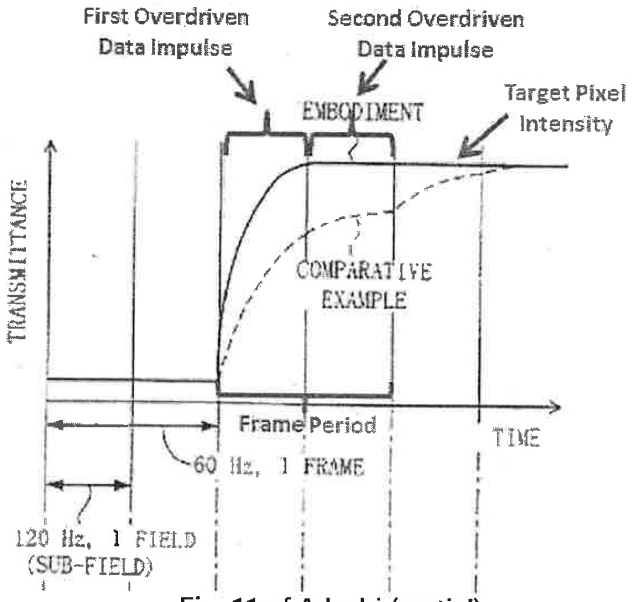
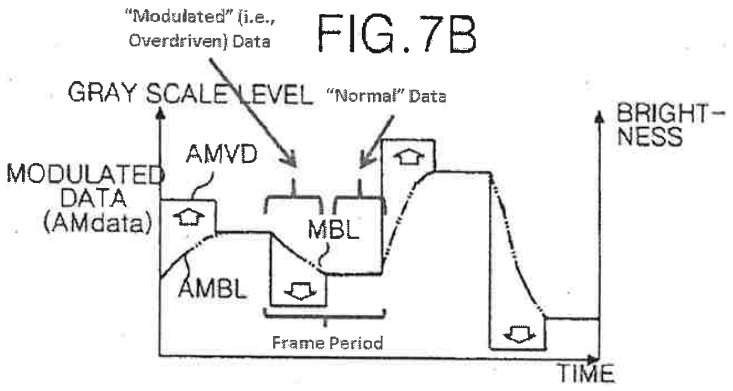


Fig. 11 of Adachi (partial)

Both Jinda and Adachi identify the *same problem* as the '843 Patent—the need to improve the response time of liquid crystal displays to eliminate blurring—and disclose the exact same solution. As shown above, Jinda teaches applying two or more overdriven impulses to each pixel a "***plurality of times*** within ***one*** vertical synchronization ***interval***" (i.e., a single frame period). (*See, e.g.,* Ex. 1002, Jinda, ¶ [0010]; *see also* ¶¶ [0007], [0041]-[0042]) (emphasis added). Similarly, as also shown above, Adachi teaches that the input signal should be subject to "overshoot driving" (i.e., overdriving) and "written at a ***double speed*** to the liquid crystal panel" (i.e., at 120 Hz) to reach the desired transmittance within a single frame period. (Ex. 1004, Adachi, ¶ [0157]) (emphasis added). Not surprisingly, the above figures from Jinda and Adachi are strikingly similar to Figure 6 of the '843 Patent.

In addition, the methods of increasing the refresh rate of an LCD display recited in Claims 4, 8 and 9 (e.g., doubling the frame rate) are also taught by Ham. Ham teaches applying overdriven pixel data in only the first half of the frame period, and applying non-overdriven data in the second half of the frame period. (Ex. 1005, Ham, ¶ [0053]). This is shown, for example, in Figure 7B of Ham (annotated and reproduced below):



The remaining elements recited in Claims 1, 4, 8 and 9 (e.g., scan lines, data lines, switching devices) are merely known components essential to the operation of any LCD display. Adachi and Ham explicitly discloses each of these elements. Although Jinda does not show some of these known elements in the drawings, they are disclosed by Miyai, which is incorporated by reference into Jinda. As such, there is a reasonable likelihood that Petitioner will prevail in establishing that: (1) Claims 1, 4, 8, and 9 are anticipated by each of Jinda and Adachi under 35 U.S.C. § 102(b); and Claims 4, 8, and 9 are anticipated by Ham under 35 U.S.C. § 102(e).

Moreover, given that Jinda ***expressly*** teaches one of ordinary skill the art to combine the disclosed driving circuit with the LCD panel of Miyai, there is a reasonable likelihood that Petitioner will prevail in establishing that Claims 1, 4, 8 and 9 are also obvious over Jinda in view of Miyai.

Finally, although the '843 Patent issued without any substantive prosecution by the U.S. Patent Office, Surpass' predecessor ("Applicant") was unsuccessful in obtaining similar claims in Europe and Japan. The European Patent Office ("EPO") rejected virtually identical claims in view of the Jinda reference discussed above. In response, the Applicant abandoned the application. And, the Japanese Patent Office ("JPO") rejected similar claims to those at issue in this Petition in view of a foreign counterpart to the Adachi reference discussed above, finding that Adachi disclosed each claim element. The Applicant did not (and could not) challenge any of these findings. Although Jinda and Adachi were cited references in the '843 Patent, the USPTO was never made aware that the EPO and JPO respectively relied upon these references to reject claims that are virtually identical to the claims of the '843 Patent.

For the foregoing reasons, Petitioner respectfully requests *Inter Partes* Review of Claims 1, 4, 8 and 9 of the '843 Patent.

II. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8(a)(1)

A. Real Party-In-Interest Under 37 C.F.R. § 42.8(b)(1)

Sharp Corporation, Sharp Electronics Corporation, and Sharp Electronics Manufacturing Company of America are the real parties-in-interest.

B. Related Matters Under 37 C.F.R. § 42.8(b)(2)

The '843 Patent is the subject of litigation in the District of Delaware, namely, *Surpass Tech Innovation LLC v. Sharp Corporation et al.*, Case No. 1:14-cv-00338-LPS (D. Del.) ("the Litigation"). Petitioner is among the named defendants in that Action.

C. Lead and Back-Up Counsel Under 37 C.F.R. § 42.8(b)(3)

Pursuant to 37 C.F.R. §§ 42.8(b)(3) and 42.10(a), Petitioner provides the following designation of lead and back-up counsel, as well as their respective service information.

Lead Counsel	Back-Up Counsel
Anthony F. Lo Cicero (Reg. No. 29,403) Amster, Rothstein & Ebenstein LLP 90 Park Avenue New York, NY 10016 Telephone: (212) 336–8110 Facsimile: (212) 336–8001 E-mail: alocicero@arelaw.com	Brian A. Comack (Reg. No. 45,343) Amster, Rothstein & Ebenstein LLP 90 Park Avenue New York, NY 10016 Telephone: (212) 336–8098 Facsimile: (212) 336–8001 E-mail: Sharp-843IPR@arelaw.com

Pursuant to 37 C.F.R. § 42.10(b), a Power of Attorney accompanies this Petition.

D. Service Information Under 37 C.F.R. § 42.8(b)(4)

Service information (by e-mail, postal mailing, or hand-delivery) for lead and back-up counsel is provided in the above designation of lead and back-up counsel.

III. PAYMENT OF FEES UNDER 37 C.F.R. § 42.103

The undersigned hereby provides authorization to charge Deposit Account No. 01-1785 to cover the fee of $23,000 for this Petition, as specified in 37 C.F.R. § 42.15(a). If this amount is insufficient or excessive, the Commissioner is authorized to deduct any underpayment from, or credit any overpayment to, Deposit Account No. 01-1785.

IV. GROUNDS FOR STANDING UNDER 37 C.F.R. § 42.104(a)

Petitioner certifies that: (1) the '843 Patent is available for *Inter Partes* Review and (2) the estoppel provisions of 35 U.S.C. § 315(e)(1) do not bar or estop Petitioner from requesting *Inter Partes* Review of any claim of the '843 Patent on the grounds raised herein.

V. IDENTIFICATION OF CHALLENGE UNDER 37 C.F.R. § 42.104(b) AND RELIEF REQUESTED

Petitioner requests *Inter Partes* Review and initiation of trial under 37 C.F.R. § 42.108 and cancellation of Claims 1, 4, 8 and 9 of the '843 Patent as unpatentable based on the statutory grounds set forth and explained below. In accordance with 37 C.F.R. §§ 42.6(c) and 42.63, a copy of the '843 Patent is submitted as Exhibit 1001. The publicly available records in the Office indicate that the '843 Patent is currently assigned to Surpass Tech Innovation LLC.

A. Claims for Which *Inter Partes* Review Is Requested Under 37 C.F.R. § 42.104(b)(1)

Petitioner requests *Inter Partes* Review of Claims 1, 4, 8 and 9 of the '843 Patent.

B. The Specific Art and Statutory Grounds on Which the Challenge Is Based Under 37 C.F.R. § 42.104(b)(2)

This Petition for *Inter Partes* Review is based on the following references, which are all prior art to the '843 Patent:

(1) U.S. Patent Application Publication No. 2002/0044115 ("Jinda," Ex. 1002), which was published on April 18, 2002 and is prior art under 35 U.S.C. § 102(b);

(2) Japanese Laid-Open Publication No. HEI 6-62355 ("Miyai," Ex. 1003), which was published on March 4, 1994 and is prior art under 35 U.S.C. § 102(b);

(3) U.S. Patent Application Publication No. 2001/0038369 ("Adachi," Ex. 1004), which was published on November 8, 2001 and is prior art under 35 U.S.C. § 102(b); and

(4) U.S. Patent Application Publication No. 2004/0196229 ("Ham," Ex. 1005), which is prior art under 35 U.S.C. § 102(e) because it was published on October 7, 2004 and is a continuation of an application filed on November 27, 2001, nearly two years before the earliest priority date of the '843 Patent.

Petitioner requests cancellation of Claims 1, 4, 8 and 9 on the following specific grounds:

Ground 1: Claims 1, 4, 8 and 9 are invalid under 35 U.S.C. § 102(b) as anticipated by Jinda;

Ground 2: Claims 1, 4, 8 and 9 are invalid under 35 U.S.C. § 103(a) as obvious over Jinda in view of Miyai;

Ground 3: Claims 1, 4, 8 and 9 are invalid under 35 U.S.C. § 102(b) as anticipated by Adachi;

Ground 4: Claims 4, 8 and 9 are invalid under 35 U.S.C. § 102(e) as anticipated by Ham.

For the reasons set forth herein, there is a reasonable likelihood that Petitioner will prevail in establishing that at least one of Claims 1, 4, 8 and 9 is unpatentable based on Grounds 1-4.

VI. SUMMARY OF THE '843 PATENT

The '843 Patent is entitled Driving Circuit of a Liquid Crystal Display Panel and Related Driving Method" and issued on April 10, 2007 from U.S. Patent Application No. 10/707,741 ("the '741 Application", Ex. 1006), filed on January 8, 2004. The '843 Patent claims priority to a Taiwanese patent application, TW92132122A, filed on November 17, 2003.

A. Specification of the '843 Patent

The '843 Patent generally relates to circuits and methods for driving an LCD panel. The LCD panel 30 described in the '843 Patent includes a number of well-known components common in prior art LCD modules, including a plurality of scan lines 32 (also called gate lines), a plurality of data lines 34, and a plurality of pixels 36. (Ex. 1001, '843 Patent, Col. 1:27-31, Col. 3:37-40). Each pixel 36 includes a switching device 38 (e.g., a TFT) and a liquid crystal device 39 (which is also called a "pixel electrode"). (*Id.* at Col.

3:40-43). These components are shown in Figure 4 of the '843 Patent (annotated and reproduced below), which also shows that the gate of the switching device 38 in each pixel is connected to the corresponding scan line 32, while the source of the switching device in the pixel is connected to the corresponding data line 34. (*Id.* at Col. 3:43-47). The LCD panel 30 is driven by applying scan line voltages to the scan lines 32 to turn on the switching devices 38 and applying data impulses to the data lines 34 to charge the liquid crystal devices 39 via the switching devices 38. (*Id.*).

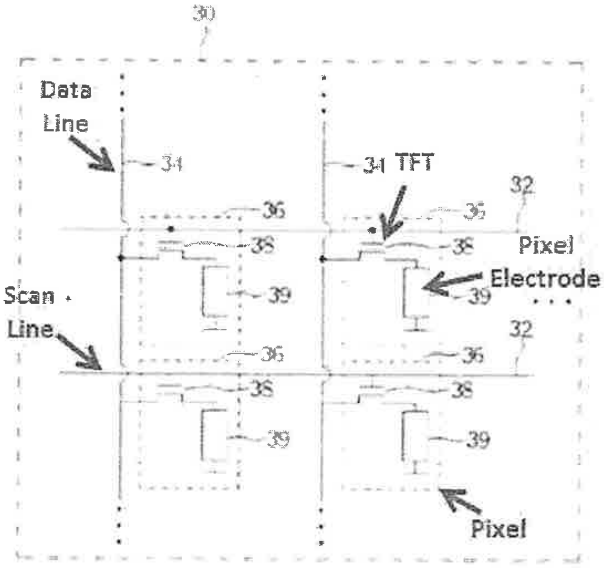


Fig. 4

As discussed above, the time that the pixel electrode needs to react to a driving voltage is called "response time." As was well known, the image quality of an LCD panel is dependent, in part, on this response time; the faster the response time, the better the image quality. In this regard, the '843 Patent explains that a delay in the response time of an LCD

panel causes image defects such as blurring, and describes the need for improving the LCD response speed. (*Id.* at Col. 1:21-26, Cols. 1:62-2:2).

In this regard, the '843 Patent discusses and claims two, previously known, techniques for improving the response time and resultant image quality of LCD displays: (1) "overdriving" the signal data; and (2) increasing the refresh rate (e.g., doubling) of the individual pixels.

As the '843 Patent explains, "overdriving" involves "applying a higher or a lower data impulse to the pixel electrode to accelerate the reaction speed of the liquid crystal molecules, so that the pixel can reach the predetermined gray level in a predetermined frame period." (*Id.* at Col. 2:2-7). In simple terms, overdriving enables a pixel to change from one gray level (i.e., shade of color) to another more quickly by either boosting or decreasing the requested pixel value. This decreases the difference between the before and after pixel values and the amount of time required for the pixel to change state.

The '843 Patent admits that the overdriving concept was known in the prior art. (*See id.* at Col. 4:17-19 ("***Same as the prior art***, ***the larger*** the value of the ***pixel data*** is [i.e. overdriving], the higher the voltage of the corresponding data impulse is, and ***the larger the gray level value*** is.") (emphasis added)). In this regard, the '843 Patent states that the "***conventional*** overdriving method" taught by U.S. Patent Application Publication No. 2002-0050965 A1 to Oda et al. could be used to increase LCD response speed. (*Id.* at Cols. 1:60-2:11) (emphasis added). Generally, an overdrive value is computed by comparing a given

pixel's ***previous*** gray level (also referred to as "transmission rate") with the pixel's ***current*** gray level in order to predict whether the gray level is increasing or decreasing. (*Id.* at Col. 5:34-44). The '843 Patent does not add anything new to this known method for computing the overdrive value.

The '843 Patent alleges that, while capable of improving response time to a certain extent, overdriving alone does not achieve adequate performance, namely reaching a desired transmission rate within a single frame period. (*See id.* at Col. 2:7-12, Fig. 2). As shown in Figure 2 of the '843 Patent (reproduced below), a single overdriven signal C2 is purportedly unable to reach a target transmission rate T2 within a single frame period N. Rather, according to this Figure, in the prior art, C2 would only reach T2 in the next frame period, N+1. According to the disclosure, since the pixels are unable to reach predetermined grey levels within a given frame period, the image could experience blurring. (*Id.* at Col. 1:21-37).

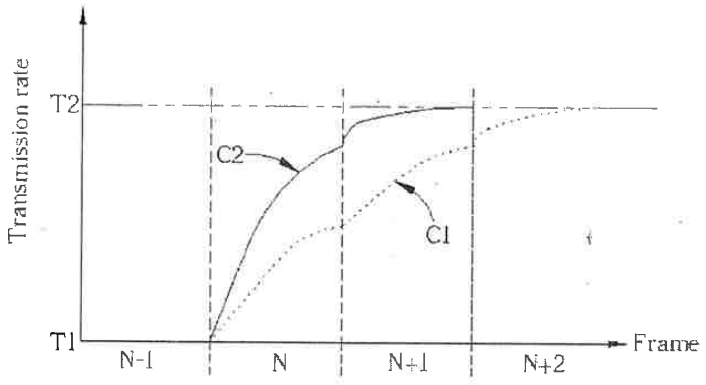


Fig. 2 Prior art

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To enable a signal to reach a target transmission rate T2 within a single frame period, the '843 Patent suggests applying two or more overdriven impulses to each pixel within the given frame period. (*Id.* at Col. 4:20-40). For example, as shown in Figure 6 of the '843 Patent, each single frame period is divided into two segments. For example, the Frame N+1 is divided into the segments n+2 and n+3. Two overdriven data impulses are then applied to these two segments (e.g., one impulse during n+2 and a second during n+3) to the pixel within the given frame period (e.g., N+1). This method allegedly allows the signal to reach a target transmission rate (T2) within a single frame period (e.g., N+1). (*Id.* at Cols. 3:15-4:43, Col. 5:45-55, Col. 1:39-41).

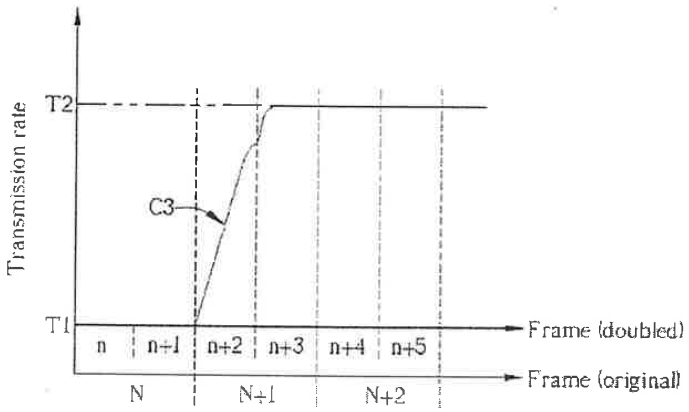


Fig. 6

Figure 3 (reproduced below, left) schematically illustrates an embodiment of the circuit for driving the LCD panel 30. The driving circuit 10 includes a blur clear converter 14, a source driver 18, and a gate driver 20. The blur clear converter 14 continuously receives,

through a signal controller 12, a plurality of frame data G. The frame data includes the data necessary to drive all of the pixels of the panel 30. The blur clear converter 14 then generates the overdriven pixel data for each pixel within each frame period based on the frame data. (*Id.* at Col. 3:24-28). Figure 5 (reproduced below, right) shows two overdriven pixel data GN+1 and GN+1(2) generated by the blur clear converter 14 for each pixel in the frame period N+1.

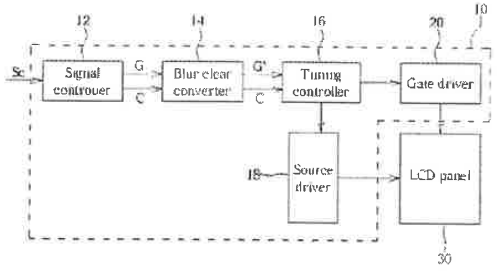


Fig. 3

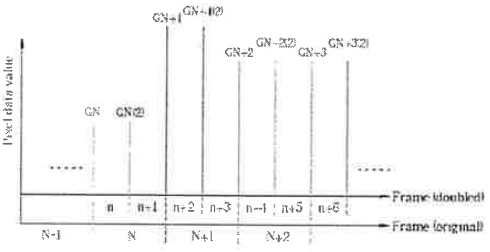


Fig. 5

The source driver 18 then converts the overdriven pixel data (e.g., GN+1 and GN+1(2)) into the corresponding data impulses. (*Id.* at Col. 3:28-36). The data impulses are applied to the liquid crystal device 39 of a pixel 36 within the corresponding frame period (e.g., at each half of the frame period N+1 as shown in Fig. 5) via the data line 34 in order to control the transmission rate of the liquid crystal device 39. (*Id.* at Col. 4:8-14). The gate driver 20 generates the corresponding scan line voltage and applies it to the scan line 32 to turn on the switching device 38 of the pixel 36 so that the data impulses from the source driver 18 can be applied to the liquid crystal device 39 of the pixel. (*Id.* at Col. 3:28-36).

B. Claims 1, 4, 8 and 9 of the '843 Patent

Independent Claim 1 of the '843 Patent is an apparatus claim directed to a driving circuit for driving an LCD panel. The claimed driving circuit "generat[es] a ***plurality of overdriven*** pixel data within every frame period for each pixel." (*Id.* at Claim 1) (emphasis added). In other words, Claim 1 requires circuitry for applying ***two or more overdriven*** impulses to each pixel within a frame period, as shown in Figures 5 and 6 above.

Claims 4, 8 and 9 are method claims directed to methods of driving an LCD display. Claim 4 is in independent form. In contrast to Claim 1, method Claims 4, 8 and 9 are only directed to "generating a ***plurality*** of data impulses for each pixel within every frame period according to the frame data." (*Id.* at Claim 4) (emphasis added). Method claims 4-9 do not require performing the overdrive technique.

C. Prosecution History of the '843 Patent

The claims of the '843 Patent were allowed during prosecution without being the subject of any prior art rejection. In the Statement of Reason for Allowance, the Examiner identified two prior art references, including Ham, as relevant. (Ex. 1006, pp. 214-215). With respect to Ham, the Examiner stated:

> Ham (US 20040196229) shows apply[ing] the normal data to the liquid crystal panel at the initial half period of the frame after supplying of the modulated data to the liquid crystal panel during the later half period of the frame, thus a desired brightness level is achieved within the initial period of the frame.

(*Id.*). The Examiner recognized that the prior art disclosed generating and applying a plurality of data impulses for each pixel within every frame period, which is precisely what is required by Claims 4, 8, and 9. Yet, the Examiner did not explain how this very relevant teaching in Ham was allegedly different than the claimed subject matter. As discussed below, because Ham discloses all of the elements of Claims 4, 8, and 9, these Claims should not have been allowed. Moreover, the Examiner never discussed or addressed Jinda or Adachi.

VII. CLAIM CONSTRUCTION UNDER 37 C.F.R. § 42.104(b)(3)

Petitioner submits that, for purposes of this Petition only, the terms of Claims 1, 4, 8 and 9 of the '843 Patent are generally clear on their face, and should be given their broadest reasonable construction in light of the specification of the '843 Patent. 37 C.F.R. § 42.100(b).

Petitioner notes an apparent typographical error in Claim 1. Specifically, Claim 1 recites "a source driver for generating a plurality of data impulses to each pixel according to the plurality of overdriven pixel data generated by the blur clear converter and applying the data impulses to the liquid crystal device of the pixel via the ***scan line*** connected to the pixel within one frame period in order to control transmission rate of the liquid crystal device." However, the '843 Patent explains that data impulses are applied via the ***data line,*** not the scan line. (*See, e.g.,* Ex. 1001, '843 Patent, Col. 3:47-51 ("To drive the LCD 30, . . . data voltages are applied to the data lines 34 and transmitted to the pixel electrodes

30....")). As discussed below, the cited prior art (or combination of prior art) discloses the same driving circuit configuration disclosed in the '843 Patent. Therefore, irrespective of this error, Claim 1 is invalid.

VIII. APPLICATION OF CITED PRIOR ART TO EVERY CLAIM FOR WHICH *INTER PARTES* REVIEW IS REQUESTED UNDER 37 C.F.R. § 42.104(b)(4)-(5)

As explained below, (1) Claims 1, 4, 8 and 9 are invalid under 35 U.S.C. § 102(b) as anticipated by Jinda; (2) Claims 1, 4, 8 and 9 are invalid under 35 U.S.C. § 103(a) as obvious over Jinda in view of Miyai; (3) Claims 1, 4, 8 and 9 are invalid under 35 U.S.C. § 102(b) as anticipated by Adachi; and (4) Claims 4, 8 and 9 are invalid under 35 U.S.C. § 102(e) as anticipated by Ham.

Before turning to each Ground, Petitioner addresses two issues that are relevant to the obviousness analyses in Ground 2, namely the level of ordinary skill in the art and secondary considerations of non-obviousness. For purposes of the obviousness analyses presented below, Petitioner submits that a person of ordinary skill in the art has an undergraduate degree in electrical engineering, or equivalent work experience, and would have had two to five years of experience in using or designing driving devices for LCD panels.

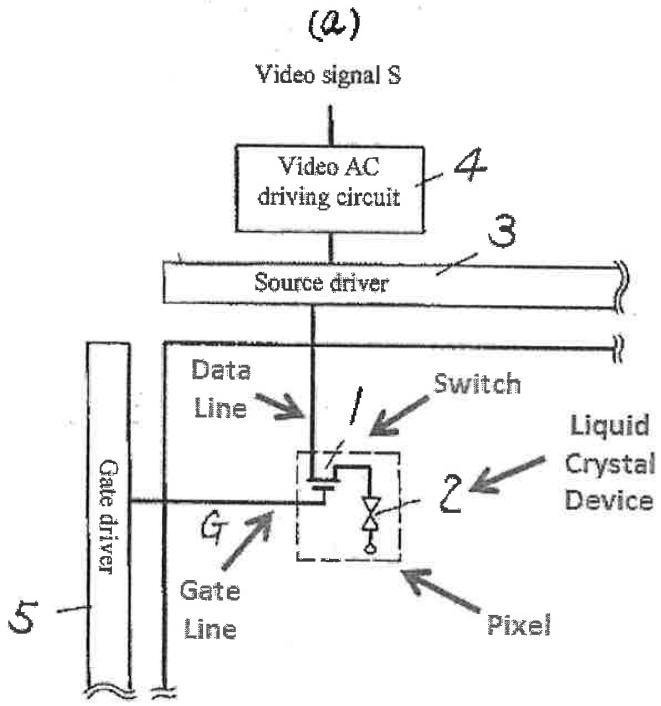
In addition, for purposes of the obviousness analyses presented below, Petitioner is not aware of any secondary considerations that would render Claims 1, 4, 8 or 9 nonobvious.

A. Ground 1: Claims 1, 4, 8 and 9 are invalid under 35 U.S.C. § 102(b) as anticipated by Jinda

1. The Disclosure of Jinda

Jinda was published on April 18, 2002 and is prior art to the '843 Patent under pre-AIA 35 U.S.C. § 102(b). Jinda is the publication of a U.S. application filed by Petitioner. Jinda was cited by the Applicant during prosecution of the '843 Patent, but was not referred to or discussed by the Examiner. As discussed below, the EPO found that Jinda anticipated virtually identical claims to those in question here, but the Applicant never told the USPTO about the EPO's findings.

Like the '843 Patent, Jinda discloses a method for "improving the response characteristic of liquid crystals and further improving the display quality of dynamic images" in "matrix type" LCD displays. (Ex. 1002, Jinda, ¶ [0007], *see also* ¶ [0002]). For example, Jinda incorporates Miyai by reference, and identifies various issues with "conventional" LCD displays, including the LCD display disclosed in Miyai. This "conventional liquid crystal panel" includes a matrix of pixels 2, each of which includes a liquid crystal device 2 and a switching device 1 (i.e., a TFT). (Ex. 1003, English Translation ¶ [0003]). The switching device is connected to a gate line and a data line. This arrangement shown in Figure 3(a) of the incorporated Miyai reference, which is reproduced and annotated below:

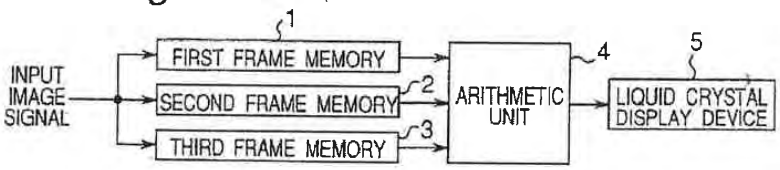


As discussed below, Jinda discloses the same two techniques disclosed in the '843 Patent for improving the image quality of a conventional LCD panel (e.g., the LCD Panel of Miyai), namely, (1) overdriving the signal data; and (2) increasing the refresh rate of the pixels.

Jinda discloses a circuit for receiving an input image signal comprising multiple frames of video. (Ex. 1002, Jinda, ¶ [0036], Fig. 1). Frame data is sequentially written into one of the first, second or third frame memories, as shown in Figure 1 below. (*Id.* ¶ [0036]). At any given point in time, one frame memory will contain the current frame data, a second

will contain the previous frame data, and a third is available to receive new frame data (*Id.* ¶¶ [0037]-[0038], Figs. 1-3).

Fig.1



An "arithmetic unit 4" retrieves data from the frame memory (1, 2, or 3) and compares the "data value of the previous image signal and the data value of the current image signal" to output overdriven pixel data. (*Id.* ¶ [0039]). In this regard, Jinda explains that: (a) "a data value of a value greater than the data value of the current image signal is written when the data value of the current image signal is greater than the data value of the previous image signal"; and (b) "a data value of a value smaller that the data value of the current image signal is written when the data value of the current image signal is smaller than the data value is smaller than the data value of the previous image signal." (*Id.*). In other words, the output data is overdriven—using a voltage of a greater magnitude (either higher or lower)—based on the prior image signal.

This is all illustrated in the look-up table of Figure 4 of Jinda (reproduced below). For example, when the data value of the previous image signal is 20 and the data value of the current image signal is 10, a lower (overdriven) signal value of 8 will be outputted. By contrast, when the data value of the previous image signal is 10 and the data value of the

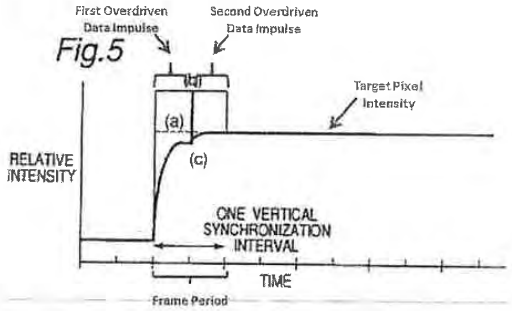
current image signal is 20, a higher (overdriven) signal value of 22 will be outputted. According to Jinda, this overdriving technique is necessary to "to make the liquid crystals have a rapid response." (*Id.* ¶ [0006]).

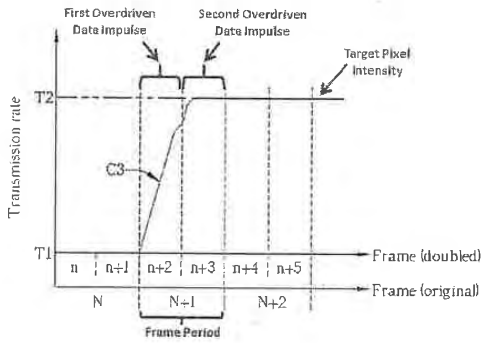
Fig.4

		DATA VALUE OF PREVIOUS IMAGE SIGNAL					
		10	20	30	40	50	60
DATA VALUE OF CURRENT IMAGE SIGNAL	10	10	8	6	4	2	0
	20	22	20	18	16	14	12
	30	34	32	30	28	26	24
	40	46	44	42	40	38	36
	50	58	56	54	52	50	48
	60	70	68	66	64	62	60

In addition, Jinda teaches applying the overdriven image data to each pixel a "plurality of times within one vertical synchronization interval" (i.e., a single frame period). (*See, e.g.*, *id.* ¶ [0010]; *see also* ¶¶ [0041]-[0042]). Jinda explains "that the repetitive input of the data value (b) is effective for the improvement of the rise of the light transmittance (c) of the [LCD] device," which reduces blurring and increases image quality. (*Id.* ¶ [0042]; *see also* ¶ [0046]). In one embodiment, the transmission rate of the LCD input data is doubled. (*Id.* ¶ [0041], Fig. 5), while, in another embodiment, the transmission rate of the LCD input data is tripled. (*Id.* ¶ [0067], Fig. 16). This enables "achievement of high-speed image display and the improvement of the dynamic image display quality." (*Id.* ¶ [0045]).

An annotated version of Figure 5 of Jinda, showing the application of two overdriven data impulses in each frame period, is reproduced below (left). As can be seen, Figure 5 of Jinda is indistinguishable from Figure 6 of the '843 Patent (reproduced below, right).





2. The European Counterpart of the '843 Patent Was Rejected In View of Jinda

On December 22, 2003, the original assignee of the '843 Patent ("Applicant") filed a virtually identical application with the EPO, which was assigned European Patent App. No. 03029643.8 ("the EPO Application"). (*See* Ex. 1007, p. 1). The EPO Application names the same inventors and contains the same specification and figures as the '843 Patent. (*See id.* at pp. 7-31). A copy of the relevant documents from the prosecution history of the EPO Application is attached hereto as Exhibit 1007.

The EPO Application, as originally filed, included nine claims, which were virtually identical to the nine claims filed in the U.S.[1] (*See id.* at pp. 32-37). As relevant here, Claim 7 of the EPO Application required "a blur clear converter (14, 60) for receiving frame data

[1] In the EPO Application, the claims are presented in a different order (e.g., the method claims before the apparatus claims).

every frame period, each frame data comprising a plurality of pixel data and each pixel data corresponding to a pixel (36), the blur clear converter (14, 60) delaying current frame data to generate delayed frame data and generating a plurality of overdriven pixel data within every frame period for each pixel (36)," which is also required in Claim 1 of the'843 Patent. (*Id.*at pp. 34-35). Similarly, EPO Claim 1 required "generating a plurality of data impulses for each pixel (36) within every frame period according to the frame data," which is required by Claim 4 of the '843 Patent. (*Id.* at p. 32).

On June 22, 2004, the EPO issued a Search Report identifying two "X" (i.e., anticipatory) references relevant to all nine claims, including the same Jinda reference relied upon in this Petition. (*Id.* at p. 48). The EPO also issued a preliminary action rejecting all of the claims as being unpatentable over Jinda. (*Id.* at pp. 40-43). The EPO Examiner found that Jinda "discloses . . . a blur clear converter" of EPO Claim 7, as shown in Figures 1 and 4 of Jinda. (*Id.* at pp. 41-42). The Examiner also found that Jinda disclosed the steps of "generating" and "applying [a plurality] the data impulses to the liquid crystal device . . . of one of the pixels within one frame period . . . in order to control a transmission rate of the pixel," as shown in Figures 5, 9 and 14 of Jinda. (*Id.* at p. 41). In addition, the examiner stated that Jinda does not explicitly disclose some of the well-known components of an LCD display (e.g., scan lines, data lines, switching devices), but found that these basic elements are "implicitly" disclosed. (*Id.*).

Rather than challenge the examiner's findings, the Applicant submitted a new set of claims directed to specific methods for driving an LCD display (all of which included generating a plurality of overdriven pixel data for each frame), and argued that these new claims were allowable over Jinda. (*Id.* at pp. 56-61). However, the Examiner rejected the narrower claims in view of Jinda. (*Id.* at pp. 62-67). In response, the Applicant only argued that Jinda does not implicitly disclose the known LCD components discussed above (e.g., scan lines, data lines, switching devices). (*Id.* at pp. 62-63). The Applicant did not challenge the EPO's determination that Jinda disclosed applying a plurality of overdriven pixel data within one frame period, which again, is also a requirement of Claim 1 of the '843 Patent.

On November 24, 2009, the EPO issued a summons to attend oral proceedings and responded to the Applicant's arguments. (*Id.* at p. 66). The EPO found that, even if the basic LCD components are not disclosed by Jinda, they are disclosed in prior art incorporated by reference in Jinda, including the same Miyai reference relied upon in this Petition (i.e., Japanese Laid-Open Publication No. HEI 6-62355). (*Id.* at p. 70). The Applicant did not attend the oral argument conducted by the EPO and, as a result, the application was refused and prosecution was closed. (*Id.* at pp. 78-81).

During the pendency of the prosecution of the '843 Patent, the applicant submitted an Information Disclosure Statement in the U.S. Patent Office identifying the prior art references cited by the EPO. However, neither the European Search Report itself nor the

related European Office Action were submitted to the U.S. Patent Office (even though they were issued long before the '843 Patent was granted). As such, the U.S. Examiner did not have the benefit of the EPO's highly relevant analysis.

3. Claims 1, 4, 8 and 9 are anticipated by Jinda

As shown in the claim charts set forth below, Jinda discloses each and every element of independent Claims 1, 4, 8 and 9 of the '843 Patent. Accordingly, these claims are invalid under 35 U.S.C. § 102(b) as anticipated by Jinda.

Specifically, Jinda discloses the key elements of Claims 1, 4, 8 and 9. Jinda plainly discloses the "blur clear converter" of Claim 1, namely, a circuit that generates two or more overdriven impulses for each frame period, for each pixel. Likewise, Jinda discloses the key element of Claims 4, 8 and 9, i.e., generating two of more data impulses for each pixel within a given frame period.

Jinda's Figures do not explicitly show some of the known elements of an LCD panel, such the scan lines, data lines and switching devices claimed in the '843 Patent. However, these known elements are disclosed by Miyai, which is incorporated by reference into Jinda.[2] Specifically, Miyai discloses an LCD panel and driving circuit for improving the response speed of the panel. (Ex. 1002, Jinda, ¶ [0004]). The driving circuit of Miyai utilizes an overdriving technique to accomplish this objective. (*Id.* (stating that Miyai

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[2] The EPO examiner took the similar position during the prosecution of the European Counterpart to the '843 Patent that "the teaching of [HEI 6-62355] is considered to be incorporated in [Jinda]." (Ex. 1007, pp. 57-58 ¶ 1.2).

"discloses the improvement in the step response characteristic of liquid crystals by superimposing a difference component by comparison with the previous image signal")). Jinda incorporates, and improves upon, the driving circuit of Miyai. (*Id.* ¶ [0006]).

In any event, the known LCD panel components are also inherent in the disclosure of Jinda. Jinda notes that, "although no detailed description is provided," "the voltage of the data value is applied to the pixel electrode (not shown) of the desired pixel by the image signal thus transferred to the liquid crystal display device **5**." (*Id.* ¶ [0038]). It would be impossible to perform this function (i.e., applying a desired voltage to a pixel) without a scan line, a data line, and a switching device (e.g., a TFT) connected to each pixel. As such, one of ordinary skill in the art would appreciate that such known elements are necessarily disclosed by Jinda.

The Claims Of The '843 Patent	Disclosure of U.S. Patent Application Publication No. 2002/0044115 (Jinda)
1. A driving circuit for driving an LCD panel, the LCD panel comprising:	Jinda discloses a "drive circuit" for an LCD panel (*E.g.*, Ex. 1002, Jinda, ¶ [0019]).
a plurality of scan lines;	The "matrix type" LCD Panel disclosed by Jinda (Ex. 1002, Jinda, ¶ [0002]) inherently includes a plurality of scan lines to control the pixels. In addition, Miyai (incorporated by reference in Jinda) discloses a plurality of scan lines. (Ex. 1003, Miyai, ¶ [0003], Fig. 3(a)).
a plurality of data lines; and	The "matrix type" LCD Panel disclosed by Jinda (Ex. 1002, Jinda, ¶ [0002]) inherently includes a plurality of data lines to control the pixels. In addition, Miyai (incorporated by reference in Jinda) discloses a plurality of data lines. (Ex. 1003, Miyai, ¶

The Claims Of The '843 Patent	Disclosure of U.S. Patent Application Publication No. 2002/0044115 (Jinda)
	[0003], Fig. 3).
a plurality of pixels, each pixel being connected to a corresponding scan line and a corresponding data line, and each pixel comprising a liquid crystal device and a switching device connected to the corresponding scan line, the corresponding data line, and the liquid crystal device,	Jinda discloses a plurality of pixels (Ex. 1002, Jinda, ¶ [0038]). Each pixel is inherently connected to a corresponding scan line and a corresponding data line in the "matrix type" LCD display disclosed by Jinda (*Id.* ¶ [0002]). Each pixel includes a "pixel electrode" (i.e., a liquid crystal device). Each pixel inherently includes a switching device connected to the corresponding scan line, the corresponding data line, and the liquid crystal device. In addition, Miyai (incorporated by reference in Jinda) discloses this limitation. (Ex. 1003, Miyai, ¶ [0003], Fig. 3(a)).
the driving circuit comprising: a blur clear converter for receiving frame data every frame period, each frame data comprising a plurality of pixel data and each pixel data corresponding to a pixel, the blur clear converter delaying current frame data to generate delayed frame data and generating a plurality of overdriven pixel data within every frame period for each pixel;	Jinda discloses a "drive circuit" comprising "frame memory" for receiving frame data every frame period, each frame data comprising a plurality of pixel data and each pixel data corresponding to a pixel ("Digital image signals for R, G and B of pixels") (Ex. 1002, Jinda, ¶ [0036]). The drive circuit delays "the current image signal" to generate delayed frame data and generates a plurality of overdriven pixel data (*id.* at Fig. 4) within every "vertical synchronization interval" for each pixel (*E.g., id.* ¶¶ [0010], [0037], [0067], Figs. 1-5, 15-16).
a source driver for generating a plurality of data impulses to each pixel according to the plurality of overdriven pixel data generated by the blur clear converter and applying the data impulses to the liquid crystal device of the pixel via the scan line connected to the pixel within one frame period in order to	Jinda discloses generating a plurality of data impulses to each pixel according to the plurality of overdriven pixel data generated by the arithmetic unit (Ex. 1002, Jinda, ¶¶ [0038], [0067], Figs. 1, 4-5, 15-16) and "supplying image data to be written into each pixel of the liquid crystal display device to the liquid crystal display device a plurality of times in one vertical synchronization interval." (*Id.* ¶ [0008]). The drive circuit of Jinda inherently includes a data line connected to each pixel

The Claims Of The '843 Patent	Disclosure of U.S. Patent Application Publication No. 2002/0044115 (Jinda)
control transmission rate of the liquid crystal device; and ,	for applying the data impulses to the liquid crystal device. In addition, Miyai (incorporated by reference in Jinda) discloses a data line connected to each pixel for applying the data impulses to the liquid crystal device. (*See, e.g.,* Ex. 1003, Miyai, Fig. 3(a)).
a gate driver for applying a scan line voltage to the switch device of the pixel so that the data impulses can be applied to the liquid crystal device of the pixel.	The drive circuit of Jinda inherently includes a gate driver for applying a scan line voltage to the switch device of the pixel so that the data impulses can be applied to the liquid crystal device of the pixel. In addition, Miyai (incorporated by reference in Jinda) discloses a gate driver for applying a scan line voltage to the switch device of the pixel so that the data impulses can be applied to the liquid crystal device of the pixel. (Ex. 1003, Miyai, ¶ [0003], Fig. 3(a)).
4. A method for driving a liquid crystal display (LCD) panel, the LCD panel comprising:	Jinda discloses a "liquid crystal display device driving method" (*E.g.,* Ex. 1002, Jinda, ¶ [0019], Fig. 1).
a plurality of scan lines;	Miyai (incorporated by reference in Jinda) discloses a plurality of scan lines. (Ex. 1003, Miyai, ¶ [0003], Fig. 3(a)). In addition, the "matrix type" LCD Panel disclosed by Jinda (Ex. 1002, ¶ [0002]) inherently includes a plurality of scan lines to control the pixels.
a plurality of data lines; and	The "matrix type" LCD Panel disclosed by Jinda (Ex. 1002, Jinda, ¶ [0002]) inherently includes a plurality of data lines to control the pixels. In addition, Miyai (incorporated by reference in Jinda) discloses a plurality of data lines. (Ex. 1003, Miyai, ¶ [0003], Fig. 3).
a plurality of pixels, each pixel being connected to a corresponding scan line and a corresponding data line, and each pixel comprising a liquid crystal device and a switching	Jinda discloses a plurality of pixels (Ex. 1002, Jinda, ¶ [0038]). Each pixel is inherently connected to a corresponding scan line and a corresponding data line in the "matrix type" LCD display disclosed by Jinda (*Id.* ¶ [0002]). Each pixel includes a "pixel electrode" (i.e., a liquid crystal device). Each pixel inherently includes a

The Claims Of The '843 Patent	Disclosure of U.S. Patent Application Publication No. 2002/0044115 (Jinda)
device connected to the corresponding scan line, the corresponding data line, and the liquid crystal device, and	switching device connected to the corresponding scan line, the corresponding data line, and the liquid crystal device. In addition, Miyai (incorporated by reference in Jinda) discloses this limitation. (Ex. 1003, Miyai, Fig. 3).
the method comprising: receiving continuously a plurality of frame data;	Jinda discloses receiving continuously a plurality of "[d]igital image signals for R, G and B of pixels sequentially read from video equipment" (*E.g.,* Ex. 1002, Jinda, ¶ [0036], Figs. 1, 2, 15).
generating a plurality of data impulses for each pixel within every frame period according to the frame data; and	Jinda discloses generating two or more data impulses for each pixel within every "one vertical synchronization interval" according to the frame data (*E.g.,* Ex. 1002, Jinda, ¶¶ [0041], [0044]-[0046], Figs. 5, 16).
applying the data impulses to the liquid crystal device of one of the pixels within one frame period via the data line connected to the pixel in order to control a transmission rate of the liquid crystal device of the pixel.	Jinda discloses applying the data impulses to the liquid crystal device of one of the pixels within one frame period. (*E.g.,* Ex. 1002, Jinda, ¶¶ [0041], [0044]). The "matrix type liquid crystal display" of Jinda (Ex. 1002, Jinda ¶ [0002]) inherently includes a data line connected to each pixel in order to control the transmission rate of the liquid crystal device of the pixel. In addition, Miyai (incorporated by reference in Jinda) discloses applying data impulses to the liquid crystal device of one of the pixels via the data line connected to the pixel in order to control a transmission rate of the liquid crystal device of the pixel. (*See, e.g.*, Ex. 1003, Miyai, ¶ [0003], Fig. 3).
8. The method of claim 4 further comprising: applying a scan line voltage to the switch device of the pixel via the scan line connected to the pixel in order to have the data impulses be applied to the liquid crystal device of the pixel.	Jinda discloses applying a scan line voltage to the switch device of the pixel via the scan line connected to the pixel in order to have the data impulses be applied to the liquid crystal device of the pixel. (*E.g.,* Ex. 1002, Jinda, ¶ [0041]). The scan line voltage and switch device are inherent to the LCD device of Jinda. In addition, Miyai (incorporated by reference in Jinda) discloses this limitation. (Ex. 1003, Miyai, ¶ [0003], Fig.

The Claims Of The '843 Patent	Disclosure of U.S. Patent Application Publication No. 2002/0044115 (Jinda)
	3(a)).
9. The method of claim 4 wherein each frame data comprises a plurality of pixel data, and each pixel data corresponds to a pixel.	Jinda discloses that each frame data comprises a plurality of pixel data (i.e., RGB) and each pixel data corresponds to a pixel (*E.g.,* Ex. 1002, Jinda, ¶¶ [0036], [0041]).

B. Ground 2: Claims 1, 4, 8 and 9 are invalid under 35 U.S.C. § 103(a) as obvious over Jinda in view of Miyai

1. Claims 1, 4, 8 and 9 are obvious over Jinda in view of Miyai

As discussed above, Petitioner contends that Miyai is incorporated by reference in Jinda and, therefore, Jinda explicitly (and at a minimum inherently) discloses each element of Claims 1, 4, 8 and 9. In addition to being anticipated by Jinda, Claims 1, 4, 8 and 9 are invalid under 35 U.S.C. § 103(a) as obvious over Jinda in view of Miyai. Miyai was published on March 4, 1994 and is prior art to the '843 Patent under pre-AIA 35 U.S.C. § 102(b). As discussed above, Miyai discloses a conventional LCD panel that includes a matrix of pixels, each of which includes a liquid crystal device and a switching device. (Ex. 1003, Miyai, ¶ [0003], Fig. 3(a)). Each switching device is connected to a gate (or scan) line and a data line. (*Id.*). As shown below, the LCD panel of Miyai (below, left) is identical to the LCD panel of the '843 Patent (below, right):

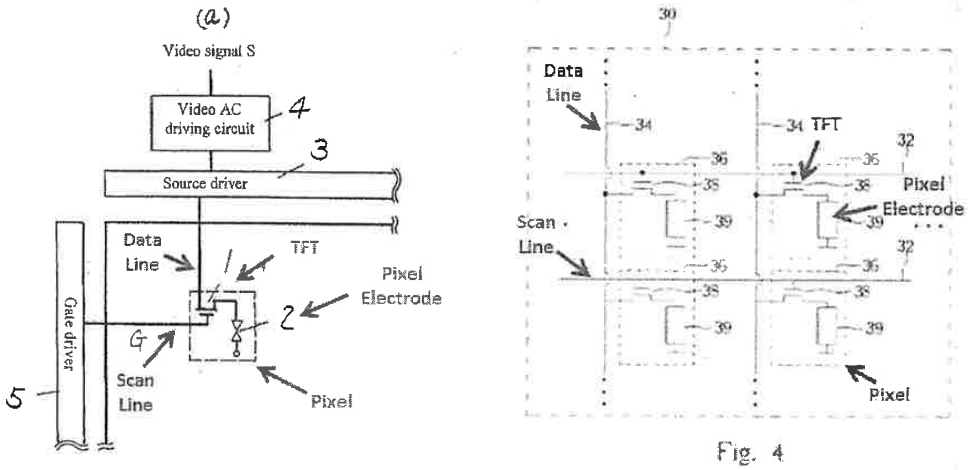


Fig. 4

Miyai is discussed in the background section of Jinda. (Ex. 1002, Jinda, ¶¶ [0004], [0006]). Specifically, Jinda identifies various shortcomings of the LCD display of the Miyai, which it seeks to improve upon. Accordingly, Jinda ***expressly*** teaches one of ordinary skill the art to combine the disclosed driving circuit with the LCD panel of Miyai. *See, e.g. Bayer Healthcare Pharms., Inc. v. Watson Pharms., Inc.*, 713 F.3d 1369, 1374 (Fed. Cir. 2013) (one prior art reference's citation to a second reference provided "express motivation to combine those teachings to derive the claimed" invention).

In addition, under Supreme Court precedent, "any need or problem known in the field" can provide a reason for combining prior art elements. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 420 (2007). Here, one of ordinary skill in the art would have been motivated to combine the teachings of Jinda and Miyai because both references focused on the exact same problem—improving the image quality of LCD displays and, more particularly,

improving the response time of the display. (*Compare e.g.,* Ex. 1002, Jinda, ¶ [0007] ("[T]he object of the present invention is to provide a liquid crystal display device driving method capable of improving the response characteristic of liquid crystals and further improving the display quality . . . .") *with* Ex. 1003, Miyai, ¶ [0006] ("[A]n object [of the invention] is to improve responsiveness and achieve an improvement in image quality . . . in the driving circuit of display elements with slow response speed, such as liquid crystal panels.").

Thus, under *KSR*, it would have been obvious to generate a plurality of overdriven pixel data in each frame period, as taught by Jinda, to improve the image quality of the "conventional" LCD panel of Miyai.

As shown in the claim charts set forth below, Jinda and Miyai combine to teach each and every element of Claims 1, 4, 8 and 9 of the '843 Patent. Accordingly, these claims are invalid under 35 U.S.C. § 103(a) as obvious over Jinda in view of Miyai.

Claims Of The '843 Patent	Disclosure of Jinda and Miyai
1. A driving circuit for driving an LCD panel, the LCD panel comprising:	Jinda discloses a "drive circuit" for an LCD panel (*E.g.,* Ex. 1002, Jinda, ¶ [0019]).
a plurality of scan lines;	Miyai discloses a plurality of scan lines (Ex. 1003, Miyai, ¶ [0003], Fig. 3(a)).
a plurality of data lines; and	Miyai discloses a plurality of data lines (Ex. 1003, Miyai, ¶¶ [0003], [0013], Fig. 3(a)).
a plurality of pixels, each pixel being connected to a corresponding scan line and a corresponding data line, and	Miyai discloses a plurality of pixels (region within dashed line), each pixel being connected to a corresponding scan line and a corresponding data line, and each pixel comprising a liquid crystal device 2 and a switching

Claims Of The '843 Patent	Disclosure of Jinda and Miyai
each pixel comprising a liquid crystal device and a switching device connected to the corresponding scan line, the corresponding data line, and the liquid crystal device,	device 1 connected to the corresponding scan line, the corresponding data line, and the liquid crystal device (Ex. 1003, Miyai, ¶ [0003], Fig. 3(a)).
the driving circuit comprising: a blur clear converter for receiving frame data every frame period, each frame data comprising a plurality of pixel data and each pixel data corresponding to a pixel, the blur clear converter delaying current frame data to generate delayed frame data and generating a plurality of overdriven pixel data within every frame period for each pixel;	Jinda discloses a "drive circuit" comprising "frame memory" for receiving frame data every frame period, each frame data comprising a plurality of pixel data and each pixel data corresponding to a pixel ("Digital image signals for R, G and B of pixels") (Ex. 1002, Jinda, ¶ [0036]). The drive circuit delays "the current image signal" to generate delayed frame data and generates a plurality of overdriven pixel data (*See id.* at Fig. 4) within every "vertical synchronization interval" for each pixel (*E.g., id.* ¶¶ [0010], [0037], [0067], Figs. 1-5, 15-16).
a source driver for generating a plurality of data impulses to each pixel according to the plurality of overdriven pixel data generated by the blur clear converter and applying the data impulses to the liquid crystal device of the pixel via the scan line connected to the pixel within one frame period in order to control transmission rate of the liquid crystal device; and	Jinda discloses generating a plurality of data impulses to each pixel according to the plurality of overdriven pixel data generated by the arithmetic unit (Ex. 1002, Jinda, ¶¶ [0038], [0067], Figs. 1, 4-5, 15-16) and "supplying image data to be written into each pixel of the liquid crystal display device to the liquid crystal display device a plurality of times in one vertical synchronization interval." (*Id.* ¶ [0008]). Miyai discloses a data line connected to each pixel for applying the data impulses to the liquid crystal device (E.*g.*, Ex. 1003, Miyai, ¶ [0003], Fig. 3(a)).
a gate driver for applying a scan line voltage to the switch device of the pixel so that the data impulses can be applied to the liquid crystal device of the pixel.	Miyai discloses a gate driver for applying a scan line voltage to the switch device of the pixel so that the data impulses can be applied to the liquid crystal device of the pixel (*See, e.g.*, Ex. 1003, Miyai,¶ [0003], Fig. 3(a)).
4. A method for driving a liquid crystal display (LCD) panel, the	Jinda discloses a "liquid crystal display device driving

Claims Of The '843 Patent	Disclosure of Jinda and Miyai
LCD panel comprising:	method" (*E.g.* Ex. 1002. ¶ [0019], Fig. 1).
a plurality of scan lines;	Miyai discloses a plurality of scan lines G (Ex. 1003, Miyai, ¶ [0003]; Fig. 3(a)).
a plurality of data lines; and	Miyai discloses a plurality of data lines (Ex. 1003, Miyai, ¶ [0003], Fig. 3(a)).
a plurality of pixels, each pixel being connected to a corresponding scan line and a corresponding data line, and each pixel comprising a liquid crystal device and a switching device connected to the corresponding scan line, the corresponding data line, and the liquid crystal device, and	Miyai discloses a plurality of pixels (region within dashed line), each pixel being connected to a corresponding scan line and a corresponding data line, and each pixel comprising a liquid crystal device 2 and a switching device 1 connected to the corresponding scan line, the corresponding data line, and the liquid crystal device (Ex. 1003, Miyai, ¶ [0003], Fig. 3(a)).
the method comprising: receiving continuously a plurality of frame data;	Jinda discloses receiving continuously a plurality of "[d]igital image signals for R, G and B of pixels sequentially read from video equipment" (*E.g.,* Ex. 1002, Jinda, ¶ [0036], Figs. 1, 2, 15).
generating a plurality of data impulses for each pixel within every frame period according to the frame data; and	Jinda discloses generating two or more data impulses for each pixel within every "one vertical synchronization interval" according to the frame data (*E.g.,* Ex. 1002, Jinda, ¶¶ [0041], [0044]-[0046], Figs. 5, 16).
applying the data impulses to the liquid crystal device of one of the pixels within one frame period via the data line connected to the pixel in order to control a transmission rate of the liquid crystal device of the pixel.	Jinda discloses applying "the data value (voltage value) of the image signal that is inputted to the liquid crystal display device 5" (Ex. 1002, Jinda, ¶ [0041]) within one frame period (*E.g., id.* ¶¶ [0041], [0044]). Miyai discloses a data line connected to each pixel in order to control the transmission rate of the liquid crystal device of the pixel (*E.g.*, Ex. 1003, Miyai, ¶ [0003], Fig. 3(a)).
8. The method of claim 4 further comprising: applying a scan line voltage to the switch device of the pixel via the scan line connected to the pixel in order	Miyai discloses applying a scan line voltage to the switch device of the pixel via the scan line connected to the pixel in order to have the data impulses be applied to the liquid crystal device of the pixel. (*E.g.*, Ex. 1003, Miyai, ¶ [0003], Fig. 3(a)).

Claims Of The '843 Patent	Disclosure of Jinda and Miyai
to have the data impulses be applied to the liquid crystal device of the pixel.	
9. The method of claim 4 wherein each frame data comprises a plurality of pixel data, and each pixel data corresponds to a pixel.	Jinda discloses that each frame data comprises a plurality of pixel data (i.e., RGB) and each pixel data corresponds to a pixel (*E.g.,* Ex. 1002, Jinda, ¶¶ [0036], [0041]).

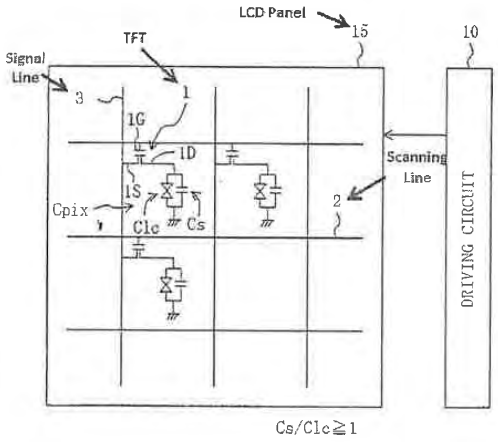
C. Ground 3: Claims 1, 4, 8 and 9 are invalid under 35 U.S.C. § 102(b) as anticipated by Adachi

1. The Disclosure of Adachi

Adachi (also assigned to Sharp) was published on November 8, 2001 and is prior art to the '843 Patent under 35 U.S.C. § 102(b).

Adachi discloses, among other things, an "active-matrix liquid crystal display" panel 15 that includes "a plurality of picture-element capacitors Cpix arranged in a matrix, and TFTs **1** electrically connected to the respective picture-element capacitors Cpix." (Ex. 1004, Adachi, ¶¶ [0009], [0165]). "Each TFT **1** has its gate electrode 1G connected to a corresponding scanning line **2** and its source electrode 1S connected to a corresponding signal line **3**." (*Id.* ¶ [0165]). "The driving circuit **10** applies a scanning voltage and a driving voltage to the scanning and source lines, respectively." (*Id.*). "Each TFT **1** has its drain electrode ID connected to a corresponding picture-element capacitor Cpix." (*Id.*). The arrangement of these basic components is shown in Figure 12 of Adachi, which is reproduced below:

FIG. 12



Like the '843 Patent, Adachi discloses various methods and circuits for improving the response characteristics of the display, including the use of overdriving and increasing the refresh rate (e.g., doubling). (*Id.* ¶ [0158]). In this regard, Adachi discloses a "driving circuit [that] supplies to the LC panel a predetermined driving voltage overshooting a gray-level voltage corresponding to an input image signal of a current vertical period, according to a combination of an input image signal of an immediately preceding vertical period and the input image signal of the current vertical period." (*Id.* at Abstract; *see also* ¶¶ [0006]-[0009]).

In addition, Adachi "[n]ote[s] that, in the case where a ***single frame is divided into a plurality of fields*** for driving, it is preferable that the first field or all the fields are subjected to the ***overshoot*** driving." (*Id.* ¶ [0112]) (emphasis added). Put differently, Adachi teaches applying a plurality of overdriven data impulses to the LCD panel in each frame period (e.g., "at a double speed"). This is illustrated in Figure 11 of Adachi (annotated and reproduced in

part below, left), which is strikingly similar to Figures 2 and 6 of the '843 Patent (below, right).

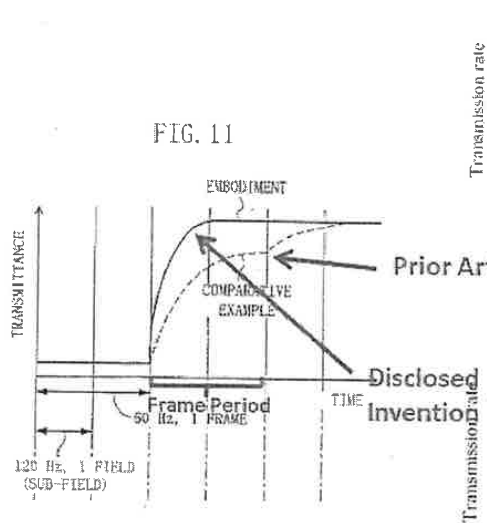
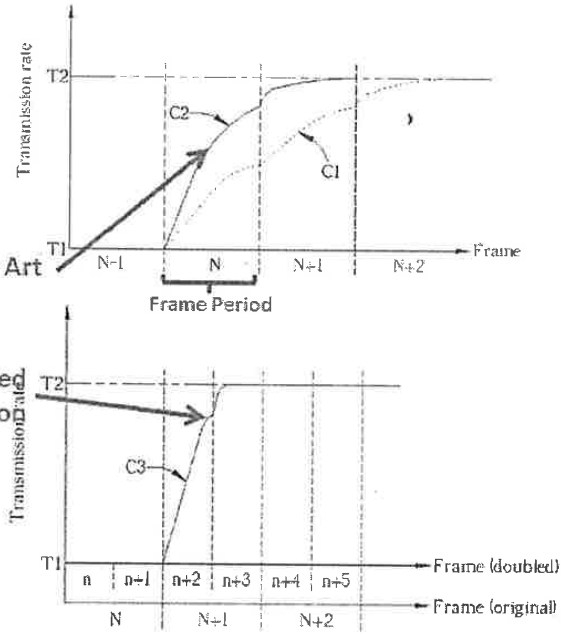


Fig. 11 of Adachi (Partial)



Figs. 2 (top) and 6 (bottom) of the '843 Patent

Figure 11 of Adachi compares the "response characteristics" (i.e., the performance) of the "embodiment" of the invention (*see* the solid line) and a prior art "comparative example" (*see* the dashed line), both of which receive a 60 Hz image signal as an input. In the "embodiment" represented by the solid line, the input signal is subject to "overshoot driving" and "is written at a double speed to the liquid crystal panel" (i.e., at 120 Hz). (Ex. 1004, Adachi, ¶ [0157]). Thus, as shown above, the desired transmittance is obtained

within a single frame (i.e., the "1 FRAME") period, and blurring is therefore reduced. (*Id.* ¶ [0158]).

By contrast, in the comparative prior art example represented by the dashed line, the input signal is not overdriven or written to the panel at a higher speed. (*Id.*). The transmittance in the prior art example is, therefore, unable to attain the desired transmittance in a single frame period. (*Id.*). Thus, blurring will occur.

2. The Japanese Counterpart of the '843 Patent Was Rejected In View of Adachi

The Applicant also filed a counterpart of the '741 Application with the Japanese Patent Office ("JPO"), which was assigned Japanese Patent App. No. JP20030417655 ("the JPO Application"). (Ex. 1008, p. 2). The JPO Application names the same inventors and contains the same specification and figures as the '843 Patent. (*Id.*). A copy of the relevant documents from the prosecution history of the JPO Application is attached as Exhibit 1008.

Like the claims of the EPO Application, the nine claims of the JPO Application were virtually identical to the nine claims filed in the U.S. (*See id.* at pp. 7-9). During prosecution, the claims of the Japanese counterpart were repeatedly rejected by the JPO examiner in view of various Japanese language references, including a Japanese application having the same figures asthe Adachi reference relied upon in this Petition, JP 2001-343956 ("JP Adachi"). (*Id.* at p. 17). For example, in a June 25, 2007 Office Action, the JPO found that JP Adachi disclosed "that when one frame is divided into a plurality of fields and driven, it is preferable to perform overshoot drive for all of the fields . . . ." (Ex.

1008, p. 16). In addition, the JPO noted that "[t]he feature of doubling the speed by reading memory at twice the speed of writing is commonly used technology in the applicable field . . . ." (*Id.* at p. 17). In short, the JPO found that all of elements of Japanese Claims 1, 5, 6 and 7, which are virtually identical to Claims 1, 4, 8 and 9 of the '843 Patent, were explicitly disclosed by JP Adachi.

The Applicant did not attempt to traverse these prior art rejections. Instead, the Applicant narrowed the application claims to by including limitations relating to the calculation of the overshoot amount, which are not found in the claims of the '843 Patent. (*Id.* at pp. 23-24). The JPO patent issued on October 10, 2008.

3. Claims 1, 4, 8 and 9 are anticipated by Adachi

As shown in the claim charts set forth below, Adachi explicitly teaches each and every element of Claims 1, 4, 8 and 9 of the '843 Patent. Accordingly, these claims are invalid as anticipated under 35 U.S.C. § 102(b).

Specifically, Adachi discloses the key elements of Claims 1, 4, 8 and 9. Adachi plainly discloses the "blur clear converter" of Claim 1, namely, a circuit that generates two or more overdriven impulses for each frame period, for each pixel. Likewise, Adachi discloses the key element of Claims 4, 8 and 9, namely, generating two or more data impulses for each pixel within a given frame period. In addition, the dependent Claims 8 and 9 merely recite known LCD driving methods, which are similarly disclosed by Adachi.

Claims Of The '843 Patent	Disclosure of U.S. Patent Application Publication No. 2001/0038369 (Adachi)
1. A driving circuit for driving an LCD panel, the LCD panel comprising:	Adachi discloses "[a] liquid crystal (LC) display device includes a LC panel and a driving circuit." (*E.g.,* Ex. 1004, Adachi, Abstract; Fig. 10).
a plurality of scan lines;	Adachi discloses an LCD panel having a plurality of "scanning line 2" (*E.g.*, Ex. 1004, Adachi, ¶ [0165], Fig. 12).
a plurality of data lines; and	Adachi discloses an LCD panel having a plurality of "signal line 3" (i.e., data lines) (*E.g.*, Ex. 1004, Adachi, ¶ [0165], Fig. 12).
a plurality of pixels, each pixel being connected to a corresponding scan line and a corresponding data line, and each pixel comprising a liquid crystal device and a switching device connected to the corresponding scan line, the corresponding data line, and the liquid crystal device,	Adachi discloses a plurality of pixels ("Cpix"), each connected to a corresponding "scanning line 2" and a corresponding "signal line 3," and each pixel includes a "liquid crystal" "picture-element" and a switching devices (i.e., TFT) connected to the corresponding "scanning line," the corresponding "signal line" and the "picture-element." (*E.g.*, Ex. 1004, Adachi, ¶ [0165], Fig. 12).
the driving circuit comprising: a blur clear converter for receiving frame data every frame period, each frame data comprising a plurality of pixel data and each pixel data corresponding to a pixel, the blur clear converter delaying current frame data to generate delayed frame data and generating a plurality of overdriven pixel data within every frame period for each pixel;	Adachi discloses a driving circuit that receives frame data ("input image signal S") every frame period (Adachi, ¶¶ [0062], [0100]), each frame data comprising a plurality of pixel data and each pixel data corresponding to a pixel, the blur clear converter delaying current frame data to generate delayed frame data and generating a plurality of overdriven pixel data within every frame period for each pixel. (*E.g.,* ¶¶ [0157]-[0158], Fig. 11).
a source driver for generating a plurality of data impulses to each pixel according to the plurality of overdriven pixel	Adachi discloses a "driving circuit 10" (Fig. 10) for generating a plurality of data impulses to each pixel (Cpix) according to the plurality of overdriven pixel data generated by the blur clear converter and applying the data impulses

Claims Of The '843 Patent	Disclosure of U.S. Patent Application Publication No. 2001/0038369 (Adachi)
data generated by the blur clear converter and applying the data impulses to the liquid crystal device of the pixel via the scan line connected to the pixel within one frame period in order to control transmission rate of the liquid crystal device; and	to the liquid crystal device of the pixel via the "signal line 3" connected to the pixel within one frame period in order to control transmission rate of the liquid crystal device (*E.g.*, Ex. 1004, Adachi, ¶¶ [0157]-[0158], [0165], Figs. 11,12).
a gate driver for applying a scan line voltage to the switch device of the pixel so that the data impulses can be applied to the liquid crystal device of the pixel.	Adachi discloses a "driving circuit" that "applies a scanning voltage" to the "TFTs" of the pixel so that the data impulses can be applied to the "picture-element" (i.e., pixels) (*E.g.*, Ex. 1004, Adachi, ¶ [0165], Figs. 10, 12).
4. A method for driving a liquid crystal display (LCD) panel, the LCD panel comprising:	Adachi discloses a method for driving an LCD panel. (E.*g.*, Ex. 1004, Abstract, Fig. 10).
a plurality of scan lines;	Adachi discloses an LCD panel having a plurality of "scanning line 2" (*E.g.*, Ex. 1004, Adachi, ¶ [0165], Fig. 12).
a plurality of data lines; and	Adachi discloses an LCD panel having a plurality of "signal line 3" (i.e., data lines) (E.*g.*, Ex. 1004, Adachi, ¶ [0165], Fig. 12).
a plurality of pixels, each pixel being connected to a corresponding scan line and a corresponding data line, and each pixel comprising a liquid crystal device and a switching device connected to the corresponding scan line, the corresponding data line, and the liquid crystal device, and	Adachi discloses a plurality of pixels ("Cpix"), each connected to a corresponding "scanning line 2" and a corresponding "signal line 3," and each pixel includes a "liquid crystal" "picture element" and a switching devices (i.e., TFT) connected to the corresponding "scanning line," the corresponding "signal line" and the "picture-element." (*E.g.*, Ex. 1004, Adachi, ¶ [0165], Fig. 12).
the method comprising: receiving continuously a plurality of frame data;	Adachi discloses receiving continuously a plurality of frame data ("input image signal S"). (Ex. 1004, Adachi, ¶¶ [0062], [0100]).

Claims Of The '843 Patent	Disclosure of U.S. Patent Application Publication No. 2001/0038369 (Adachi)
generating a plurality of data impulses for each pixel within every frame period according to the frame data; and	Adachi discloses generating a plurality of data impulses for each pixel within every frame period according to the frame data. (Ex. 1004, Adachi, ¶¶ [0112], [0157]-[0158], Fig. 11).
applying the data impulses to the liquid crystal device of one of the pixels within one frame period via the data line connected to the pixel in order to control a transmission rate of the liquid crystal device of the pixel.	Adachi discloses "appl[ying] a scanning voltage" to the "TFTs" of the pixel so that the data impulses can be applied to the "picture-element" (i.e., pixels) (*E.g.*, Ex. 1004, Adachi, ¶¶ [0157]-[0158], [0165], Fig. 10-11).
8. The method of claim 4 further comprising: applying a scan line voltage to the switch device of the pixel via the scan line connected to the pixel in order to have the data impulses be applied to the liquid crystal device of the pixel.	Adachi discloses applying a "scanning voltage" to the switch device ("TFT 1") of the pixel via the "scanning line 2" connected to the pixel in order to have the data impulses be applied to the liquid crystal device of the pixel (Ex. 1004, ¶ [0165], Fig. 10).
9. The method of claim 4 wherein each frame data comprises a plurality of pixel data, and each pixel data corresponds to a pixel.	Adachi discloses that each frame data comprises a plurality of pixel data, and each pixel data corresponds to a pixel. (Ex. 1004, ¶ [0165], Fig. 10).

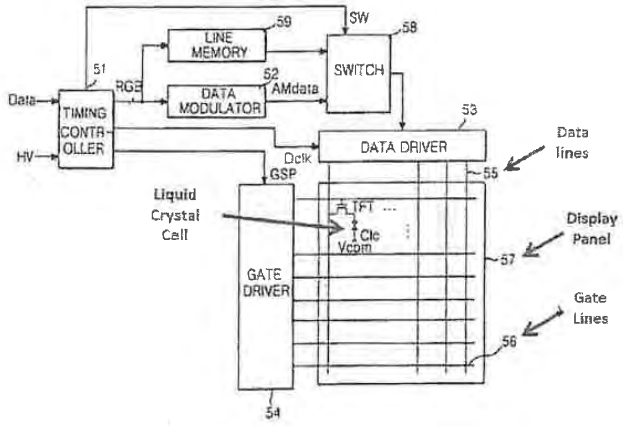
D. Ground 4: Claims 4, 8 and 9 are invalid under 35 U.S.C. § 102(e) as anticipated by Ham

1. The Disclosure of Ham

Ham was published on October 7, 2004 and is a continuation of an application filed on November 27, 2001, nearly two years before the earliest possible priority date of the '843 Patent. Ham is prior art to the '843 Patent under 35 U.S.C. § 102(e).

Ham is directed to a "method and apparatus for driving a liquid crystal display device suitable for enhancing a picture quality." (Ex. 1005, Ham, Abstract). As shown in Figure 5 of Ham (annotated and reproduced below), the "LCD driving apparatus includes a liquid crystal display panel **57** having a plurality of data lines **55** and a plurality of gate lines **56** crossing each other and having TFT's provided at each intersection to drive liquid crystal cells Clc." (*Id.* ¶ [0037]).

FIG. 5

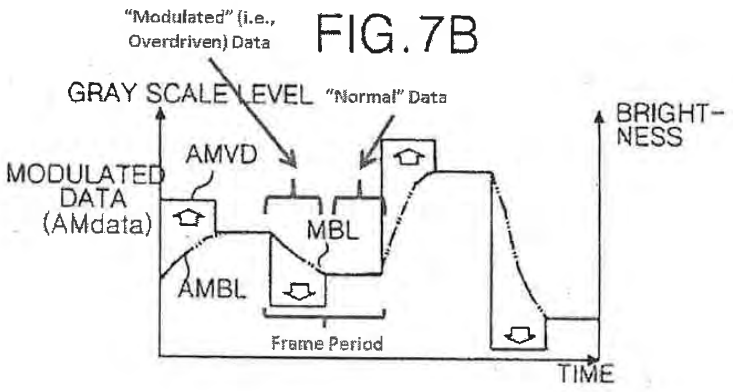


Ham recognizes that, if overdriven pixel data is applied "through the entire period of the frame" (as taught by the prior art), "picture quality may be deteriorated." (*Id.* ¶ [0052]).

To address this problem, Ham teaches applying overdriven pixel data in only the first half of the frame period, and applying non-overdriven data in the second half of the frame period. (*Id.* ¶ [0053]).

The apparatus also includes a "timing controller 51" that "receives digital video data" and a "data modulator 52" that generates ***two data impulses*** (i.e., "modulated data" signal and "normal data" signal) for each pixel within one frame period. (*Id.* ¶ [0037] ("Each gate start pulse GSP and each gate shift clock GSC have a frequency twice greater than those of the conventional gate start pulse and the gate shift clock. Thus, they allow all scanning lines **56** on the liquid crystal display panel **57** to be scanned twice within one frame interval."); *see also id.* ¶ [0040], Fig. 7C).

As shown in the Table 1 of Ham, "modulated data" is selected from a look-up table based upon the data voltage of the "previous frame" and the data voltage of the "current frame." (*Id.* ¶¶ [0013], [0017]). As a result, the "modulated data" signal is overdriven. On the other hand, the "normal data" signal is simply the actual data received by the controller (i.e., it is not overdriven). The output of the circuit disclosed by Ham is shown in Figure 7B (annotated and reproduced below). As can be seen, each frame period is split into two halves. During the first half of the frame period, overdriven data is applied to each pixel. During the second half of the frame period, non-overdriven data is applied.



2. Claims 4, 8 and 9 are anticipated by Ham

As shown in the claim charts set forth below, Ham discloses each and every element of Claims 4, 8 and 9 of the '843 Patent. Accordingly, these claims are invalid under 35 U.S.C. § 102(e) as anticipated by Ham.

Specifically, Ham discloses the key element of Claims 4, 8 and 9, namely, generating two of more data impulses for each pixel within a given frame period. Dependent Claims 8 and 9 merely recite known LCD driving methods, which are similarly disclosed by Ham.

Claims Of The '843 Patent	Disclosure of U.S. Patent Application Publication No. 2004/0196229 (Ham)
4. A method for driving a liquid crystal display (LCD) panel, the LCD panel comprising:	Ham Discloses "a method . . . for driving a liquid crystal display device suitable for enhancing a picture quality." (*E.g.*, Ex. 1005, Ham, Abstract, ¶ [0003]).
a plurality of scan lines;	The LCD panel of Ham includes a "plurality of gate lines 56" (i.e., scan lines). (*E.g.*, Ex. 1005, Ham, ¶ [0037], Fig. 5).

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Claims Of The '843 Patent	Disclosure of U.S. Patent Application Publication No. 2004/0196229 (Ham)
a plurality of data lines; and	The LCD panel of Ham includes a "plurality of data lines 55." (*E.g.*, Ex. 1005, ¶ [0037], Fig. 5).
a plurality of pixels, each pixel being connected to a corresponding scan line and a corresponding data line, and each pixel comprising a liquid crystal device and a switching device connected to the corresponding scan line, the corresponding data line, and the liquid crystal device, and	The LCD panels includes a plurality of "pixels" (Ex. 1005, Ham, ¶ [0038]). Each pixel is connected to a corresponding "gate lines 56" and a corresponding "data lines 55," and each pixel includes a "liquid crystal cell Clc" and a switching device (i.e., a "TFT") connected to the corresponding "gate lines 56," the corresponding "data lines 55," and the "liquid crystal cell Clc" (*e.g.*, *id.* ¶ [0037], Fig. 5).
the method comprising: receiving continuously a plurality of frame data;	The method includes continuously "receiv[ing] digital video data." (*E.g.*, Ex. 1005, Ham, ¶¶ [0003], [0037], Fig. 5).
generating a plurality of data impulses for each pixel within every frame period according to the frame data; and	The method includes generating two data impulses (i.e., "modulated data" and "normal data") for each pixel "within one frame period." (E.*g.*, ¶¶ [0040]-[0041], ¶ [0053] ("[T]he LCD drive apparatus and method according to the present invention appl[ies] the normal data to the liquid crystal panel at the initial half period of the frame after supplying of the modulated data to the liquid crystal panel during the later half period of the frame . . . . ").
applying the data impulses to the liquid crystal device of one of the pixels within one frame period via the scan line connected to the pixel in order to control a transmission rate of the liquid crystal device of the pixel.	The method includes applying the data impulses to "the liquid crystal cell" "within one frame interval" via the "data lines 55" connected to the "liquid crystal cell" to double the transmission rate of the cell. (*E.g.*, Ex. 1005, Ham, ¶¶ [0037], [0040], Figs. 5, 7C).

Claims Of The '843 Patent	Disclosure of U.S. Patent Application Publication No. 2004/0196229 (Ham)
8. The method of claim 4 further comprising: applying a scan line voltage to the switch device of the pixel via the scan line connected to the pixel in order to have the data impulses be applied to the liquid crystal device of the pixel.	The method includes applying a "scanning pulse to the gate lines 56 of the liquid crystal display panel 57" in order to have the data impulses be applied to the "liquid crystal cells" of the pixel. (*E.g.*, Ex. 1005, Ham, ¶ [0037]-[0038], [0044], Fig. 5).
9. The method of claim 4 wherein each frame data comprises a plurality of pixel data, and each pixel data corresponds to a pixel.	Each frame of data includes a plurality of pixel data (i.e., "normal data RGB"), and each pixel data corresponds to pixel (i.e., "liquid crystal cell") (*E.g.*, Ex. 1005, Ham, ¶ [0042], Fig. 6).

IX. CONCLUSION

For the reasons discussed above, Petitioner has established a reasonable likelihood that it will prevail with respect to at least one of Claims 1, 4, 8 and 9 of the '843 Patent challenged in this Petition. Therefore, this Petition should be granted, *Inter Partes* Review should be instituted, and Claims 1, 4, 8 and 9 should be found unpatentable and cancelled.

Respectfully submitted,

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Dated: October 3, 2014
New York, New York

By: */Anthony F. Lo Cicero No. 29,403/*
Anthony F. LO CICERO
Registration No.: 29,403

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §§ 42.6(e) and 42.105, I hereby certify that on this 3rd day of October, 2014, a true copy of the foregoing PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 7,202,843, together with Petitioner's Exhibit List, Exhibit Nos. 1001-1008 and PETITIONER'S POWER OF ATTORNEY FOR AN *INTER PARTES* REVIEW, was served via EXPRESS MAIL® on the Patent Owner at the following correspondence address of record for the subject patent:

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
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MERRIFIELD, VA 22116

Dated: October 3, 2014
New York, New York

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583127.3

United States Patent [19]

Marentic et al.

[11] **Patent Number: 4,464,657**

[45] **Date of Patent: Aug. 7, 1984**

[54] **MODULAR WAVEFORM GENERATOR FOR PLASMA DISPLAY PANELS**

[75] Inventors: **Michael J. Marentic**, Orange; **Daniel A. Manseau**, Garden Grove, both of Calif.

[73] Assignee: **Interstate Electronics Corp.**, Anaheim, Calif.

[21] Appl. No.: **273,092**

[22] Filed: **Jun. 12, 1981**

[51] **Int. Cl.**³ **G09G 3/28**

[52] **U.S. Cl.** **340/776**; 315/169.4; 340/767; 340/779; 340/799; 340/805

[58] **Field of Search** 340/713, 767, 771, 776, 340/779, 805; 315/169.4

[56] **References Cited**

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4,183,062	1/1980	Weisbrod	340/776 X

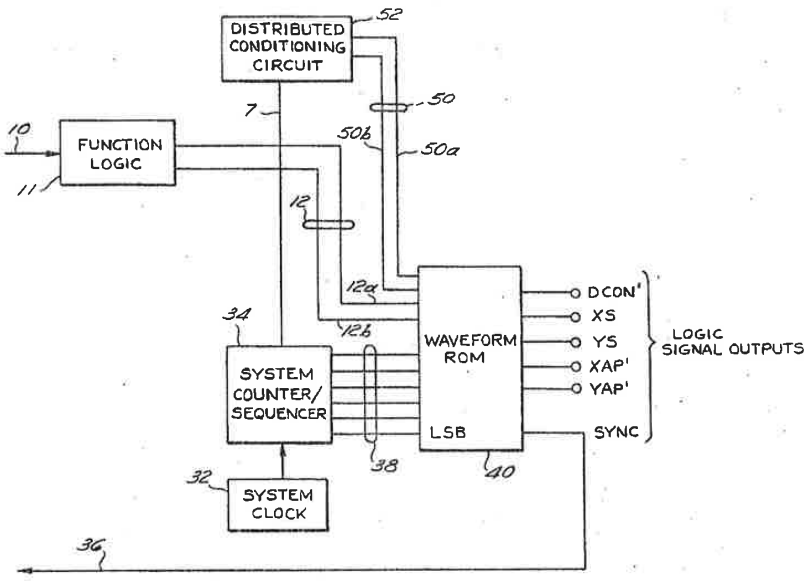
Primary Examiner—David L. Trafton

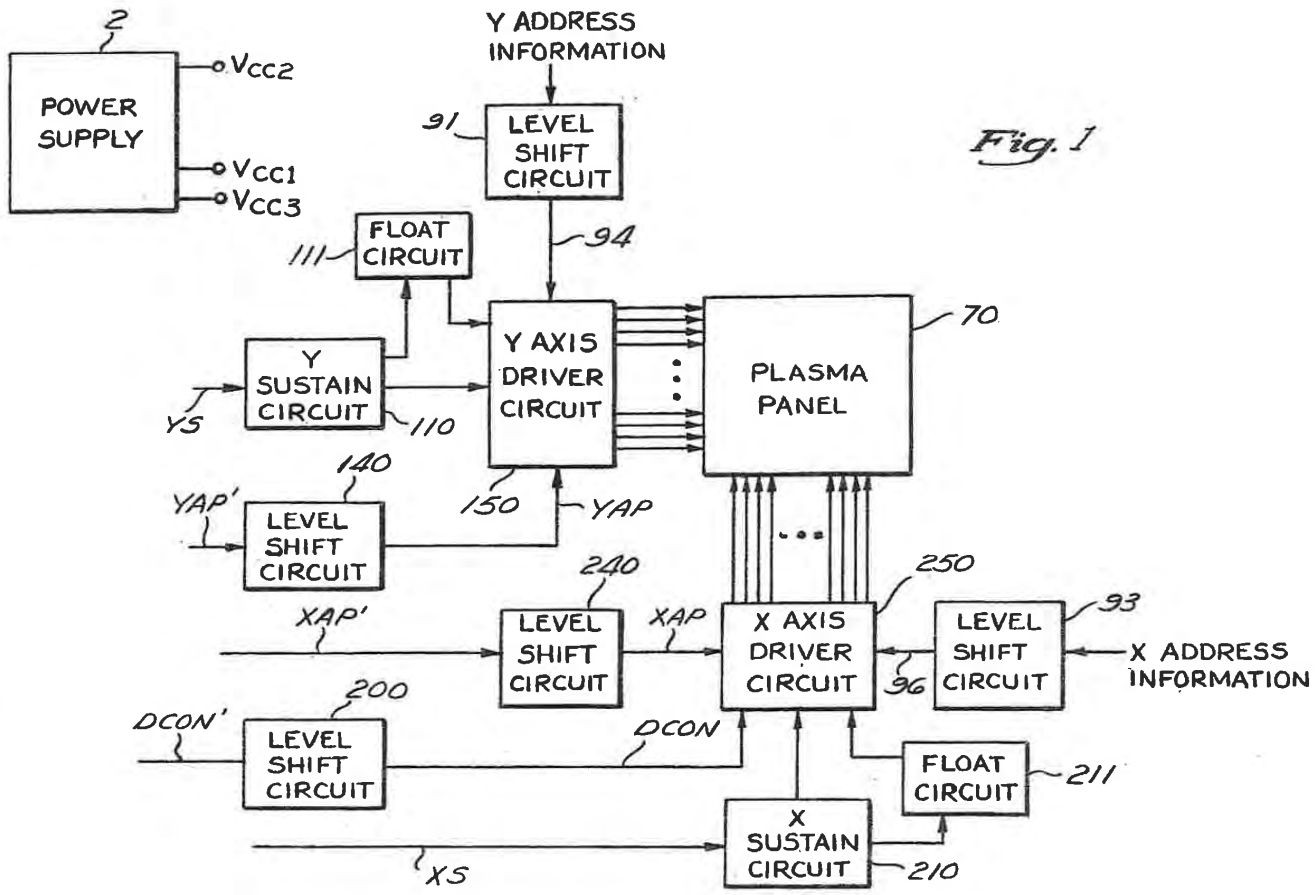
Attorney, Agent, or Firm—Knobbe, Martens, Olson & Bear

[57] **ABSTRACT**

Complex waveforms used to control a plasma panel are formed as sequences of common elemental waveform modules. These modules are combined in various orders into strings capable of performing various functions on the plasma panel. Large scale parallel addressing is accomplished by forming a string of several sustain modules, followed by a write or erase module.

33 Claims, 10 Drawing Figures




2
POWER SUPPLY
Vcc2
Vcc1
Vcc3
Y ADDRESS INFORMATION
91
LEVEL SHIFT CIRCUIT
94
111
FLOAT CIRCUIT
Y SUSTAIN CIRCUIT
110
YS
Y AXIS DRIVER CIRCUIT
150
YAP
70
PLASMA PANEL
140
YAP'
LEVEL SHIFT CIRCUIT
240
XAP'
LEVEL SHIFT CIRCUIT
XAP
250
X AXIS DRIVER CIRCUIT
96
93
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DCON'
LEVEL SHIFT CIRCUIT
DCON
FLOAT CIRCUIT
211
X SUSTAIN CIRCUIT
210
XS

Fig. 1

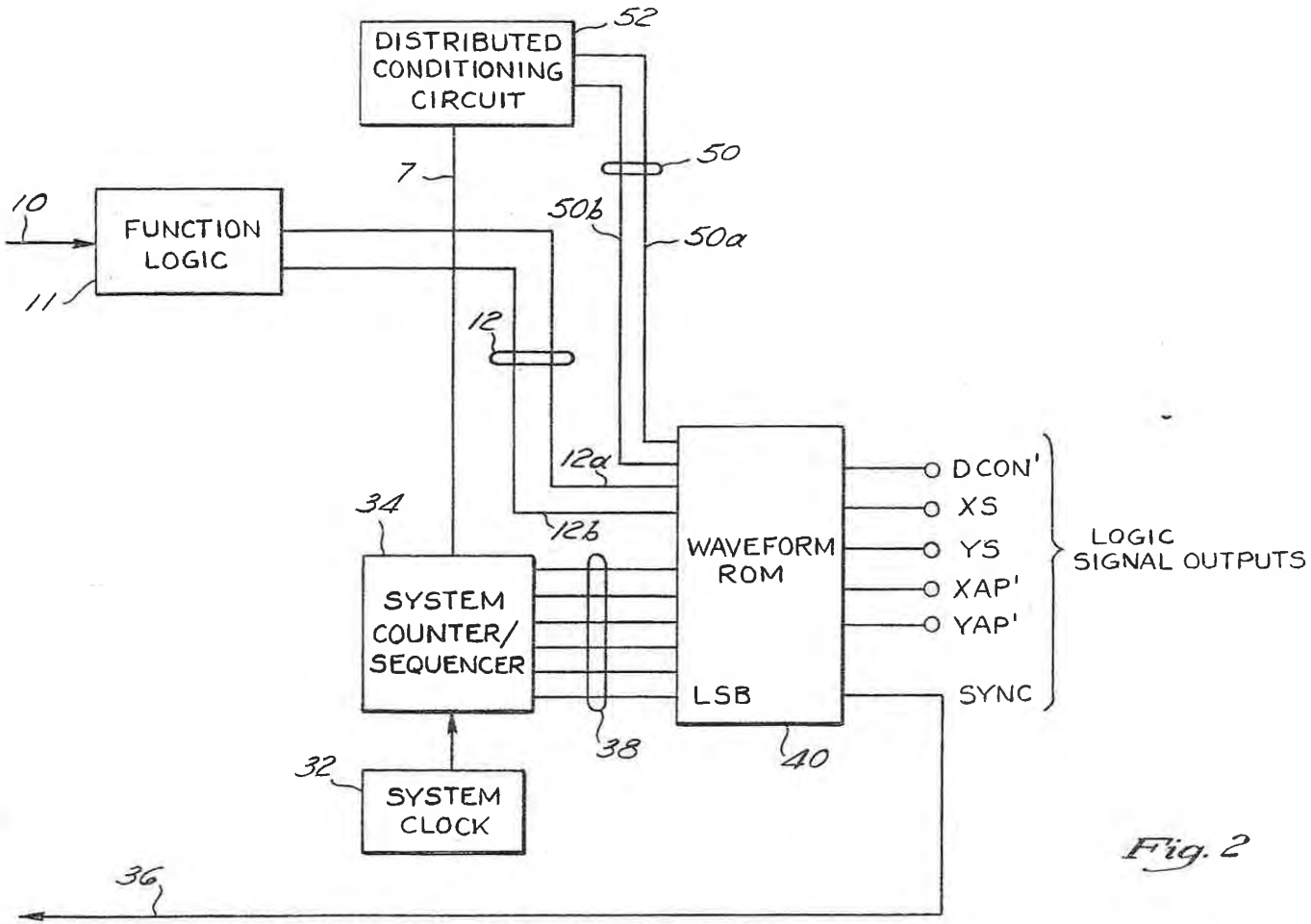
DISTRIBUTED CONDITIONING CIRCUIT
52
50
7
10
FUNCTION LOGIC
50b
50a
11
12
12a
34
12b
WAVEFORM ROM
DCON'
XS
YS
XAP'
YAP'
LOGIC SIGNAL OUTPUTS
SYSTEM COUNTER/ SEQUENCER
LSB
SYNC
38
40
32
SYSTEM CLOCK
36

Fig. 2

50a & 50b	12a & 12b	ADDRESS GROUP	ROM ADDRESS	FUNCTION
0 0	0 0	1	0 - 63	BULK ERASE
0 0	0 1	2	64 - 127	ERASE
0 0	1 0	3	128 - 191	WRITE
0 0	1 1	4	192 - 255	SUSTAIN
0 1	0 0	5	256 - 319	NOT USED
0 1	0 1	6	320 - 383	
0 1	1 0	7	384 - 447	
0 1	1 1	8	448 - 511	
1 0	0 0	9	512 - 575	
1 0	0 1	10	576 - 639	FIRST 20 μ SEC. OF DISTRIBUTED CONDITIONING
1 0	1 0	11	640 - 703	
1 0	1 1	12	704 - 767	
1 1	0 0	13	768 - 831	SECOND 20 μ SEC. OF DISTRIBUTED CONDITIONING
1 1	0 1	14	832 - 895	
1 1	1 0	15	896 - 959	
1 1	1 1	16	960 - 1023	

Fig. 2A

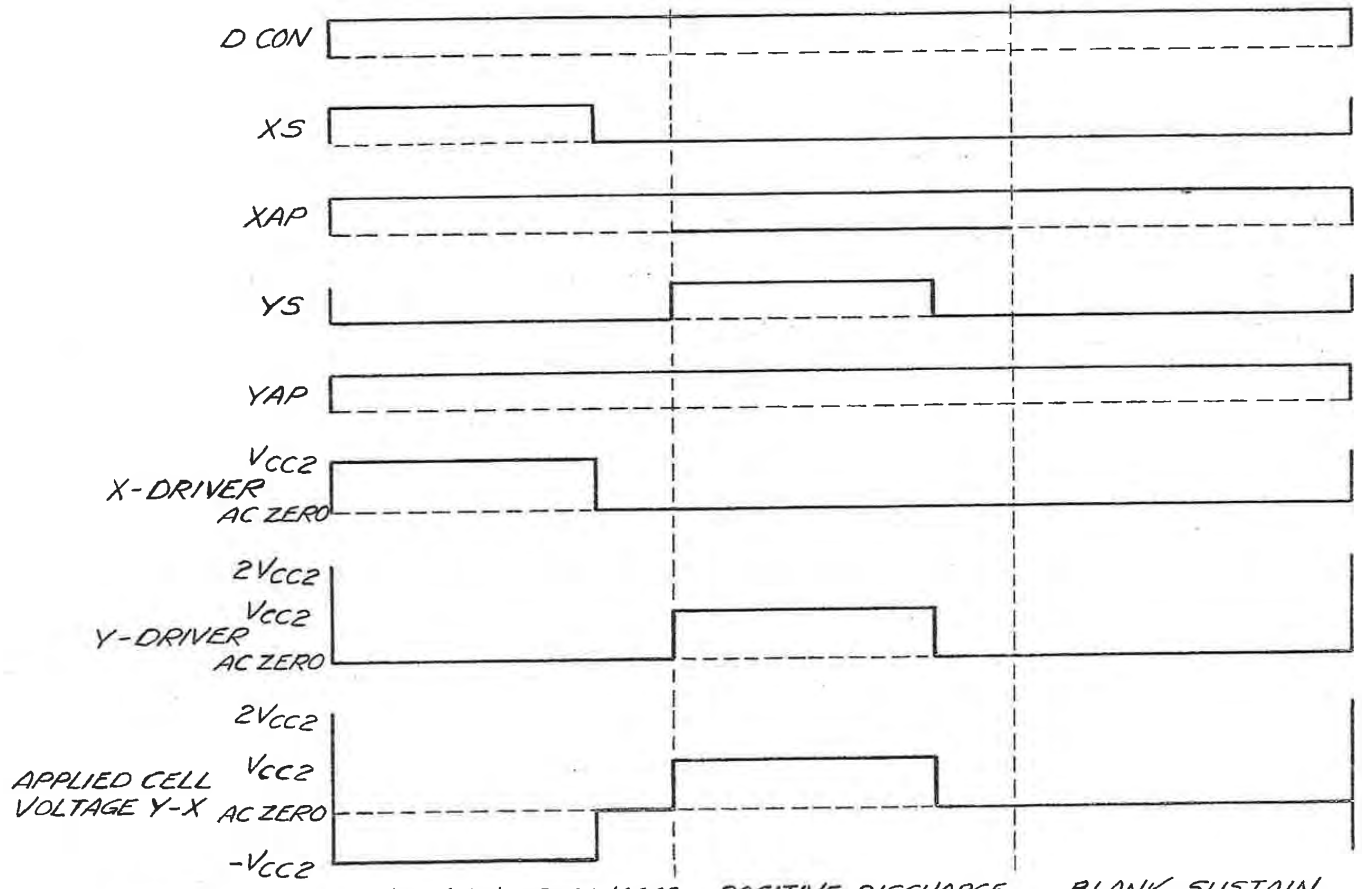
D CON
XS
XAP
YS
YAP
Vcc2
X-DRIVER
AC ZERO
2Vcc2
Vcc2
Y-DRIVER
AC ZERO
2Vcc2
Vcc2
APPLIED CELL VOLTAGE Y-X
AC ZERO
-Vcc2
NEGATIVE DISCHARGE
POSITIVE DISCHARGE
BLANK SUSTAIN

Fig. 3

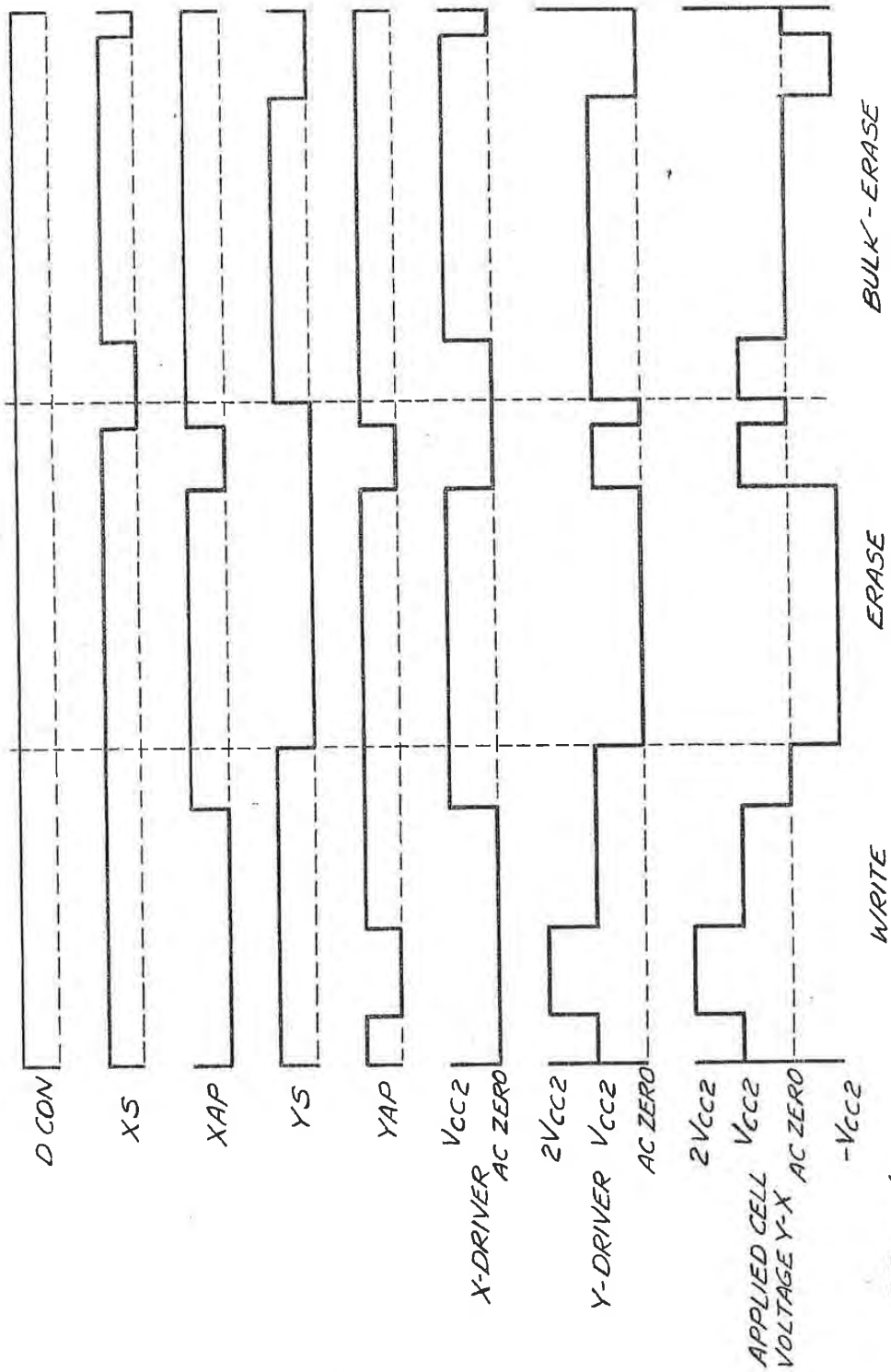
D CON
XS
XAP
YS
YAP
X-DRIVER
V_{CC2}
AC ZERO
Y-DRIVER
$2V_{CC2}$
V_{CC2}
AC ZERO
APPLIED CELL VOLTAGE Y-X
$2V_{CC2}$
V_{CC2}
AC ZERO
$-V_{CC2}$
WRITE
ERASE
BULK-ERASE

Fig. 4

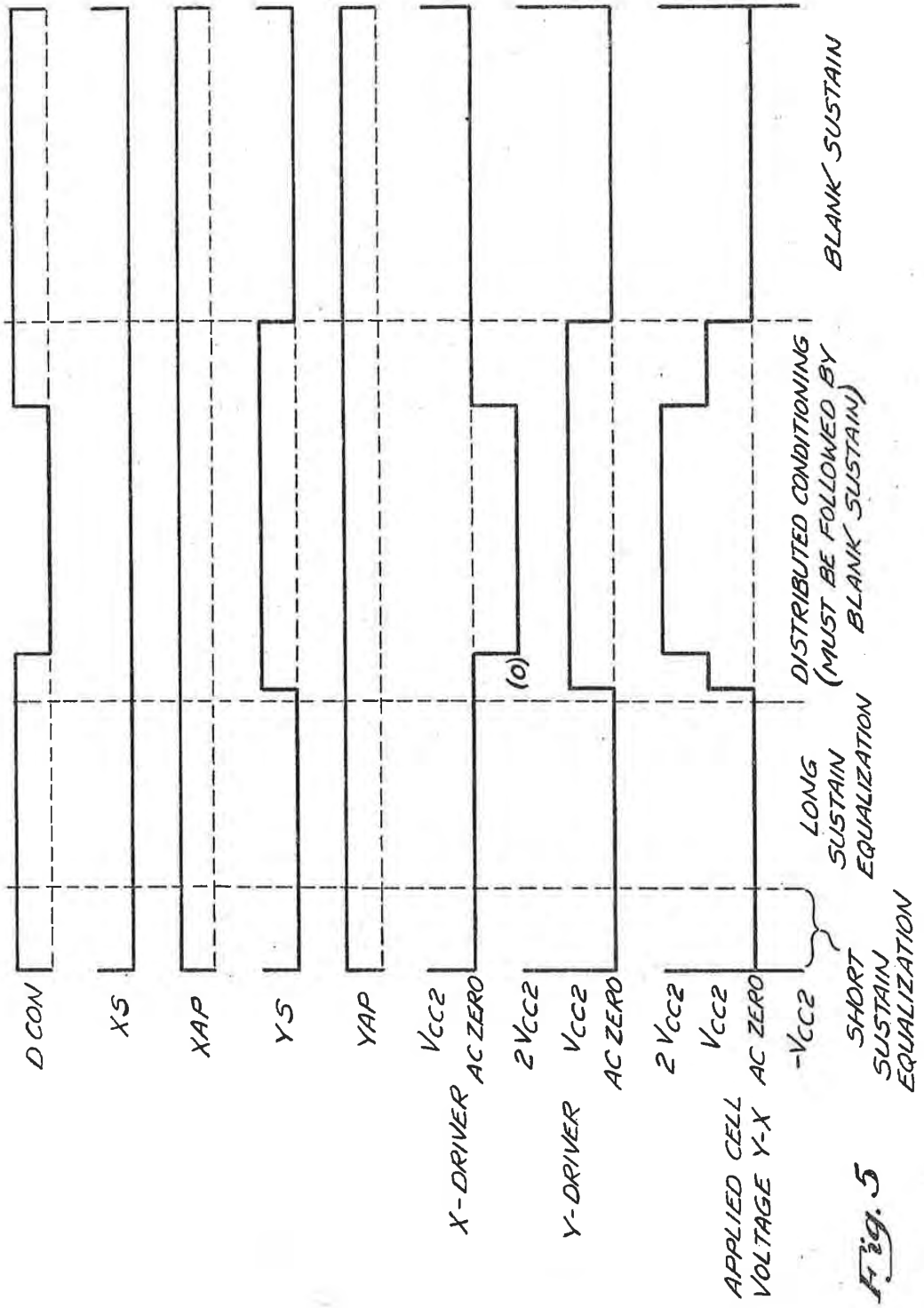
D CON
XS
XAP
YS
YAP
X-DRIVER
VCC2
AC ZERO
(0)
Y-DRIVER
2VCC2
VCC2
AC ZERO
APPLIED CELL VOLTAGE Y-X
2 VCC2
VCC2
AC ZERO
-VCC2
LONG SUSTAIN EQUALIZATION
SHORT SUSTAIN EQUALIZATION
DISTRIBUTED CONDITIONING (MUST BE FOLLOWED BY BLANK SUSTAIN)
BLANK SUSTAIN

Fig. 5

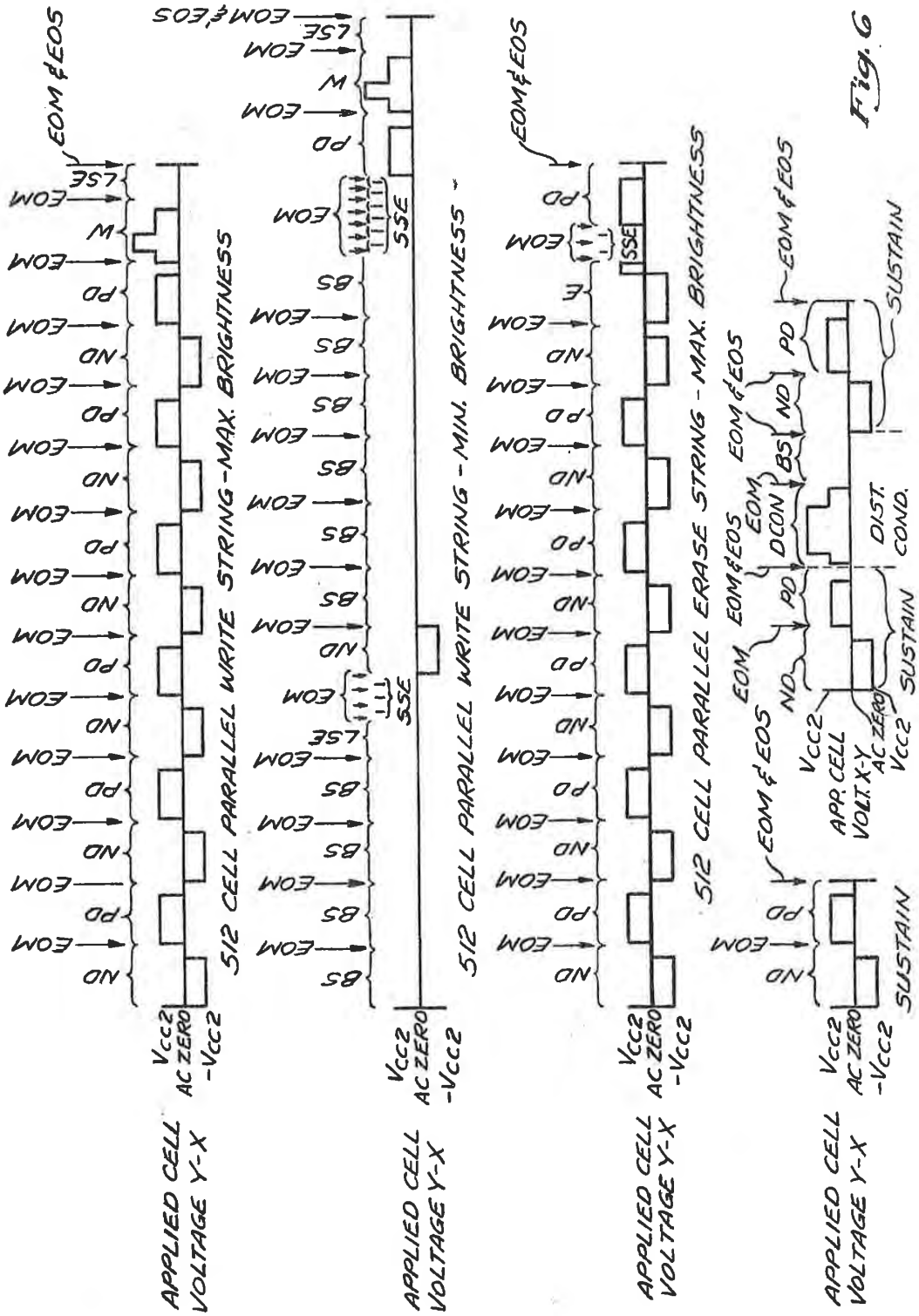
512 CELL PARALLEL WRITE STRING - MAX. BRIGHTNESS
512 CELL PARALLEL WRITE STRING - MIN. BRIGHTNESS
512 CELL PARALLEL ERASE STRING - MAX. BRIGHTNESS
APPLIED CELL VOLTAGE Y-X
EOM & EOS
LSE
W
PD
ND
BS
SSE
ISSE
E
DCON
DIST. COND.
SUSTAIN
APP. CELL VOLT. X-Y
AC ZERO
Vcc2
-Vcc2

Fig. 6

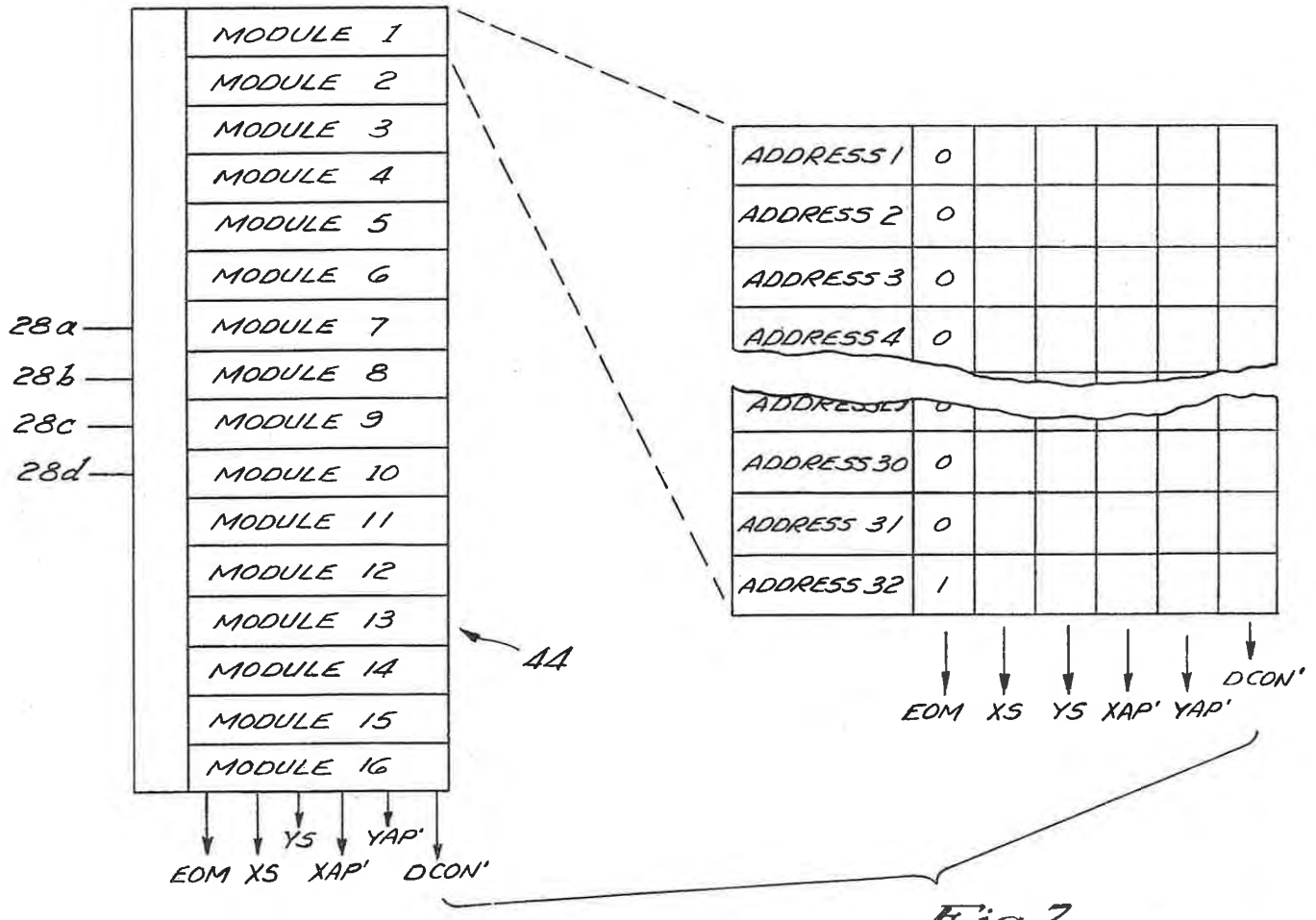
MODULE 1
MODULE 2
MODULE 3
MODULE 4
MODULE 5
MODULE 6
MODULE 7
MODULE 8
MODULE 9
MODULE 10
MODULE 11
MODULE 12
MODULE 13
MODULE 14
MODULE 15
MODULE 16
28a
28b
28c
28d
44
YS
YAP'
EOM XS XAP' DCON'
ADDRESS 1 0
ADDRESS 2 0
ADDRESS 3 0
ADDRESS 4 0
ADDRESS 30 0
ADDRESS 31 0
ADDRESS 32 1
EOM XS YS XAP' YAP' DCON'

Fig. 7

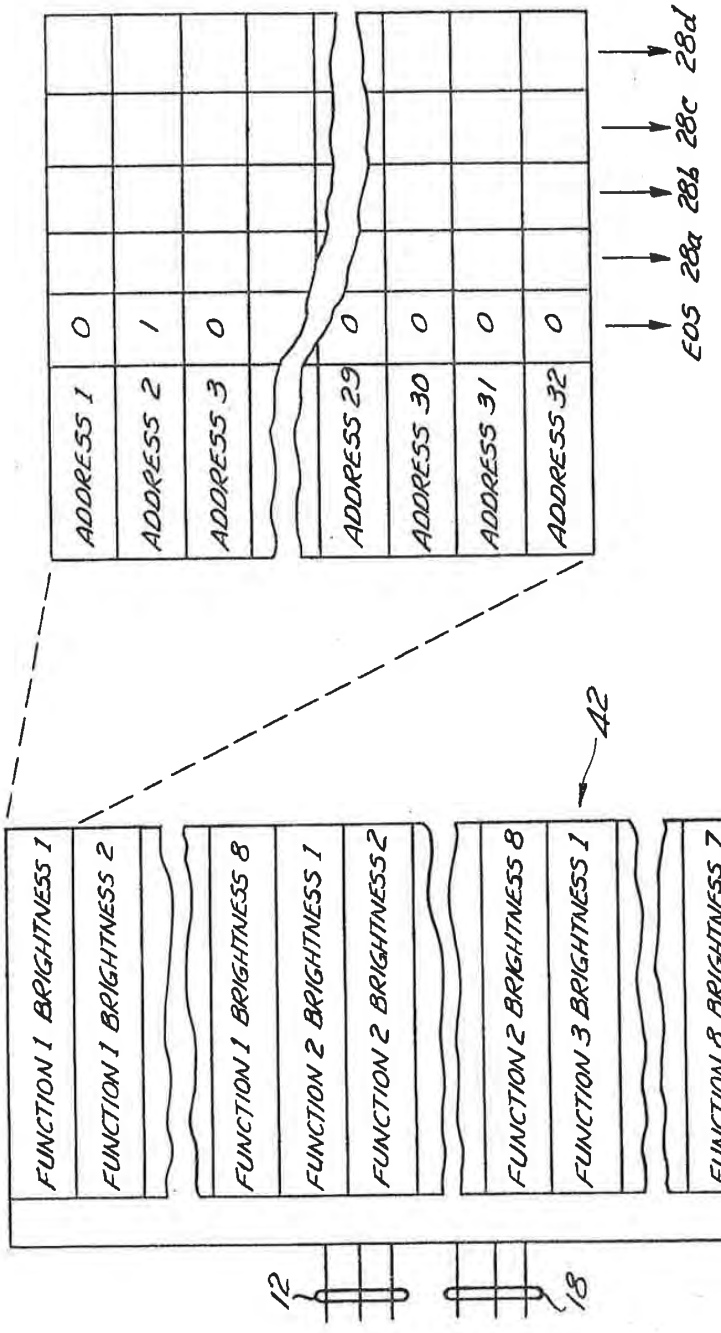
ADDRESS 1
ADDRESS 2
ADDRESS 3
ADDRESS 29
ADDRESS 30
ADDRESS 31
ADDRESS 32
0
1
0
0
0
0
0
EOS
28a
28b
28c
28d
42
FUNCTION 1 BRIGHTNESS 1
FUNCTION 1 BRIGHTNESS 2
FUNCTION 1 BRIGHTNESS 8
FUNCTION 2 BRIGHTNESS 1
FUNCTION 2 BRIGHTNESS 2
FUNCTION 2 BRIGHTNESS 8
FUNCTION 3 BRIGHTNESS 1
FUNCTION 8 BRIGHTNESS 7
FUNCTION 8 BRIGHTNESS 8
12
18

Fig. 8

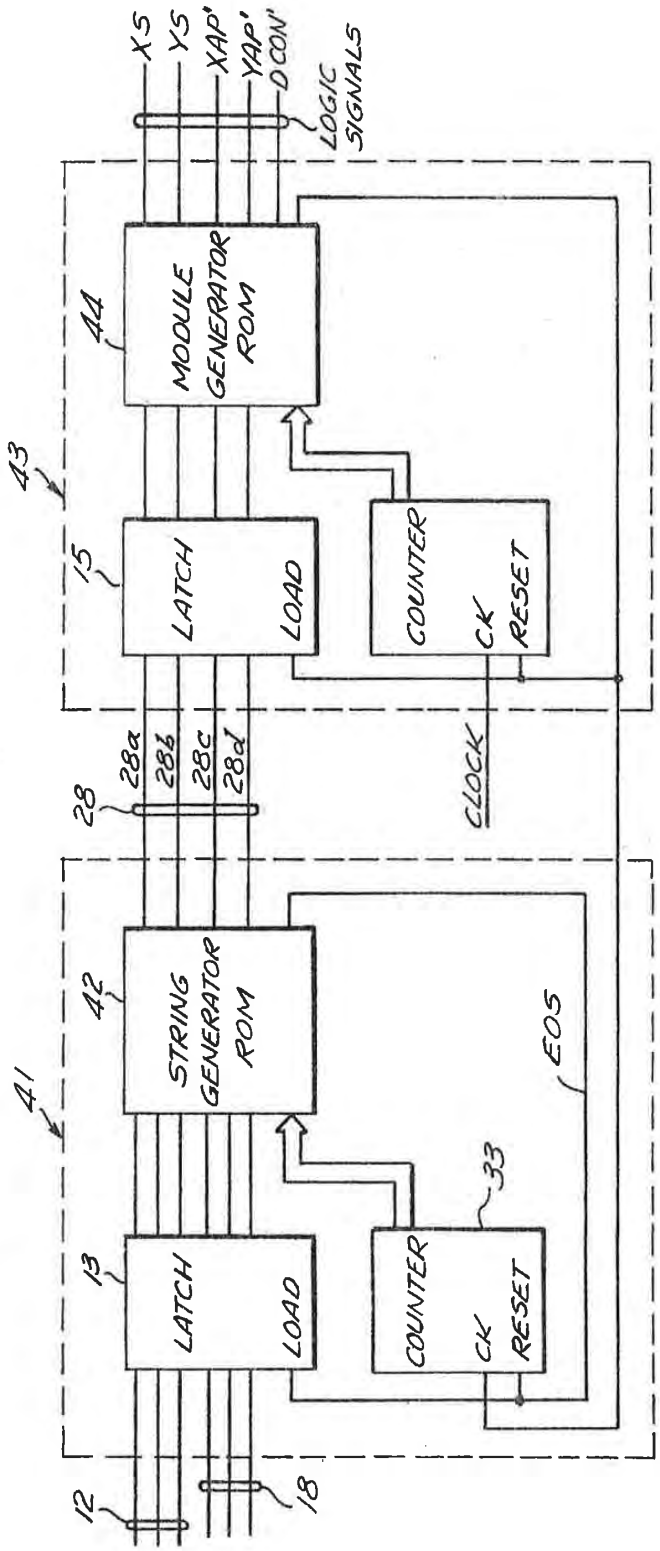
XS
YS
XAP'
YAP'
DCON'
LOGIC SIGNALS
44
MODULE GENERATOR ROM
43
15
LATCH
LOAD
COUNTER
CK
RESET
CLOCK
28
28a
28b
28c
28d
42
STRING GENERATOR ROM
41
EOS
33
13
LATCH
LOAD
COUNTER
CK
RESET
12
18

Fig. 9

MODULAR WAVEFORM GENERATOR FOR PLASMA DISPLAY PANELS

BACKGROUND OF THE INVENTION

Plasma display panels are presently in commercial use as digitally addressable information display devices. The panel itself typically consists of two glass plates with a gas mixture sealed between them. A plurality of X-axis electrodes extend in a mutually parallel array on an interior substrate of one plate, and a plurality of Y-axis electrodes extending in a mutually parallel array on the interior of the other plate. The X-axis electrodes are at a 90° angle to the Y-axis electrodes, thereby forming a plurality of intersections between the X-axis and Y-axis electrodes. A typical commercially available AC plasma panel has 512 X-axis electrodes and 512 Y-axis electrodes, yielding 262,144 intersections, or cells.

When a voltage of between 180 to 200 volts is applied across an X-axis electrode and a Y-axis electrode, a discharge in the gas occurs at the cell formed by the electrodes, causing a pulse of light to be emitted at this point. Simultaneously, a charge is collected on the cell wall, which results in the cell being an "on" cell. Once such a discharge has been produced and the cell is turned "on", the collected wall charge acts to continue the discharging when a lesser AC sustain voltage is applied between the electrodes. In an "on" cell, the gas will discharge and the cell will emit a pulse of light at each transition of the applied AC sustain waveform. The sustain voltage, however, is insufficient to initiate a discharge at an X-Y intersection. This phenomenon is known as inherent memory, and was originally disclosed by Baker et al, U.S. Pat. No. 3,499,167, and by Bitzer et al, in U.S. Pat. No. 3,959,190. By precisely timing, shaping, and phasing multiple alternating voltage waveforms supplied to X and Y axes electrodes, the generation, sustaining and erasure of light emitting gas discharges at selected locations on the plasma display panel can be controlled.

Four functions are used to control the operation of an AC plasma panel: the write function, the erase function, the sustain function, and the bulk-erase function. The write function causes a selected cell on the panel to change from the "off", or non-light emitting state, to the "on" or light emitting state. The sustain function maintains the state of all cells on the panel, i.e. causes "on" cells to remain on, and "off" cells to remain off. The sustain function also causes the "on" cells to emit light. The erase function causes a selected cell to be changed from the "on" state to the "off" state. The bulk-erase function causes all "on" cells in the panel simultaneously to be changed to the "off" state.

Operation of the write, erase, sustain, and bulk-erase functions is generally controlled by four logic signals: the X-sustain signal XS, the Y-sustain signal YS, the X-address pulse XAP, and the Y-address pulse YAP. These signals, generally supplied by a waveform ROM (Read Only Memory), are digital pulse trains typically recurring at a frequency of 50 kHz. The logic signals are supplied to the sustain and drive circuits, and cause the circuits to execute the four control functions on the panel. Since the typical operational frequency of the plasma display system is 50 kHz, the complex waveform for each of the four control functions is executed in a 20 microsecond period. It has been found necessary, in the prior art, to have all four functions of an equal length since one ROM is used to store them, and addressing is less complex for the constant length.

This 20 microsecond period is a compromise, since the amount of time needed for the various operations varies. For example, the amount of time needed for a sustain cycle is about 15 microseconds, for a write cycle about 23 microseconds, for an erase cycle about 16 microseconds, and for a bulk-erase cycle only about 8 microseconds. The typical 20 microsecond period is, therefore, a compromise for the four control functions. Increasing the period for each of the four functions to the 23 microseconds taken by the write function would increase the stability of the plasma display panel after a write function, but it would cause the system to be approximately 15% slower due to the longer period of time required to perform each function. The 20 microsecond period decreases the stability of the plasma display panel after a write function somewhat, an acceptable compromise.

A more significant problem is the fact that prior art systems bear the constraint of having a fixed time base, this fixed time base allowing only one fixed cycle length of 20 microseconds. If the lengths of the four control functions could differ, each of the functions could be done in the minimal time required, thus yielding both a higher data rate and a better write function.

It is also desirable to be able to add a new function which has a length greater than the fixed cycle length of 20 microseconds, such as the distributed conditioning pulse, which is the subject of copending U.S. patent application Ser. No. 273,093, filed on June 12, 1981, entitled: Distributed Conditioning For An AC Plasma Panel, by Joseph T. Suste and Michael J. Marentic. Since the distributed conditioning function takes more than 20 microseconds to perform, two 20 microsecond periods must be chained together to give a compound mode of length 40 microseconds. In order to perform the operation, extra logic for the ROM address lines is necessary to execute the two 20 microsecond component periods sequentially. It may be desirable to have other functions which also take a greater length than the standard 20 microsecond period. Therefore, it may be seen that the use of a fixed time base having a 20 microsecond period does not allow sufficient flexibility to operate sophisticated plasma display systems.

One possible solution is to increase the length of the period. This solution presents several problems of its own. First, the maximum update rate would be reduced by an amount directly proportional to the increase in the period of the cycle. Also, if only one sustain cycle is run in the increased period, the brightness of the display would be reduced, since only two pulses of light would be emitted from the display in the increased period.

Another major problem caused by the fixed 20 microsecond time base is that large scale parallel addressing is not possible. It is highly desirable to address an entire line, comprised of the 512 cells along an X-electrode, simultaneously. However, the time required to load the data necessary to address 512 cells is at least 71 microseconds to prepare the drive circuitry for a write or erase operation. Five complete sustain operations can be done in a period of 75 microseconds, providing sufficient time for loading data. A write function, done properly, takes 23 microseconds, so it may be seen that a period of approximately 98 microseconds or more is required in order to parallel address 512 cells. If a fixed period of 100 microseconds is adopted, 512 cell parallel addressing would be possible, but at a substantial cost.

Since the sustain and bulk-erase cycles would have the same period, to prevent complex addressing circuitry from being required, there would be a substantial delay in addressing, i.e. performing write or erase operations, if a sustain function was being executed at the time.

A major consideration in the design of plasma display panel systems is the amount of ROM memory storage space required, since larger amounts of memory increase both the cost and complexity of the system. The basic system described above, with only write, erase, sustain, and bulk-erase functions, at a fixed 20 microsecond period, needs only about 1K of memory.

If another function is to be added to the system, the amount of required memory is doubled. For a complex function, such as distributed conditioning, described in the above-referenced copending patent application, to be added to the system, the memory space in the ROM must be quadrupled, and external control logic must be added to access these new locations in the ROM.

If 512 cell parallel addressing is desired, the minimum period for a cycle that would allow 512 cell parallel addressing is about 100 microseconds. Each of the pulse trains stored in the ROM would have to be 100 microseconds long, 5 times the length of the basic system. Therefore, in order to add a 512 cell parallel addressing feature to the basic plasma panel system, the memory required would be 5 times the minimum memory of 1K, since the address groups are 5 times as long as the previous 20 microseconds, and thus 5K of memory would be required. If it is desired to parallel address 512 cell locations, and to also have a distributed conditioning feature, the memory capability must be further expanded.

Another desirable feature in a plasma panel is brightness control. The addition of brightness control expands the ROM by a factor equal to the number of brightness levels desired, typically 8. If brightness control is desired in a system with more than the basic four control functions, and 512 cell parallel addressing is also desired, the amount of memory required becomes prohibitively large, as demonstrated by the following example. For a system with 8 different control functions and 8 brightness levels, with a 120 microsecond period (required for 8 level brightness control), the amount of memory required is 384 address×8 modes×8 brightness levels×5 outputs (required for distributed conditioning)=120K. This size of memory is simply too expensive to be considered. Thus, if it is desired to have constant data rate brightness control in combination with sophisticated operating modes, an alternative system is required.

SUMMARY OF THE INVENTION

The present invention alleviates the above problems by forming the required waveforms as sequences of a small number of elemental waveform parts, called modules. Thus, the system generates short, elemental modules, and uses these modules as building blocks, stringing them together in different orders to provide a variety of waveforms to perform the required functions.

The modules used include a positive discharge module, a negative discharge module, a blank sustain module, a write module, an erase module, a bulk-erase module, a short sustain equilization module, a long sustain equilization module and a distributed conditioning module. In order to form a complete waveform which performs a function on the plasma panel, a number of modules are assembled into the complete function.

For example, to generate a sustain waveform, two modules are used. The first module is a negative discharge module, and the second module is a positive discharge module. In this way, the sustain function is assembled from two smaller modules so that the sustain operation will be performed in a minimum time.

A write function is generated by a positive discharge module and a write module. The positive discharge module is the same module used as the second module in the sustain function above. In addition, if the write function is immediately preceded by a sustain function, the initial positive discharge module, used in the write function, is not necessary. An erase function is generated by an erase module and a positive discharge module. A bulk-erase module is used to provide the complete bulk-erase function. Other functions, such as distributed conditioning brightness control, may be performed by the addition of a single extra module to perform each additional function.

512 cell parallel addressing can be done by forming a string of sustain pulses, for a period of time sufficient to enable addressing information to be loaded into the driver chips, and then by causing a write or erase module to be generated. Since it takes approximately 71 microseconds to load the data into the driver chips, five sustain modules of 15 microsecond duration would provide sufficient time for the information to be loaded. In order to complete the function, a write or erase module follows the sustain pulses, performing the write or erase function. The erase module must be followed by a sustain equilization module and then a positive discharge module, since each string of pulses must end with a positive charge pulse.

Because each function occurs in the minimum cycle time required, the addressing rate of the system is maximized. This permits 512 cell parallel addressing while, actually increasing the panel data update rate.

Modular waveforms are generated by using two ROMs that are cascaded. These ROMs include a module generator ROM, which operates at a fast access time, and a string generator ROM, which operates at a slow access time. The module generator ROM is capable of generating each of the modules described above. The string generator ROM indicates to the module generator ROM which modules it is to generate, and will cause the module generator ROM to generate a desired group of modules sequentially, forming a complete function.

By generating basic components of the waveform in modules, each individual component operation is executed in the minimum time required. This not only has the effect of improving the data rate of the system, but also provides an optimum write function which was not possible in the system operating with a fixed 20 microsecond period.

The memory required by a complex system not using modular waveform generation techniques would be prohibitively large. In order to have 8 levels of brightness control, 8 different control functions, 5 different outputs, and 512 cell parallel addressing, 120K of memory would be required. The module generator ROM of the present invention requires 2.5K of memory, and the string generator ROM requires 10K of memory, for a total requirement of 12.5K memory storage space.

In addition, the system of the present invention does not require complex external control logic, but requires only two counters and two latches in addition to the two ROMs.

The amount memory utilized has been minimized, thus keeping the overall cost of the system as low as possible. In addition, the system of the present invention calls for considerable flexibility, and is easily expandable for additional operational modes.

RELATED APPLICATIONS

This specification is one of a group of specifications on plasma display technology, all assigned to the present assignee, including: System For Driving AC Plasma Panel, Ser. No. 166,579, filed Jul. 7, 1980, by Joseph T. Suste; MOSFET Sustainer Circuit For An AC Plasma Display Panel, Ser. No. 258,757, filed Apr. 29, 1980, by Larry F. Weber; Constant Data Rate Brightness Control For An AC Plasma Panel, Ser. No.273,095, filed Jun. 12, 1981, by Joseph T. Suste; Distributed Conditioning For An AC Plasma Panel, Ser. No. 273,093, filed Jun. 12, 1981, by Michael J. Marentic and Joseph T. Suste; Plasma Display Panel Drive Electronics Improvement, Ser. No. 272,885, filed Jun. 12, 1981 by Michael J. Marentic; and Advanced Waveform Techniques For Plasma Display Panel, Ser. No. 273,094, filed Jun. 12, 1981, by Michael J. Marentic.

DESCRIPTION OF THE DRAWINGS

These and other advantages of the present invention are best understood through reference to the drawings, in which:

FIG. **1** is a block diagram of a conventional system with sustainer and driver circuitry controlling an AC plasma panel;

FIG. **2** is a block diagram of the conventional logic circuitry for providing the logic signal outputs which control the sustainer and driver circuitry of the system in FIG. **1**;

FIG. **2***a* is a chart showing the ROM addresses and the functions performed for a given mode control input for the logic circuitry of FIG. **2**;

FIG. **3** shows the applied cell voltage Y - X, the Y-driver voltage, the X-driver voltage, and the logic signal outputs supplied by the present invention for a positive discharge module, a negative discharge module, and a blank sustain module;

FIG. **4** shows the applied cell voltage Y - X, the Y-driver voltage, the X-driver voltage, and the logic signal outputs supplied by the present invention for a write module, an erase module, and a bulk-erase module;

FIG. **5** shows the applied cell voltage Y - X, the Y-driver voltage, the X-driver voltage, and the logic signal outputs supplied by the present invention for a short sustain equilization module, a long sustain equilization module, a distributed conditioning module, and the blank sustain module which must follow the distributed conditioning module;

FIG. **6** shows the assembled string for 512 cell parallel addressing write and erase functions, for the sustain function, and for the distributed conditioning function, the assembled strings being composed of the modules shown in FIGS. **3–5**;

FIG. 7 is a schematic diagram of a digital memory device storing 16 modules, each module having 32 addressable locations, for generating logic signal outputs causing one of the basic module operations shown in FIGS. **3–5** to be executed on a plasma panel;

FIG. **8** is a schematic diagram of a digital memory device having 64 address groups, each group having 32 addressable locations, for causing a selected group of modules from the device in FIG. **7** to be sequentially accessed; and

FIG. **9** is a block diagram schematic of the components of the present invention used to provide the logic signal outputs shown in FIGS. **3–5**.

DESCRIPTION OF THE PREFERRED EMBODIMENT

A plasma panel **70**, as shown in FIG. **1**, is driven by an X-axis driver circuit **250** and a Y-axis driver circuit **150**. The circuitry of FIG. **1** is described in detail in the above-identified copending application entitled "Distributed Conditioning For An AC Plasma Panel", which is incorporated herein by reference. A general description is provided below, to aid in the understanding of the present invention.

A pair of sustain circuits **210** and **110** are used to provide the sustain signal to the driver circuits **250** and **150**, respectively. Float circuits **211** and **111** are used to supply floating supply levels of V_{CC1}, the low voltage used to power the logic circuitry, and V_{CC2}, the high voltage used to drive the panel, to the circuits **250** and **150**, respectively. The X-axis sustain circuit **210** is controlled by an X-sustain signal XS, and the Y-axis sustain circuit is controlled by a Y-sustain signal YS. The addressing of individual cells of the panel **70**, to accomplish selective writing and erasing of these cells, is controlled by an X-address pulse XAP and a Y-address pulse YAP, supplied from a waveform ROM (Read Only Memory, not shown in FIG. **1**) through a pair of level shift circuits **240** and **140**, which are required, since the driver circuits **250** and **150** operate on floating grounds. The X-address information and Y-address information is supplied to the driver circuits **250** and **150** through a pair of level shift circuits **93** and **91**, respectively, and identifies which cells on the plasma panel **70** are to receive the X and Y address pulses.

FIG. **1** also shows a distributed conditioning signal DCON supplied to the X-axis driver circuit **250** via a level shift circuit **200**. The distributed conditioning operation is described in the above-identified copending application, "Distributed Conditioning For An AC Plasma Display Panel."

A waveform ROM **40** and its addressing circuitry are shown in FIG. **2**. A distributed conditioning input **50** and a mode control input **12** determine which of **16** address groups in the waveform ROM **40** will be accessed. The distributed conditioning input **50** is generated by a distributed conditioning circuit **52** and comprises **2** address bits, **50***a* and **50***b*, supplied to the waveform ROM **40**. These two bits form the most significant address bits for the ROM **40**, and determine whether the address group which is to be accessed is in address groups **1** through **4**, **5** through **8**, **9** through **12**, or **13** through **16**, as shown by the chart in FIG. **2***a*. The two next most significant address bits for the waveform ROM **40** are bits **12***a* and **12***b*, which are generated by a function logic circuit **11**. These bits **12***a* and **12***b* determine which of the four basic functions (bulk-erase, erase, write, or sustain) will be implemented, as shown in FIG. **2***a*.

It may be seen from the chart in FIG. **2***a* that each of the address groups have 64 addressable data words, as shown in the column marked "ROM Address." Sequencing through these 64 addresses is controlled by timing information **38**, supplied by a system counter/sequencer **34**, and a system clock **32**, shown in FIG. **2**. The chart in FIG. **2***a* shows, under the heading "Func-

tion", the operations that will be performed for each of the 16 address groups.

The waveform ROM **40** supplies the 5 logic signal outputs controlling the sustainer and driver circuitry of FIG. **1**: an X-sustain signal XS, a Y-sustain signal YS, an inverse X-address pulse XAP', an inverse Y-address pulse YAP', and an inverse distributed conditioning pulse DCON'. The latter three pulses are in inverse form since the level shifters used in the circuitry of FIG. **1** will invert them. The level shifters of FIG. **1**, **240**, **140**, and **200**, are well-known, and may comprise, for example, optical isolators or transformers. The single ROM system described above is designed to operate at a fixed frequency, typically 50 kHz. This type of system has all of the drawbacks and disadvantages described above.

The present invention uses a modular waveform generation circuit in place of the circuitry of FIG. **2**. The invention separates each of the waveforms used to address the plasma panel into modules. By combining these modules in different sequences, any desired waveform may be generated. Each module begins and ends with no discharge activity taking place, and the applied cell voltage Y - X is at the AC zero voltage level at the beginning and end of each module. This requirement enables any module to follow any other module.

The modules used by the present invention to generate waveforms to address the plasma panel, are shown in FIGS. **3–5**. The logic signals shown in these figures (DCON, XS, XAP, YS, AND YAP) are supplied to the sustain and driver circuits **110,210,150,250** shown in FIG. **1** which, in response, generate the waveforms X-driver, Y-driver shown in FIGS. **3–5**. These waveforms cooperate to generate, at the plasma panel **70**, the applied cell voltage Y - X, which performs the functions indicated.

The first module in FIG. **3** is a negative discharge module. The second module is a positive discharge module. A negative discharge module and a positive discharge module are the two components required to perform the sustain function. When a negative discharge module is followed by a positive discharge module, a single sustain cycle is generated. The negative discharge module and the positive discharge module are also used as components of other functions, when combined with other modules.

The third module shown in FIG. **3** is the blank sustain module, which is used for brightness control. Since the brightness control concept for use with the modular waveform generator of the present invention has a different inventor, it is discussed in the above-referenced copending application entitled, "Advanced Waveform Techniques For Plasma Display Panels."

The first module in FIG. **4** is a write module. When the write module is preceded by a positive discharge module (FIG. **3**), a complete write function will be performed. If a sustain function immediately precedes the write function, the positive discharge module is not necessary, since a sustain function ends with a positive discharge module.

The second module in FIG. **4** is an erase module, and when followed by a positive discharge module, a complete erase function will be performed. The positive pulse of the positive discharge module is necessary, following the erase module, because each string of modules comprising a function must end with a module producing a positive pulse so that the first pulse of a succeeding sustain function will produce a discharge of light. A positive pulse is produced by positive discharge, write, and distributed conditioning modules.

The final module shown in FIG. **4** is the bulk-erase module. This module alone will perform the bulk-erase function. Since it is comprised of two very short pulses, which pulses erase the entire display, a succeeding sustain function will not produce a pulse of light in any case. Thus, it is not necessary to follow the bulk-erase module with a positive pulse producing module; therefore, the bulk-erase module is an exception to the requirement of ending a function with a positive pulse producing module.

In FIG. **5**, the first two modules shown are a short sustain equilization module and a long sustain equilization module. These two modules are characterized by an applied cell voltage Y - X at the AC zero voltage level, and are used for spacing purposes. These spaces are required when it is necessary to have a string of modules in a certain time period, and are most commonly used for brightness control systems which are capable of addressing 512 cells, as will be described later.

The third module shown in FIG. **5** is a distributed conditioning module. The distributed conditioning function eliminates the need for border sustainers by periodically discharging all of the cells in the panel, and is discussed in the above-referenced copending application, "Distributed Conditioning For An AC Plasma Display Panel." In order to perform a distributed conditioning operation, the distributed conditioning module must be followed by a blank sustain module, as shown in FIG. **5**. The distributed conditioning module must be preceded by a positive discharge module, but this positive discharge module may be the last module of the preceding operation.

While only 9 modules have been disclosed, the system of the present invention has the capability of storing 16 different modules. When any one of these modules is accessed, the system must output the 5 logic signals (XS, YS, XAP', YAP', and DCON') which will cause the waveform generated by that module to be executed on the plasma display panel. FIG. **7** shows, schematically, a module generator ROM **44** storing information to perform 16 different modules. Module **1** is shown to have 32 address locations, and the operation performed by module **1** will be executed by stepping through these locations, in order, to produce binary bit patterns which define the logic signal outputs. An additional signal generated by each of the modules is the "end of module" signal EOM. This signal is necessary, since different modules require different time periods.

For example, in order to produce a short sustain equilization module, only 7 of these address locations are utilized. However, in order to perform the longer distributed conditioning function, all 32 of the address locations are needed. Since each module will be performed in the minimum amount of time required, the end of module signal EOM, is necessary to indicate that the module is completed. Therefore, the EOM bit for all but the last address location utilized will have a 0 logic level. For the last address location utilized, the EOM bit will be 1, indicating that the operation performed by the module is complete.

Since there are 16 different modules, four address bits **28***a*, **28***b*, **28***c* and **28***d* are required to select one of the 16 modules. These address bits **28***a*, **28***b*, **28***c*, and **28***d*, are provided by a string generator ROM **42**, shown schematically in FIG. **8**. The string generator ROM **42** se-

quentially addresses groups of modules from the module generator ROM **44** to assemble a string of modules into a complex waveform. The string generator ROM **42** is shown to provide 8 functions, each at 8 brightness levels, requiring a total of 64 address groups. Each of these address groups contains 32 address locations, each identifying a module. Thus, each string may include up to 32 modules. In other words, each of the addressable locations stores address bits **28***a*, **28***b*, **28***c*, and **28***d* which identify 1 module, and cause that module to be executed.

There is an additional logic signal output, the "end of string" signal EOS. When the EOS signal is at a logic level of 1, it indicates that the last module, in the string is being generated. For example, if a sustain function is being generated, a negative discharge module and a positive discharge module must be produced. Since there are only two modules in the basic sustain function, addressable location 2 would have a 1 bit for the EOS logic signal.

Referring now to FIG. **6**, a number of examples will be utilized to describe the use of modules to assemble functional strings. In a first example, a distributed conditioning function, assembled from a distributed condition module (DCON) and a blank sustain module (BS), is shown preceded by a sustain function. The sustain function is assembled from a negative discharge module (ND) and a positive discharge module (PD). Since the last module of the sustain function is a positive discharge module, the distributed conditioning function may follow the sustain function without requiring an additional positive discharge module.

The blank sustain module (BS) following the distributed conditioning module (DCON), and completing the distributed conditioning function, generally is followed by a negative discharge module (ND), as shown in FIG. **6**, where the negative discharge module (ND) following the distributed conditioning function is the first module of a sustain function. It should be noted, however, that it is only typical, and not mandatory, that a negative discharge module (ND) follows the distributed conditioning function.

A second example provided by FIG. **6** is the sustain function. A negative discharge module (ND) will be generated, and at the last point in that module, an "end of module" signal EOM will be generated. As can be seen from FIG. **6**, each module ends with an EOM signal, which causes the system to access the next module from the ROM **44**. In the case of the sustain function being described, this next module is a positive discharge module (PD). When the positive discharge module has been generated, an "end of module" signal EOM and an "end of string" signal EOS are generated. As can be seen from FIG. **6**, each function ends with an EOS signal, which causes the next function to be accessed from the string ROM **42**. By using this technique, the basic functions may be executed in the minimum amount of time required.

In order to perform a 512 cell parallel addressing operation, a period of at least 71 microseconds is required for loading addressing data into the driver circuits. Therefore, if a write or erase function is to be performed, a string of modules will be assembled as shown in the remaining examples of FIG. **6**. For a period of at least the 71 microseconds required to load the data, sustain functions composed of positive discharge (PD) and negative discharge (ND) modules will be assembled. After a time sufficient to load the data, a write (W) or erase (E) module is accessed. 512 cell parallel write strings are shown in FIG. **6** for both maximum and minimum brightness. For maximum brightness, there are 6 complete sustain functions followed by a write module (W) and a long sustain equilization module (LSE). During the time that the sustain functions are being executed, data is being loaded into the driver circuits. Then, near the end of the string, the 512 cell parallel write module (W) is accessed.

For a minimum brightness level string performing the 512 cell write operation, most of the negative discharge (ND) modules and positive discharge (PD) modules are removed, substituting blank sustain (BS), long sustain equilization (LSE), and short sustain equilization (SSE) modules. It can be seen that one complete sustain function will be performed before the write module (W) is accessed. In addition, the cycle shown for minimum brightness is extended to 120 microseconds, rather than the 100 microseconds of the maximum brightness string. Making the string longer with the same number of light emissions, of course, has the effect of further reducing the overall light emitted from the plasma display panel **70**.

FIG. **6** also shows a 512 cell parallel erase string, for maximum brightness. There are 5 complete sustain functions, followed by a negative discharge module (ND), and the erase module (E). There are then two short sustain equilization modules (SSE), and a positive discharge module (PD) to end the string with a positive pulse. The requirement for this positive pulse was discussed above.

The total time for a write or erase operation is approximately 102 microseconds. In this time period, 512 cells may be written. With non-module systems, **16** cells could be written in a period of 20 microseconds. Therefore, it may be seen that this system performs a write or erase function approximately 6.4 times faster than such systems. Even when the system is operating at the minimum brightness level shown in FIG. **6**, and the write or erase function takes 120 microseconds to be performed, the system of the present invention is approximately 5.3 times faster than non-module systems. Therefore, the overall data rate of the system of the present invention is at least 5.3 times higher than the data rate systems which do not include the present invention.

The actual circuitry used to form the modules and to assemble the strings of modules is shown in FIG. **9**. This circuit is used in place of the more common waveform ROM **40** shown in FIG. **2**. There are two main components to the system: a string generator **41**, and a module generator **43**. The module generator **43** includes, as a component, the module generator ROM **44** shown in FIG. **7**, and generates the individual modules described above. The string generator **41** includes, as a component, the string generator ROM **42** shown in FIG. **8**, and assembles the modules in a desired string to perform whatever function is to be executed.

The operation of the module generator **43** is as follows. Module address information **28** (bits **28***a–d*) is supplied by the string generator **41**, and defines which module is to be generated. This information is supplied via a latch **15** to the module generator ROM **44** when the previous module has been completed. The module generator ROM **44** will then output logic signals (XS, YS, XAP′, YAP′, DCON′) which will cause the driver and sustainer circuitry (FIG. **1**) to execute the desired module. The module generator ROM **44** is clocked

through its addressable locations by timing information from a counter 35.

When a module has been completed, an end of module signal EOM will be output from the module generator ROM 44 as described above. This signal is supplied to the counter 35, causing it to reset. The EOM signal is also supplied to the latch 15, causing it to clock an address into the module generator ROM 44 defining the next module to be accessed in the string. Since the counter 35 has been reset, information from the next module will be accessed beginning at the first addressable location in that module.

These modules are assembled into strings by the string generator 41. When a module has been generated and the End of Module signal EOM is supplied by the module generator ROM 44, the EOM signal is used as a clocking pulse for a counter 33. Each time the counter 33 receives this End of Module signal EOM, it will increment and cause the string generator ROM 42 to output address information 28 defining the next module to be executed. If the address information 28 defines the last module in the string, an End of String signal EOS is generated by the string generator ROM 42. This End of String signal EOS causes the counter 33 to reset, and the latch 13 to provide to the string generator ROM 42 an address defining the next string which is to be performed.

This address comprises the two inputs to the system: a brightness control input 12, and a mode control input 18. The module generation system shown in FIG. 9, to provide 512 cell parallel addressing with brightness control as described above, would require a string generator ROM memory of 10K, and a module generator ROM of 2.5K, for a total memory requirement of 12.5K. The use of a non-modular system with such capability would require 120K of memory. It can be seen that, as more functions are added, and more brightness levels are used, the memory savings will be multiplied.

The modular waveform generator system described in this specification may also be used to perform a distributed conditioning function, as shown by the distributed conditioning string in FIG. 6. Since the distributed conditioning concept has a different inventor, that concept is covered in a copending application. The module waveform generator technique can also be used to implement an improved brightness control system, but since the concept of the improved brightness control system also has a different inventor, that concept is also covered in a copending application.

The module waveform generator technique has provided a means by which to vary the time base to optimize each function being performed. In this way, the data rate of the system is increased and the performance of each of the functions has been optimized.

Thus, the system is capable of parallel addressing 512 cells, and by doing so, the data rate of the system is increased by more than 5.3 times. In addition, the modular waveform generator system is easily expandable for additional operating functions.

The amount of memory used has been minimized. The modular waveform generator system described in the preferred embodiment uses less than 1/9th the memory of non-modular systems, and it does not need nearly as sophisticated an addressing system.

I claim:

1. An AC plasma panel system, comprising:
a plasma panel driver circuit; and
means for providing input waveforms for said driver circuit, said means comprising:
means for providing waveforms of different arbitrary lengths, each of said waveforms of different arbitrary lengths for accomplishing a different function on said panel, wherein one of said functions is a write function and another of said functions is a sustain function.

2. An AC plasma panel system as defined in claim 1 wherein said means for providing waveforms of different arbitrary lengths comprises:
first and second memories, said first memory addressing said second memory.

3. An AC plasma panel system as defined in claim 2 wherein said second memory stores data defining elemental waveform components and wherein said first memory stores data defining combinations of elemental waveform components for providing said waveforms of different arbitary lengths.

4. An AC plasma panel system as defined in claim 3 wherein two of said combinations of elemental waveform components include identical elemental waveform components.

5. An AC plasma panel system as defined in claim 1 wherein said waveforms of different arbitrary lengths accomplish a write function on said AC plasma panel in a time period greater than 20 microseconds and a sustained function on said AC plasma panel system in a period shorter than 20 microseconds.

6. An AC plasma panel system as defined in claim 1 wherein said different functions comprise a write, erase, sustain and bulk-erase function.

7. An AC plasma panel system as defined in claim 6 wherein said different functions additionally comprise a distributed conditioning function.

8. An AC plasma panel system as defined in claim 7 wherein said different functions additionally comprise a variable brightness function.

9. A method of generating complex waveforms for an AC plasma panel, comprising:
storing data defining partial waveforms for writing and sustaining said panel; and
accessing said data in a predetermined sequential order to define a waveform comprising plural ones of said partial waveforms.

10. A method of generating complex waveforms as defined in claim 9 wherein said partial waveforms include a positive discharge, negative discharge, write, erase and bulk-erase partial waveform.

11. A method of generating complex waveforms as defined in claim 9 additionally comprising:
generating a clocking signal at the completion of accessing of said data defining partial waveforms.

12. A method of generating complex waveforms as defined in claim 9 additionally comprising:
generating a clocking signal upon completion of accessing of said data in a predetermined order to indicate the completion of a waveform.

13. A method of generating complex waveforms as defined in claim 9 wherein said accessing step permits accessing of plural waveforms to permit the brightness of said AC plasma panel to be varied.

14. A method of generating complex waveforms as defined in claim 9 wherein said accessing step accesses said data in a pair of predetermined orders, said predetermined orders having different lengths.

15. A plasma panel waveform generator comprising:

a first memory storing elemental waveform components; and

a second memory storing instructions for assembling said components in plural sequential orders into waveform strings.

16. A plasma panel waveform generator as defined in claim 15 in which said second memory addresses said first memory.

17. A plasma panel waveform generator as defined in claim 15 in which said elemental waveform components stored within said first memory have different lengths.

18. A plasma panel waveform generator as defined in claim 15 wherein said waveform strings include a variable number of said elemental waveform components.

19. A plasma panel waveform generator as defined in claim 15 wherein said first and second memories comprise read-only-memories.

20. A plasma panel waveform generator as defined in claim 15 wherein said first memory stores data defining an end to said elemental waveform components.

21. A plasma panel waveform generator as defined in claim 20 wherein said data defining an end of said elemental waveform components accesses data from said second memory.

22. A plasma panel waveform generator as defined in claim 15 wherein said second memory stores data defining the end of said waveform strings.

23. A plasma panel waveform generator as defined in claim 22 wherein said data defining the end of said waveform strings enables addressing of said second memory.

24. A modular waveform generator for a plasma panel, comprising:

first means for generating partial waveforms for operating said plasma panel; and

second means for assembling said partial waveforms generated by said first means in plural sequential orders into strings to perform functions on said panel.

25. A modular waveform generator for a plasma panel as defined in claim 24 wherein said functions include write, erase and sustain functions for said plasma panel.

26. A modular waveform generator for a plasma panel as defined in claim 25 wherein said operations include common elements of said write, erase and sustain functions.

27. A modular waveform generator for a plasma panel as defined in claim 24 wherein said first and second means comprise read-only-memories.

28. An AC plasma panel waveform generator comprising:

means for providing a write and an erase waveform having a duration in excess of 71 microseconds; and

means for providing a sustain waveform having a duration less than 20 microseconds.

29. A method of providing logic signals for controlling a plasma panel, comprising:

generating basic waveform components common to more than one function; and

assembling at least two of said basic waveform components into a string to perform a function on said plasma panel.

30. A method of addressing an AC plasma panel, comprising:

writing new displays onto said panel during a data loading and writing period having a first duration; and

periodically permitting initiation of said writing step at intervals shorter than said first duration.

31. A method of addressing an AC plasma panel as defined in claim 30 wherein said first duration is longer than 71 microseconds.

32. A method of addressing an AC plasma panel as defined in claim 30 wherein said second duration is shorter than 20 microseconds.

33. An AC plasma panel waveform generator, comprising:

means for driving electrodes in said panel in response to partial input waveforms assembled in sequential series; and

means for generating, as said input waveforms, a write and a sustained waveform, each having a different duration, which duration is the minimum duration required to adequately perform its function.

* * * * *

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(54) **METHOD AND APPARATUS FOR DRIVING LIQUID CRYSTAL DISPLAY**

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(30) **Foreign Application Priority Data**

Sep. 4, 2001 (KR) P2001-54127

Publication Classification

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(52) **U.S. Cl.** **345/87**

(57) **ABSTRACT**

The present invention discloses a method and apparatus for driving a liquid crystal display device suitable for enhancing a picture quality. More specifically, in the method and apparatus, source data is modulated based on registered data that is previously provided therein. The modulated data is applied to a liquid crystal panel at the initial period of one frame period. A data different from the modulated data is supplied to the liquid crystal panel at the later period of the frame period.

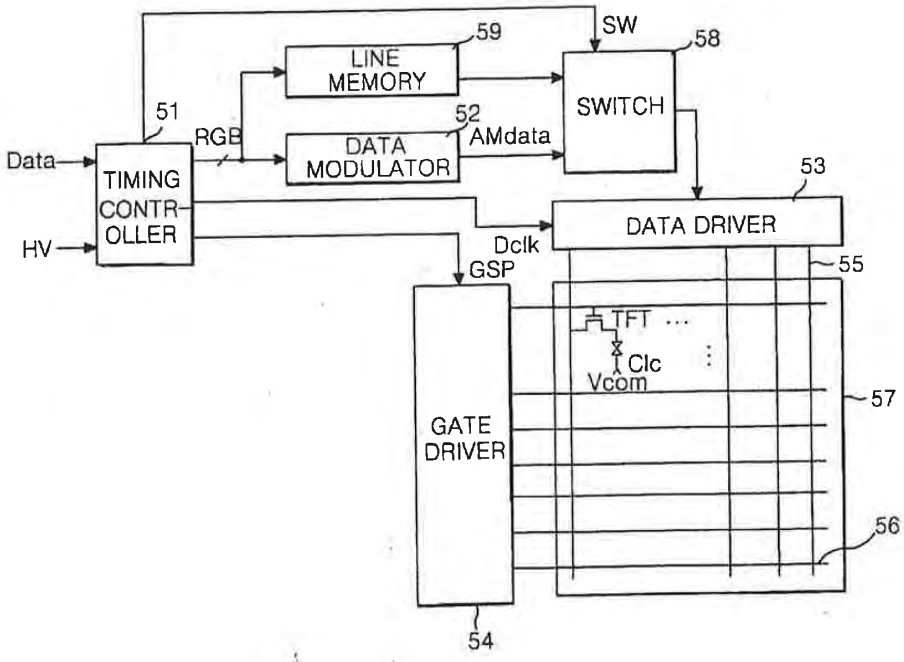


FIG. 1
CONVENTIONAL ART

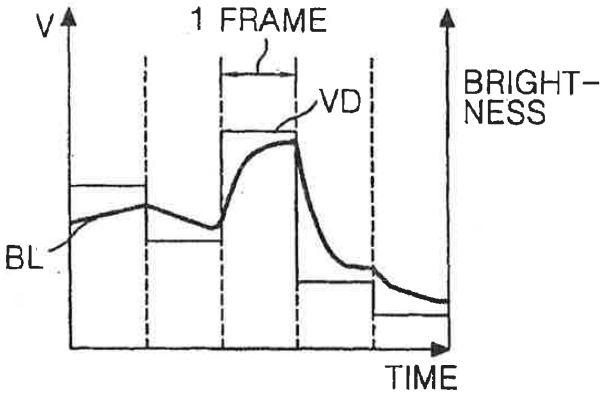


FIG. 2
CONVENTIONAL ART

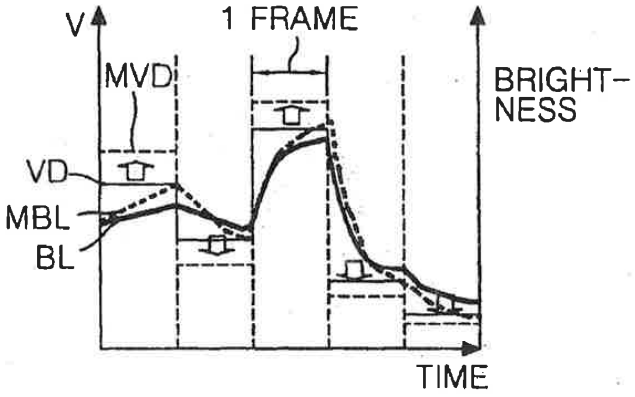


FIG.3
CONVENTIONAL ART

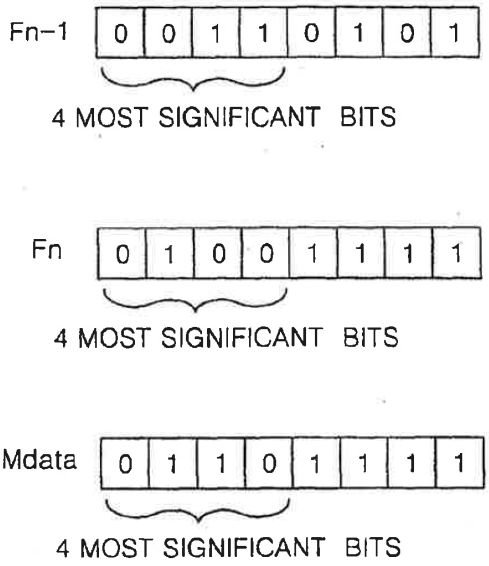
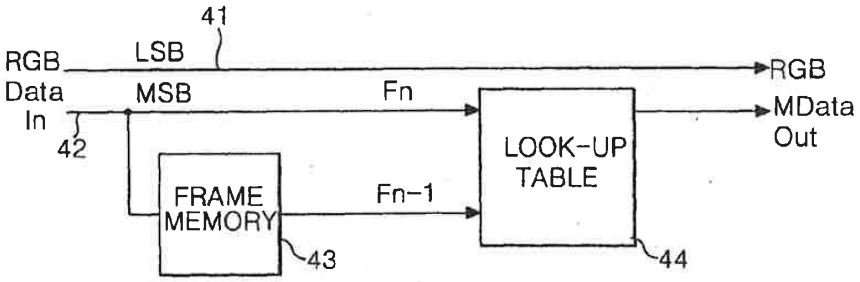


FIG.4
CONVENTIONAL ART



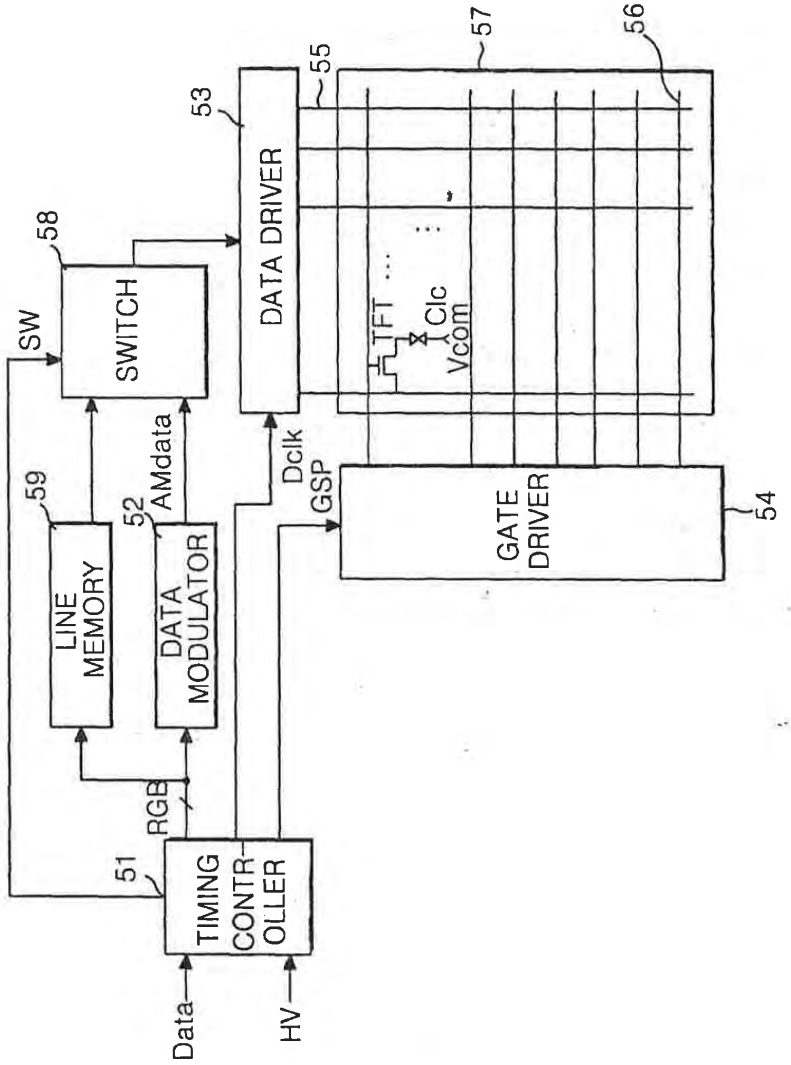


FIG.5

FIG.6

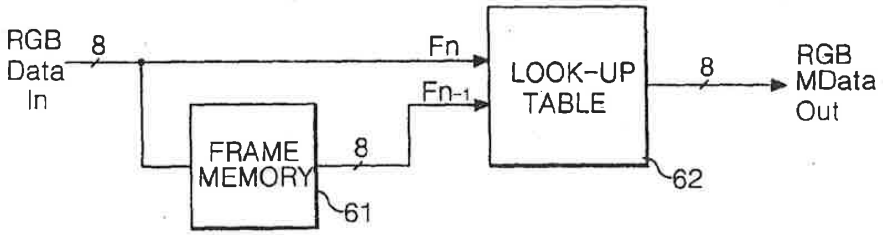

RGB
Data
In
8
Fn
Fn-1
LOOK-UP
TABLE
8
RGB
MData
Out
FRAME
MEMORY
8
61
62

FIG.7A

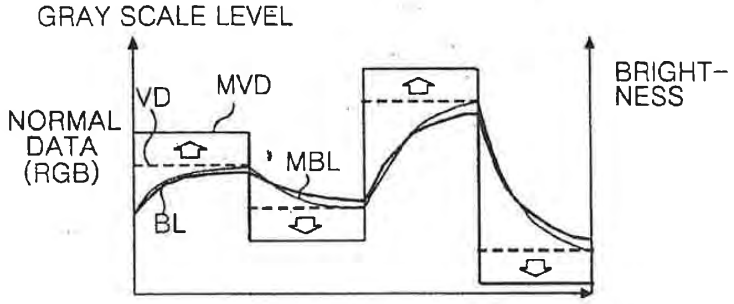


FIG.7B

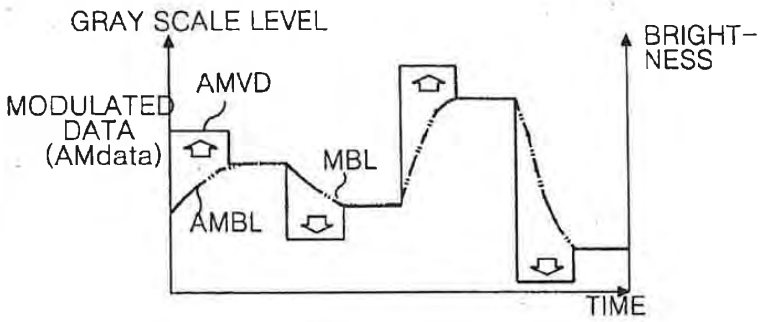
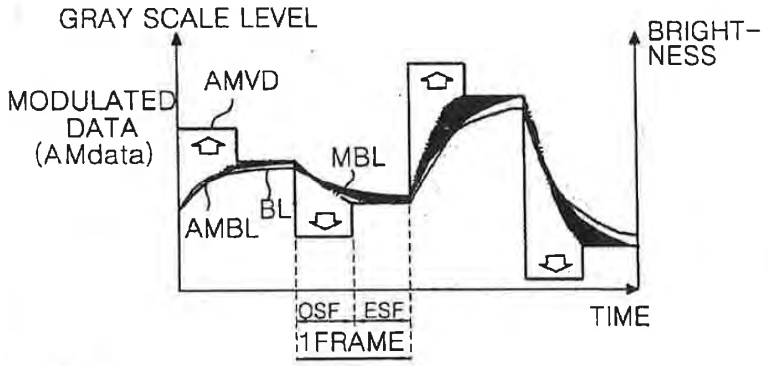


FIG.7C



VARIATION OF BRIGHTNESS BETWEEN MODULATION SYSTEMS OF THE PRESENT INVENTION AND CONVENTIONAL HIGH-SPEED DRIVING SYSTEM

METHOD AND APPARATUS FOR DRIVING LIQUID CRYSTAL DISPLAY

[0001] This application claims the benefit of Korean Application No. P2001-54127 filed on Sep. 4, 2001, which is hereby incorporated by reference.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to a liquid crystal display, and more particularly, to a method and apparatus for driving a liquid crystal display. Although the present invention is suitable for a wide scope of applications, it is particularly suitable for enhancing a picture quality.

[0004] 2. Discussion of the Related Art

[0005] Generally, a liquid crystal display (LCD) controls a light transmittance of each liquid crystal cell in accordance with a video signal, thereby displaying a picture. An active matrix LCD including a switching device for each liquid crystal cell is suitable for displaying a dynamic image. The active matrix LCD uses a thin film transistor (TFT) as a switching device.

[0006] The LCD has a disadvantage in that it has a slow response time due to inherent characteristics of a liquid crystal, such as a viscosity and an elasticity, etc. Such characteristics can be explained by using the following equations (1) and (2):

$$\tau_r \propto \gamma d^2/\Delta\epsilon|V_a^2-V_F^2| \quad (1)$$

[0007] where τ_r represents a rising time when a voltage is applied to a liquid crystal, V_a is an applied voltage, V_F represents a Freederick transition voltage at which liquid crystal molecules begin to perform an inclined motion, d is a cell gap of the liquid crystal cells, and γ represents a rotational viscosity of the liquid crystal molecules.

$$\tau_f = \gamma d^2/K \quad (2)$$

[0008] where τ_f represents a falling time at which a liquid crystal is returned into the initial position by an elastic restoring force after a voltage applied to the liquid crystal was turned off, and K is an elastic constant.

[0009] A twisted nematic (TN) mode liquid crystal has a different response time due to physical characteristics of the liquid crystal and a cell gap, etc. Typically, the TN mode liquid crystal has a rising time of 20 to 80 ms and a falling time of 20 to 30 ms. Since such a liquid crystal has a response time longer than one frame interval (i.e., 16.67 ms in the case of NTSC system) of a moving picture, a voltage charged in the liquid crystal cell is progressed into the next frame prior to arriving at a target voltage. Thus, due to a motion-blurring phenomenon a screen is blurred out at the moving picture.

[0010] Referring to **FIG. 1**, the conventional LCD cannot express desired color and brightness. Upon implementation of a moving picture, a display brightness BL fails to arrive at a target brightness corresponding to a change of the video data VD from one level to another level due to its slow response time. Accordingly, a motion-blurring phenomenon appears from the moving picture and a display quality is deteriorated in the LCD due to a reduction in a contrast ratio.

[0011] In order to overcome such a slow response time of the LCD, U.S. Pat. No. 5,495,265 and PCT International Publication No. WO99/05567 have suggested to modulate data in accordance with a difference in the data by using a look-up table (hereinafter referred to as high-speed driving method). This high-speed driving method allows data to be modulated by a principle as shown in **FIG. 2**.

[0012] Referring to **FIG. 2**, a conventional high-speed driving method modulates input data VD and applies the modulated data MVD to the liquid crystal cell, thereby obtaining a desired brightness MBL. This high-speed driving method increases $|V_a^2-V_F^2|$ from the above equation (1) on the basis of a difference in the data so that a desired brightness can be obtained in response to a brightness value of the input data within one frame interval, thereby rapidly reducing a response time of the liquid crystal. Accordingly, the LCD employing such a high-speed driving method compensates for a slow response time of the liquid crystal by modulating a data value in order to alleviate a motion-blurring phenomenon in a moving picture, thereby displaying a picture at desired color and brightness.

[0013] In other words, the high-speed driving method detects a variation in most significant bit data through a comparison of most significant bit data MSB of a current frame Fn with most significant bit data MSB of the previous frame Fn−1. If the variation in the most significant bit data MSB is detected, a modulated data corresponding to the variation is selected from a look-up table so that the most significant bit data MSB is modulated as shown in **FIG. 3**. The high-speed driving method modulates only a part of the most significant bits among the input data for reducing a memory capacity. For example, the high-speed driving method can be implemented as shown in **FIG. 4**.

[0014] Referring to **FIG. 4**, a conventional high-speed driving apparatus includes a frame memory **43** connected to a most significant bit output bus line **42** and a look-up table **44** connected to the most significant bit output bus line **42** and an output terminal of the frame memory **43**.

[0015] The frame memory **43** stores most significant bit data MSB during one frame period and supplies the stored data to the look-up table **44**. Herein, the most significant bit data MSB are high-order 4 bits among 8 bits of the source data RGB.

[0016] The look-up table **44** makes a mapping of the most significant bit data of the current frame Fn inputted from the most significant bit output bus line **42** and the most significant bit data of the previous frame Fn−1 inputted from the frame memory **43** into a modulation data table such as Table 1 to select modulated most significant bit data Mdata. Such modulated most significant bit data Mdata are added to an non-modulated least significant bit data LSB from a least significant bit output bus line **41** before outputting to a liquid crystal display.

TABLE 1

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	2	3	4	5	6	7	9	10	12	13	14	15	15	15	15
1	0	1	3	4	5	6	7	8	10	12	13	14	15	15	15	15
2	0	0	2	4	5	6	7	8	10	12	13	14	15	15	15	15
3	0	0	1	3	5	6	7	8	10	11	13	14	15	15	15	15
4	0	0	1	3	4	6	7	8	9	11	12	13	14	15	15	15
5	0	0	1	2	3	5	7	8	9	11	12	13	14	15	15	15
6	0	0	1	2	3	4	6	8	9	10	12	13	14	15	15	15
7	0	0	1	2	3	4	5	7	9	10	11	13	14	15	15	15
8	0	0	1	2	3	4	5	6	8	10	11	12	14	15	15	15
9	0	0	1	2	3	4	5	6	7	9	11	12	13	14	15	15
10	0	0	1	2	3	4	5	6	7	8	10	12	13	14	15	15
11	0	0	1	2	3	4	5	6	7	8	9	11	13	14	15	15
12	0	0	1	2	3	4	5	6	7	8	9	10	12	14	15	15
13	0	0	1	2	3	3	4	5	6	7	8	10	11	13	15	15
14	0	0	1	2	3	3	4	5	6	7	8	9	11	12	14	15
15	0	0	0	1	2	3	3	4	5	6	7	8	9	11	13	15

[0017] In the above Table 1, a left column is for a data voltage VDn−1 of the previous frame Fn−1 while an uppermost row is for a voltage VDn of the current frame Fn.

[0018] Such a conventional high-speed driving method enhances a dynamic contrast ratio in comparison with a conventional normal driving method that does not modulate the source data. However, the conventional high-speed driving method gradually enhances brightness so that a desired brightness level is achieved at the end of one frame period. Due to this, in the conventional high-speed driving method, the dynamic contrast ratio cannot be reached at a desired level. Furthermore, a color represented by combining red, green, and blue is distorted when those colors are reproduced.

SUMMARY OF THE INVENTION

[0019] Accordingly, the present invention is directed to a method and apparatus for driving a liquid crystal display that substantially obviates one or more of problems due to limitations and disadvantages of the related art.

[0020] Another object of the present invention is to provide a method and apparatus for driving a liquid crystal display that is adaptive for enhancing a picture quality.

[0021] Additional features and advantages of the invention will be set forth in the description which follows and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0022] To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, a method of driving a liquid crystal display includes modulating source data using registered data previously provided and supplying the modulated data to a liquid crystal panel at an initial period of one frame period, and applying data different from the modulated data to the liquid crystal panel at a later period of the one frame period.

[0023] In another aspect of the present invention, an apparatus for driving a liquid crystal display includes a modulator modulating source data using registered data, and a data provider alternatively applying the modulated data and data different from the modulated data to the liquid crystal panel within one frame period.

[0024] In a further aspect of the present invention, a liquid crystal display includes a liquid crystal display panel displaying images and having a plurality of data lines and a plurality of scanning lines thereon, a modulator modulating source data based on registered data previously provided therein, and a data provided alternatively applying the modulated source data and the source data to the liquid crystal panel through the data lines within one frame period.

[0025] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0026] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this application, illustrate embodiments of the invention and together with the description serve to explain the principle of the invention.

[0027] In the drawings:

[0028] **FIG. 1** is a waveform diagram showing a brightness variation of a data modulation according to a conventional liquid crystal display driving method;

[0029] **FIG. 2** is a waveform diagram showing a brightness variation of a data modulation according to a conventional high-speed driving method;

[0030] **FIG. 3** illustrates a modulation of most significant bit data in the conventional high-speed driving apparatus using 8 bits data;

[0031] **FIG. 4** is a block diagram showing a configuration of a conventional high-speed driving apparatus for a liquid crystal display;

[0032] **FIG. 5** is a block diagram showing a configuration of a driving apparatus for a liquid crystal display according to the present invention;

[0033] **FIG. 6** is a block diagram for a data modulator of **FIG. 5**; and

[0034] **FIGS. 7A and 7B** are graphic diagrams respectively showing modulated data and brightness of the conventional high-speed driving and the present invention, and **FIG. 7C** is a graphic diagram illustrating an improvement indicated by a dark area.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0035] Reference will now be made in detail to the illustrated embodiments of the present invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

[0036] **FIG. 5** is a schematic diagram for a driving apparatus for a liquid crystal display (LCD) according to the present invention.

[0037] The LCD driving apparatus includes a liquid crystal display panel **57** having a plurality of data lines **55** and a plurality of gate lines **56** crossing each other and having TFT's provided at each intersection to drive liquid crystal cells Clc. A data driver **53** supplies data to the data lines **55** of the liquid crystal display panel **57**. A gate driver **54** applies a scanning pulse to the gate lines **56** of the liquid crystal display panel **57**. A timing controller **51** receives digital video data and synchronizes signals H and V. A data modulator **52** is connected between the timing controller **51** and the data driver **53** to modulate input data RGB. The LCD driving apparatus further includes a switch **58** selecting any one of a modulated data AMdata and the normal input RGB. A line memory **59** is connected between the timing controller **51** and the switch **58**. Herein, the normal data is non-modulated data.

[0038] The liquid crystal display panel **57** has a liquid crystal formed between two glass substrates and has the data lines **55** and the gate lines **56** provided on the lower glass substrate in such a manner to perpendicularly cross each other. The TFT provided at each intersection between the data lines **55** and the gate lines **56** responds to a scanning pulse to apply data on the data lines **55** to the liquid crystal cell Clc. To this end, a gate electrode of the TFT is connected to the gate lines **56** while a source electrode is connected to the data lines **55**. The drain electrode of the TFT is connected to each pixel electrode of the liquid crystal cell Clc.

[0039] The timing controller **51** rearranges digital video data supplied from a digital video card (not shown). The RGB data rearranged by the timing controller **51** are supplied to the data modulator **52** and the line memory **59**. Further, the timing controller **51** creates timing control signals, such as a dot clock Dclk, a gate start pulse GSP, a gate shift clock GSC (not shown), an output enable/disable signal, and a polarity control signal using horizontal and vertical synchronizing signals H and V to control the data driver **53** and the gate driver **54**. The dot clock Dclk and the polarity control signal are applied to the data driver **53** while the gate start pulse GSP and the gate shift clock GSC are applied to the gate driver **54**. Herein, frequencies of the timing control signals and the polarity control signal generated in the timing controller **51** have a polarity opposing to those of the conventional timing control signals and the prior polarity control signal. Also, magnitudes of the timing control signals and the polarity control signal are twice greater than those of the conventional timing control signals and the prior polarity signal. The timing controller **51** also provides a switching control signal SW allowing the switch **58** to be switched twice within one frame interval. To this end, the switching control signal SW is inverted in a logic value within one frame interval. In other words, the logic value of the switching control signal SW is inverted at each ½ period in comparison with the conventional vertical synchronous signal V. The timing controller **51** controls the switch **58** using the switching control signal SW.

[0040] The gate driver **54** includes a shift register sequentially generating a scanning pulse (i.e., a gate high pulse) in response to the gate start pulse GSP and the gate shift clock GSC applied from the timing controller **51**. A level shifter shifts a voltage of the scanning pulse into a level suitable for driving the liquid crystal cell Clc. The TFT is turned on in response to the scanning pulse to apply video data on the data lines **55** to the pixel electrode of the liquid crystal cell Clc. Each gate start pulse GSP and each gate shift clock GSC have a frequency twice greater than those of the conventional gate start pulse and the gate shift clock. Thus, they allow all scanning lines **56** on the liquid crystal display panel **57** to be scanned twice within one frame interval.

[0041] The data driver **53** is sequentially supplied with the modulated data AMdata and the normal data RGB from the switch **58** within one frame interval. It also receives the dot clock Dclk from the timing controller **51**. The data driver **53** continuously samples each of the modulated data AMdata and the normal data RGB in synchronization with the dot clock Dclk. Thereafter, the data driver **53** latches the sampled data for one line. The data for one line latched by the data driver **53** is converted into analog data and applied to the data lines **55** in each scanning period. Further, the data driver **53** may apply a gamma voltage corresponding to the modulated data to the data line **55**. The dot clock Dclk has a frequency twice greater than that of the conventional dot clock. Thus, each modulated data AMdata and the normal data RGB are applied to each liquid crystal cell Clc within one frame interval.

[0042] The data modulator **52** can modulate **4** most significant bits of the normal data RGB through a comparison of the data, as shown in **FIG. 4**. Alternatively, the data modulator **52** also can modulate the entire bits of the normal data RGB by comparing the entire bits of the normal data RGB, as shown in **FIG. 6**. To this end, the data modulator **52** includes a frame memory **61** storing 8 bits of the normal data RGB received from the timing controller **51** and a look-up table **62** comparing the 8 bits of the normal data from the timing controller **51** with the 8 bits of the normal data from the frame memory **61** to modulate the 8 bits of the normal data RGB into 8 bits of modulated data AMdata. Each modulated data AMdata stored into the look-up table **61** is obtained from following equation (3) to (5):

$$VDn<VDn-1 \rightarrow MDNn<VDn \quad (3)$$

$$VDn=VDn-1 \rightarrow MDNn=VDn \quad (4)$$

$$VDn>VDn-1 \rightarrow MDNn>VDn \quad (5)$$

[0043] where VDn−1 represents a data voltage in the previous frame, VDn is a data voltage of the current frame, and MVDn represents a modulated data voltage.

[0044] The switch **58** responds to the switching control signal SW from the timing controller **51** and sequentially applies the modulated data AMdata and the normal data RGB to the data driver **53** within one frame.

[0045] The line memory **59** delays the normal data RGB during the period of one line. The period of one line is a time for which the modulated data AMdata is applied to the data driver **53**.

[0046] **FIGS. 7A and 7B** illustrate variations in brightness in response to the applied voltage to the liquid crystal panel **57** according to the conventional art and the present invention, respectively. **FIG. 7C** illustrates an improvement in the variations in brightness by the present invention indicated by a dark area. One frame interval in the present invention is divided into an odd-numbered sub-field OSF and an even-numbered sub-field ESF. The period of each odd-numbered sub-field OSF and each even-numbered sub-field ESF can be appropriately adjusted within one frame interval.

[0047] In **FIG. 7A**, "VD" is a normal data voltage and "BL" is brightness varying with the normal data voltage VD. "MVD" is a modulated data voltage modulated by the conventional high-speed driving system and "MBL" is brightness varying with the modulated data voltage MVD. "AMVD" is a modulated data voltage modulated by the liquid crystal display driving apparatus and method according to the present invention and "AMBL" is brightness varying with the modulated data voltage AMVD.

[0048] In the odd-numbered sub-field OSF, the modulated data AMdata modulated by the data modulator **52** is applied to the liquid crystal panel **57**. Continuously, the normal data RGB, which is not modulated, is supplied to the liquid crystal panel **57** during the even-numbered sub-field ESF.

[0049] Since the modulated data voltage in the first odd-numbered sub-field OSF is higher (or lower) than the normal data voltage in the even-numbered sub-field ESF, an effective voltage of the modulated data voltage applied to the liquid crystal cell Clc is higher (or lower) than that of the normal data voltage. Accordingly, brightness of the liquid crystal cell reaches at a desired brightness level within the period of the odd-numbered sub-field OSF shorter than one frame. In other words, the modulated data voltage applied in the odd-numbered sub-field OSF can be higher or lower than the inputted current normal data voltage depend upon conditions satisfying the above equations (3) to (5).

[0050] On the other hand, the normal data voltage applied in the even-numbered sub-field ESF forces to maintain the desired brightness level achieved at the odd-numbered sub-field OSF during the period of the even-numbered sub-field ESF.

[0051] As shown in **FIG. 7C**, the liquid crystal display drive apparatus and method according to the present invention allow the brightness of the liquid crystal panel **57** to arrive rapidly at the desired brightness level and to maintain the desired level during the constant period. Meanwhile, the conventional high-speed driving system forces to each the desired brightness level only at the end of the frame because the brightness is gradually varied with the modulated data maintaining a constant voltage within one frame.

[0052] On the other hand, the modulated data AMdata of the high-speed driving apparatus according to present invention can be adjusted to be higher than that of the conventional high-speed driving system. Due to this fact, if the modulated data AMdata of the present invention is applied to the liquid crystal panel **57** through the entire period of the frame in such a manner to identify with the conventional high-speed driving system, a white pattern (non-desired) may be generated by an over-shoot. In such a case, a picture quality may be deteriorated.

[0053] As described above, the LCD drive apparatus and method according to the present invention apply the normal data to the liquid crystal panel at the initial half period of the frame after supplying of the modulated data to the liquid crystal panel during the later half period of the frame. Thus, a desired brightness level is achieved within the initial period of the frame. Accordingly, the LCD drive apparatus and method in the present invention enhances a dynamic contrast and a color reproducibility. As a result, the LCD drive apparatus and method of the present invention provide with a high display quality.

[0054] The data modulator **52** may be implemented by other means, such as a programmable software and a microprocessor for carrying out the present invention, rather than a look-up table. The present invention can also be applied to a digital flat display device, which requires a data modulation, such as a plasma display panel, an electro-luminescence display device, and an electric field emitting device and so on. Furthermore, the switch and the line memory can be combined in one unit together with the timing controller or the data driver.

[0055] It will be apparent to those skilled in the art that various modifications and variations can be made in the method and apparatus for driving the liquid crystal display of the present invention without departing from the spirit or scope-of the inventions. Thus, it is intended that the present invention covers the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

1. A method of driving a liquid crystal display, comprising:

modulating source data using registered data previously provided and supplying the modulated data to a liquid crystal panel at an initial period of one frame period; and

applying data different from the modulated data to the liquid crystal panel at a later period of the one frame period.

2. The method according to claim 1, wherein the data applied to the liquid crystal panel at the later period is the source data.

3-4 (Canceled).

5. The method according to claim 1, wherein the later period begins at a half period of the one frame period.

6. The method according to claim 2, wherein the source data are not applied to the liquid crystal panel while the modulated data are applied thereto.

7. An apparatus for driving a liquid crystal display, comprising:

a modulator modulating source data using registered data previously provided therein; and

a data provider alternatively applying the modulated data and data different from the modulated data to the liquid crystal panel within one frame period.

8. The apparatus according to claim 7, wherein the data different from the modulated data is the source data.

9-14 (Canceled).

15. The apparatus according to claim 7, wherein the data provider includes a delay circuit delaying the source data while the modulated data are applied to the liquid crystal panel.

16. The apparatus according to claim 7, further comprising:

a data driver applying the modulated data and the source data received alternatively from the switch to a plurality of data lines on the liquid crystal panel; and

a scanning driver applying a scanning pulse to a plurality of scanning lines on the liquid crystal panel.

17. The apparatus according to claim 16, wherein the scanning pulse has a frequency high enough to scan twice entire scanning lines on the liquid crystal panel within the one frame period.

18. A liquid crystal display comprising:

a liquid crystal display panel displaying images and having a plurality of data lines and a plurality of scanning lines thereon;

a modulator modulating source data based on registered data previously provided therein; and

a data provider alternatively applying the modulated source data and the source data to the liquid crystal panel through the data lines within one frame period.

19 (Canceled).

20. The liquid crystal display panel according to claim 18, wherein the data provider applies the modulated source data to the liquid crystal display for a first half frame period and the source data to the liquid crystal display for a second half period.

21. A method of driving a liquid crystal display, comprising:

applying a modulated data signal to a liquid crystal panel within one frame period; and

applying a data signal within the one frame period,

wherein the modulated data signal has a voltage level larger than that of the data signal.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SHARP CORPORATION, SHARP ELECTRONICS CORPORATION, and SHARP ELECTRONICS MANUFACTURING COMPANY OF AMERICA, INC.,
Petitioners

v.

SURPASS TECH INNOVATION LLC,
Patent Owner

Case IPR2015-00021
Patent No. 7,202,843 B2

REBUTTAL DECLARATION OF MICHAEL J. MARENTIC IN SUPPORT OF PETITIONERS' REPLY TO PATENT OWNER'S RESPONSE

SHARP EXHIBIT 1010
Sharp Corp., et al. v. Surpass Tech Innovation LLC
IPR2015-00021

TABLE OF CONTENTS

I, Michael J. Marentic, declare as follows:

The following is my written Declaration submitted in rebuttal to the Patent Owner's, Surpass Tech Innovation LLC ("Patent Owner"), Response (Paper 20, "Response") and the Declarations of William K. Bohannon in support thereof (Exs. 2005-2006). My Declaration includes my rebuttal opinions regarding Claims 4, 8 and 9 of U.S. Patent No. 7,202,843 ("the '843 Patent," Ex. 1001), and is submitted on behalf of Petitioners Sharp Corporation, Sharp Electronics Corporation, and Sharp Electronics Manufacturing Company of America, Inc. (collectively, "Petitioners").

I. SUMMARY OF MY DECLARATION AND OPINIONS

1. I understand that the Patent Trial and Appeal Board ("the Board") has initiated *inter partes* review of Claims 4, 8 and 9 of the '843 Patent. Specifically, I understand that the Board has found that Petitioners have shown that there is a reasonable likelihood that Claims 4, 8 and 9 are invalid as anticipated by U.S. Patent Application No. 2004/0196229 to Ham ("Ham," Ex. 1005). (Paper 10, Decision at 14-15).

2. I have reviewed the Petition (Paper 1) and the Board's Decision (Paper 10) and concur that Claims 4, 8 and 9 are anticipated by Ham.

3. I understand that the Patent Owner and its expert, Mr. Bohannon, argue that Claims 4, 8 and 9 are not anticipated by Ham. As set forth herein, it is my opinion that Surpass and Mr. Bohannon are wrong.

II. BACKGROUND INFORMATION

A. Summary of My Professional Background and Qualifications

4. Exhibit 1011 is my *curriculum vitae* which sets forth my professional background and qualifications. A list of publications that I have authored or co-authored is included.

5. I have many years of experience in the flat panel display industry. I first became involved in the flat panel display industry in 1973, when I began working at the University of Illinois Coordinated Science Laboratories where the AC Plasma Display Panel ("PDP") was invented. During my studies at the University, I was employed as an intern working in the area of plasma display construction and gas discharge physics characterization. I received a B.S. degree in Engineering Physics from the University of Illinois.

6. Upon entering graduate school, I continued my work on the characterization of gas discharge in PDP pixels. I received an M.S. degree in Electrical Engineering from the University of Illinois, and wrote my master's thesis on measuring the electron density in an AC PDP.

7. One of my engineering positions was with Interstate Electronics Corporation (IEC) as a design electrical engineer. IEC designed PDP drive electronics, mechanically packaged the display modules, and incorporated them into terminals for harsh, military environments. During this time, I was awarded several patents relating to PDP technologies. I also investigated LCDs and thin film electroluminescent displays for incorporation into military applications.

8. I later formed Plasma Displays, Inc., a single proprietorship consulting corporation. I worked for several clients, one being Bell Laboratories and AT&T at their joint Reading, Pennsylvania facility. This facility was where the original picture phone was developed, the first commercial light emitting diodes ("LEDs") were manufactured, and AT&T's PDPs were developed and manufactured. I worked on PDP drive electronic design, driver-to-panel interconnect, driver circuit characterization, and yield improvement.

9. I was a founder and Vice President of Plasmaco, a company that acquired IBM's PDP production line in New York. Plasmaco manufactured several types of PDPs, including VGA panels for early notebook computers.

10. At Science Applications International Corporation, I worked on efficient backlights for LCDs, some for direct viewing in sunlight. Commercially available LCDs were disassembled and repackaged with these backlights. The finished displays were used in cockpit avionics, medical, banking, and FAA towers.

11. At Hitachi, from 1995 to 1999, I managed a technology center that developed technologies relating to the interface between the motherboard and the LCD driver chips for flat panel monitors and notebook displays. I reported directly to the LCD design and manufacturing center in Japan. I had access to future LCD technical details and specifications, and facilitated technology transfer between Silicon Valley firms and Japan management. The Video Electronics Standards Association ("VESA") writes and publishes video standards for the electrical interfacing for displays. I was the chairman of the VESA flat panel display committee, a member of the board of directors, and later the president of the board of directors.

12. While at Philips, from 1999 to 2001, I managed a group of engineers that designed electronics for flat panel displays. My group designed interface timing ICs and video processing circuit boards for monitors and televisions utilizing LCDs. Philips invested in a tiled LCD display company, and I participated in the technology development using Philips panels. My group designed circuits and assisted with their incorporation into commercial products within Philips' worldwide subsidiaries.

13. Philips purchased the LCD factory of the Korean company LG, and later formed a joint venture called LG-Philips LCD. I was a member of the group of technical advisors that performed the due diligence for Philips for the purchase.

14. At Alien Technology, I was a member of the integrated design team that produced custom drivers made for cholesteric LCD displays, organic LEDs, and polymer dispersed LCDs.

15. I am the named inventor or co-inventor on three U.S. patents in the PDP field.

B. Data and Other Information Considered

16. In forming my opinions, I reviewed the following documents referenced by their "Paper" or "Exhibit" number:

PAPER NO.	EXHIBIT NO.	DESCRIPTION
1	—	Petition for *Inter Partes* Review ("IPR")
—	1001	U.S. Patent No. 7,202,843 to Shen et al. ("'843 Patent")
—	1005	U.S. Patent Application Publication No. 2004/0196229 to Ham ("Ham")
—	1006	Prosecution History of U.S. Appl. No. 10/707,741
9	—	Patent Owner's Preliminary Response
10	—	Decision - Institution of IPR
20	—	Patent Owner's Response

PAPER NO.	EXHIBIT NO.	DESCRIPTION
—	2005	Declaration of William K. Bohannon
—	2006	Second Declaration of William K. Bohannon
—	1009	Transcript of the August 20, 2015 Deposition of William K. Bohannon

17. I also base this declaration on my knowledge from my 30 years of experience working on liquid crystal display (LCD) and related technologies.

C. Scope of the Assignment

18. I have been requested by counsel for Petitioners to provide my expert opinion in rebuttal to Patent Owner's Response, as well as the portions of Mr. Bohannon's Declaration cited in Patent Owner's Response.

D. Compensation

19. I am being compensated at my consulting rate of $250 per hour for my time spent in connection with this case. I am being separately reimbursed for any out-of-pocket expenses. No part of my compensation is dependent upon the outcome of this proceeding or the nature of the opinions that I express.

E. Legal Standards

20. To render my invalidity analysis, I have been informed about the legal standards for patent invalidity in *inter partes* review proceedings before the Patent Trial and Appeal Board.

21. Specifically, I understand that the petitioner must prove patent invalidity by a "preponderance of the evidence" and that there is no "presumption of validity" in *inter partes* review proceedings.

22. I understand that claims are to be given their "broadest reasonable" construction in light of the specification as would be read by a person of ordinary skill in the art. In this regard, I also understand that, under the broadest reasonable construction standard, claim terms are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure.

23. I understand that, while claims must be construed in light of the specification, it is generally not permissible to import limitations from the specification. I have also been informed that any special definition for a claim term must be set forth in the specification with reasonable clarity, deliberateness, and precision, and, in the absence of such a definition, limitations are not to be read from the specification into the claims.

24. I have been informed that there is no requirement to construe terms that are readily understood by a person of ordinary skill the art.

25. I also understand that a patent claim may be invalidated as anticipated if a single prior art reference discloses each and every element of the patent claim. In this regard, I have been informed that a prior art reference need not use the exact terminology used in the claim in order to anticipate that claim.

III. THE '843 PATENT

26. Patent Owner and Mr. Bohannon describe their understanding of the '843 Patent. (*See* Paper No. 20, Response at 13-17; Ex. 2005, Bohannon Decl. ¶¶14-23). However, their descriptions are inaccurate and incomplete. (*See, e.g.*, Ex. 2005, Bohannon Decl. ¶18 (stating that "the '843 Patent uniformly correlates the idea of overdriving and controlling the transmission rate . . .")). Therefore, I have correctly summarized the relevant disclosures of the '843 Patent below.

27. The '843 Patent is entitled Driving Circuit of a Liquid Crystal Display Panel and Related Driving Method" and issued on April 10, 2007 from U.S. Patent Application No. 10/707,741 ("the '741 Application", Ex. 1006), filed on January 8, 2004.

28. The '843 Patent generally relates to circuits and methods for driving an LCD panel. The '843 Patent describes a generic LCD panel 30 that includes a plurality of scan lines 32 (also called gate lines), a plurality of data lines 34, and a

plurality of pixels 36 arranged in a matrix. (Ex. 1001, '843 Patent, Col. 1:27-31, Col. 3:37-40). Each pixel 36 includes a switching device 38 (e.g., a TFT) and a liquid crystal device 39 (which is also called a "pixel electrode"). (*Id.* at Col. 3:40-43). These components are shown in Figure 4 of the '843 Patent (annotated and reproduced below), which also shows that the gate of the switching device 38 in each pixel is connected to the corresponding scan line 32, while the source of the switching device in the pixel is connected to the corresponding data line 34. (*Id.* at Col. 3:43-47).

29. Like all active matrix TFT panels, the LCD panel 30 is driven by applying scan line voltages to the scan lines 32 to turn on the switching devices 38 and applying "data impulses" to the data lines 34 to charge the liquid crystal devices 39 via the switching devices 38. (*Id.*).

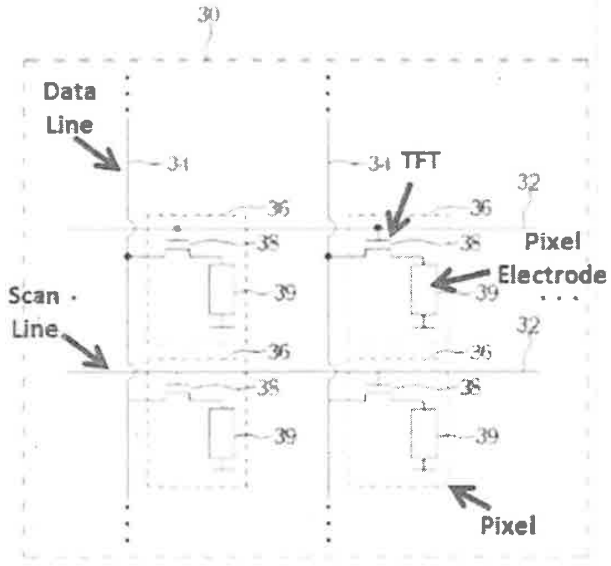


Fig. 4

30. By way of background, a "twisted nematic" (or TN mode) LCD panel, such as the one discussed in the '843 Patent, produces images by controlling the "transmission rate" of each pixel or, in other words, the percentage of light from the display panel's backlight that passes through each pixel. In this regard, Mr. Bohannon has opined that the phrase "controlling the transmission rate" is synonymous with "overdriving" (discussed below). (*See, e.g.*, Ex. 2005, Bohannon Decl. ¶¶28-30). Mr. Bohannon is mistaken.

31. The '843 Patent specification describes an LCD panel where the "transmission rate" was controlled without overdriving. (Ex. 1001, '843 Patent, Col. 1:53-2:2). Specifically, Figure 2 of the '843 Patent plots "transmission rate" (vertical axis) versus time (horizontal axis). The '843 Patent explains that "[t]he

curve C1 shows the ***transmission rate*** of a pixel ***not overdriven***." (*Id.* at Col. 1:57-60). By contrast, curve C2 shows the transmission rate of a pixel that is overdriven. Since the '843 Patent clearly shows transmission rates that were controlled both with (C2) and ***without*** (C1) overdriving, overdriving cannot be synonymous with "controlling the transmission rate.

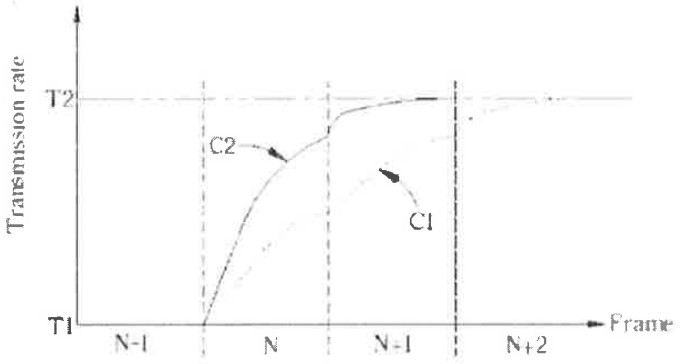


Fig. 2 Prior art

32. The '843 Patent's use of the phrases "transmission rate" and "controlling the transmission rate" is consistent with the understanding of those of ordinary skill in the art. Specifically, in its "off" state, the twisted nematic panel discussed in the specification appears black as the pixel blocks the backlight illumination. This type of display is referred to in the art as a "normally black display." (*See* Ex. 1015, Sharp Application Note at 10). In operation, a voltage (or data impulse) is applied to the pixel electrodes through the data lines. This voltage causes the liquid crystal material in each pixel to be rearranged. (Ex. 1001, '843

Patent, Col. 1:62-65). As a result, depending on the applied voltage, different amounts of light are transmitted through the pixel. A pixel's "transmission rate" of light is therefore directly related to the pixel's input voltage.

33. When no voltage is applied to the pixel's electrodes the liquid crystal molecules remain in an ordered state that blocks nearly all light from the backlight. As a result, only a minimal amount of light passes through the pixel (i.e., the transmission rate is near zero and the pixels appear black). By contrast, when a voltage is applied to the pixel electrodes, the LC molecules reorient themselves in such a manner that light from the backlight is allowed to pass through the pixel (i.e., the pixels appear brighter to the observer). As discussed above, the particular percentage of light that passes through the pixel (or transmission rate) increases as the applied voltage increases.

34. A range of light transmission values (or gray scale values) can be obtained by applying intermediate voltages between the full "Off" and full "On" voltages. In the LCD panel described in the '843 Patent, the number of gray scale values is 256 values (i.e., 0 to 255). (Ex. 1001, '843 Patent, Col. 1:35-37). The lowest value "0" represents the darkest display illuminance, while a luminance value of "255" represents the highest transmission rate. The interplay between data line voltages, LC twisting angles and transmission rate is correctly summed up in the '843 Patent: "***Different data voltages cause*** different twisting angles and

show ***different transmission rates***." (Ex. 1001, '843 Patent, Col. 3:58-62). This is consistent with how the term "controlling a transmission rate" is understood and used in the art. This also confirms that Mr. Bohannon's assertion, that there is a connection between "controlling the transmission rate" and "overdriving," is incorrect.

35. The time that the pixel molecules need to react (i.e., rearrange) in response to a driving voltage is called the "response time" (or response speed). The image quality of an LCD panel is dependent, in part, on this response time; the faster the response time, the better the image quality for video imagery. In this regard, the '843 Patent explains that a delay in the response time of an LCD panel causes image defects such as blurring, and describes the need for improving the LCD response speed. (*Id.* at Col. 1:21-26, Cols. 1:62-2:2).

36. In this regard, the '843 Patent discusses and claims two previously known techniques for improving the response time and resultant image quality of LCD displays: (1) applying two or more data impulses to a pixel within a given frame; and (2) "overdriving" the signal data. These are two independent concepts, which can be used by themselves or in combination to reduce blurring.

37. Specifically, applying two or more data impulses to a pixel within a given frame helps smooth out fast motion video and improves the image sequence that the eye perceives. When the first data impulses are applied to each pixel

earlier in the frame period, the LC material initiates its response sooner. As the gate scan starts at the top of the display and finishes at the bottom in half of a frame period (rather than in the full period), pixels are driven to the final voltage sooner and have a longer time to orient to the applied pixel impulse. For example, the pixels in the first line of the display are driven with a first data impulse at the start of the frame and with a second data impulse a half of a frame later. The displayed image will have less blur since the LC material has an additional half frame to respond and, therefore, reach the target transmission rate more quickly.

38. The second technique, overdriving, enables a pixel to change from one gray level (i.e., shade of color) to another more quickly by either boosting or decreasing the requested pixel value. (*Id.* at Col. 2:2-7). This decreases the difference between the before and after pixel values and the amount of time required for the pixel to change state.

39. The '843 Patent states that overdriving alone can improve the performance of an LCD display, to a certain extent. (*See id.* at Col. 2:7-12, Fig. 2). In addition, as discussed above, applying two or more data impulses in a single frame alone improves performance of an LCD display. To enable a signal to reach a target transmission rate within a single frame period, the '843 Patent suggests combining these techniques, i.e., applying two or more overdriven impulses to each pixel within the given frame period. (*Id.* at Col. 4:20-40, Col. 5:63-6:25).

For example, as shown in Figure 6 of the '843 Patent, each single frame period is divided into two segments (e.g., Frame N+1 is divided into the segments n+2 and n+3). Two overdriven data impulses are then applied to these two segments (e.g., one impulse during n+2 and a second during n+3) to the pixel within the given frame period (e.g., N+1). This method allegedly allows the signal to reach a target transmission rate (T2) within a single frame period (e.g., N+1). (*Id.* at Cols. 3:15-4:43, Col. 1:39-41).

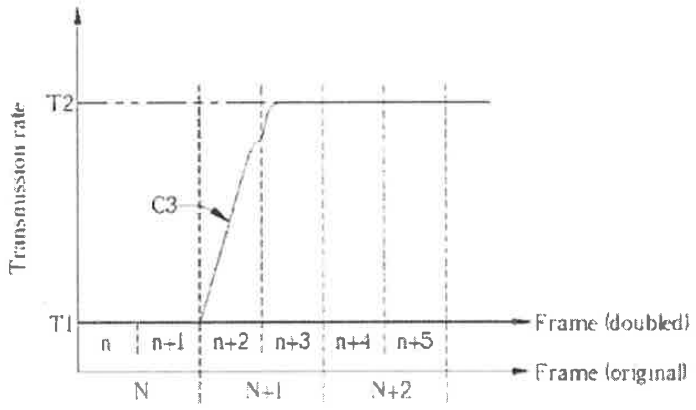


Fig. 6

A. Claims 4, 8 and 9 of the '843 Patent

40. Claims 4, 8 and 9 are method claims directed to methods of driving an LCD display. Claim 4 is in independent form. These claims are reproduced below.

> 4. A method for driving a liquid crystal display (LCD) panel, the LCD panel comprising:
>
> a plurality of scan lines;

a plurality of data lines; and

a plurality of pixels, each pixel being connected to a corresponding scan line and a corresponding data line, and each pixel comprising a liquid crystal device and a switching device connected to the corresponding scan line, the corresponding data line, and the liquid crystal device, and

the method comprising:

receiving continuously a plurality of frame data;

generating a plurality of data impulses for each pixel within every frame period according to the frame data; and

applying the data impulses to the liquid crystal device of one of the pixels within one frame period via the data line connected to the pixel ***in order to control a transmission rate*** of the liquid crystal device of the pixel.

8. The method of claim 4 further comprising:

applying a scan line voltage to the switch device of the pixel via the scan line connected to the pixel in order to have the data impulses be applied to the liquid crystal device of the pixel.

9. The method of claim 4 wherein each frame data comprises a plurality of pixel data, and each pixel data corresponds to a pixel.

41. As can be seen, method claims 4, 8 and 9 are only directed to one of the disclosed solutions for blurring, namely, applying two or more data impulse to a pixel within a given frame. By contrast, Claim 1 (not under review) requires both: (1) applying two or more data impulse to a pixel within a given frame; and (2) overdriving.

IV. LEVEL OF SKILL IN THE ART

42. A person of ordinary skill in the art would have had an undergraduate degree in electrical engineering, or equivalent work experience. That person would also have had 3 or more years of experience designing flat panel display drive electronics and active matrices for LCDs.

43. I have also considered the level of skill proposed by Mr. Bohannon, namely, that "a person of ordinary skill in the relevant art of the '843 patent has at least a bachelor's degree in electrical engineering, mathematics, or computer science with two or more years of experience in designing electronics and displays." (Ex. 2005, Bohannon Decl. ¶ 8). I do not agree that a person with a degree in mathematics or computer science would have the requisite education to design LCD drive electronics. Nevertheless, even assuming that Mr. Bohannon's proposed level of skill were correct, it would not affect my analysis.

V. CLAIM CONSTRUCTION

44. As previously noted, I understand that in *inter partes* review proceedings, patent claims are to be given their "broadest reasonable" construction in light of the specification as would be read by a person of ordinary skill in the art.

45. I understand that the Petition asserted that Claim 4, 8 and 9 of the '843 Patent "are generally clear on their face, and should be given their broadest reasonable construction in light of the specification of the '843 Patent." (Paper 1 at

18). Likewise, I understand that, in instituting this proceeding, the Board did not find it necessary to construe any of the terms of Claims 4, 8 or 9. (Paper 10, Decision at 5).

46. I agree with the Petitioners and the Board. All of the terms of Claims 4, 8 and 9 of the '843 Patent are readily understood by a person of ordinary skill in the art. They do not require further construction.

47. I understand that Patent Owner and Mr. Bohannon, nevertheless, argue that certain terms of Claim 4 require construction: (1) "generating"; and (2) "control a transmission rate." I address these arguments below.

VI. HAM ANTICIPATES THE CLAIMS

A. The Disclosure of Ham

48. Ham was published on October 7, 2004 and is based on an application filed on November 27, 2001. I am advised that Patent Owner does not dispute that Ham is prior art.

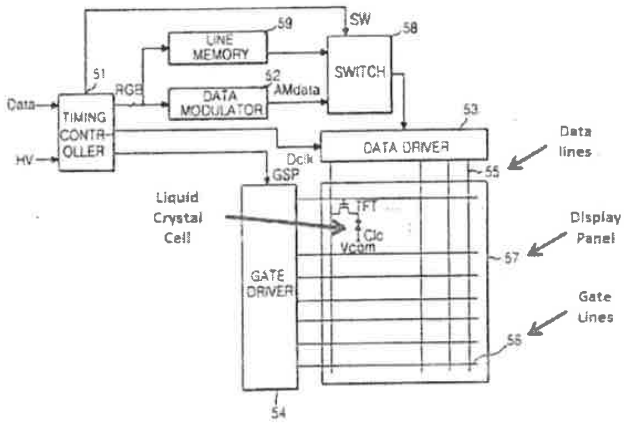
49. Neither Patent Owner nor Mr. Bohannon provides a complete description of the relevant portions of Ham cited in the Petition. In order to address their arguments, I provide a complete summary of Ham below.

50. Ham is directed to a "method and apparatus for driving a liquid crystal display device suitable for enhancing a picture quality." (Ex. 1005, Ham, Abstract).

Ham recognizes that, if overdriven pixel data is applied "through the entire period of the frame" (as taught by the prior art), "picture quality may be deteriorated." (*Id.* ¶52). To address this problem, Ham teaches applying overdriven pixel data in only the first half of the frame period, and applying non-overdriven data in the second half of the frame period. (*Id.* ¶53).

51. One issue raised by Patent Owner and Mr. Bohannon is whether Petitioners have established that Ham "generates a plurality of data impulses to . . . one of the pixels within one frame period." In this regard, Petitioners cited Figure 5 of Ham, which provides an overview of Ham's LCD driving device. (Paper 1, Petition at 45; *see also* Paper 10, Decision at 11-13). As shown in Figure 5 of Ham (annotated and reproduced below), the "LCD driving apparatus includes a liquid crystal display panel **57** having a plurality of data lines **55** and a plurality of gate lines **56** crossing each other and having TFT's provided at each intersection to drive liquid crystal cells Clc." (*Id.* ¶37).

FIG.5



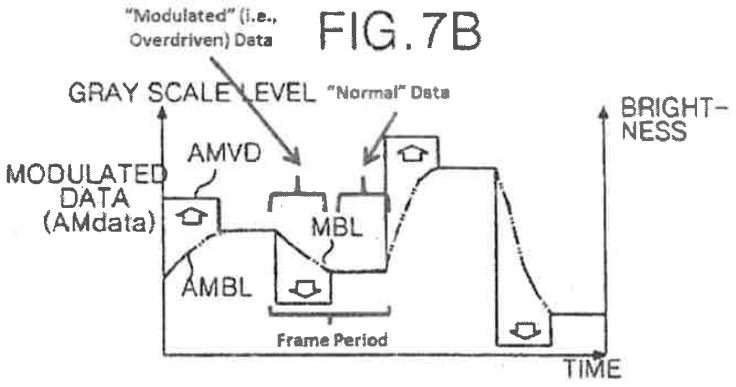
52. The LCD driving apparatus also includes a data driver 53 that supplies data impulses to data lines 55 and gate driver 54 applies a scanning pulse to gate lines 56. *Id.* Timing controller 51 receives digital video data and synchronizes signals H and V for gate and source driver circuits. Data modulator 52 is connected between timing controller 51 and data driver 53 via switch 58 to modulate input data RGB. Line memory 59 is connected between timing controller 51 and switch 58. Switch 58 is utilized to select any one of modulated data AMdata and normal input RGB. *Id.*

53. Using these components, the driving apparatus in Figure 5 generates two data impulses (i.e., "modulated data" signal and "normal data" signal) for each pixel within one frame period. (*Id.* ¶37; *see also id.* ¶ [0040], Fig. 7C). Neither Patent Owner nor Mr. Bohannon address the operation of Ham's driving circuit (as

shown in Figure 5) as a whole. Rather, they address only one component in Figure 5, i.e., the data modulator 52.

54. In all events, as shown in the Table 1 of Ham, "modulated data" is selected from a look-up table based upon the digital data of the "previous frame" and the digital data of the "current frame." (*Id.* ¶¶13, 17). As a result, the "modulated data" signal is overdriven. The "normal data" signal is not overdriven. Rather, the "normal data" signal is a time shifted copy of the digital input signal. The output of the circuit disclosed by Ham is shown in Figure 7B (annotated and reproduced below). As can be seen, each frame period is split into two halves. During the first half of the frame period, an overdriven data impulse is applied to each pixel. During the second half of the frame period, a non-overdriven data impulse is applied.

FIG. 7B



B. Patent Owner's Arguments

55. I have reviewed the Petition, including the discussion of Ham and the related claim charts. I concur with Petitioners that Ham anticipates Claims 4, 8 and 9.

56. I note that Patent Owner's Response and Mr. Bohannon's Declaration address only the last two limitations of Claim 4:

> ***generating*** a plurality of data impulses for each pixel within every frame period according to the frame data; and
>
> ***applying the data impulses*** to . . . one of the pixels within one frame period via the data line . . . in order ***to control a transmission rate*** of the liquid crystal device of the pixel.

57. In addition, during his deposition, Mr. Bohannon confirmed that, other than with respect to these two limitations, he is not offering any other opinions in this proceeding. (Ex. 1009, Bohannon Tr. 127:23-131:18). I address his opinions on these two limitations below.

1. Ham Discloses the "Generating" Step

58. Claim 4 requires "generating a ***plurality of data impulses*** for each pixel within every frame period according to the frame data." As discussed above, for each frame period, Ham's driving method (and related driving apparatus) receives one piece of information (i.e., "digital video data") for each pixel in a frame and generates two data impulses for that pixel: (1) a modulated data voltage;

and (2) a normal data voltage. (Paper 1, Petition at 48; *see also* Paper 10, Decision at 11-13). In my opinion, this establishes that Ham satisfies the "generating" limitation of Claim 4.

59. This is not surprising since the relevant elements of Ham's driving circuit are very similar to those shown in the driving circuit of the '843 Patent. Specifically, Ham's source driver (i.e., the "data driver 53")[1] receives two digital signals (i.e., "the modulated data AMdata and the normal data RGB") within one frame interval, "convert[s]" (i.e., generates) each of these digital signals into two corresponding analog data signals (i.e., a plurality of data impulses) and "appl[ies]" these two data impulses "to the data lines 55 in each scanning period." (Paper 1, Petition at 48 citing, *inter alia*, Ex. 1005, Ham ¶¶ 40, 41).

60. In the '843 Patent, the step of "generating a plurality of data impulses" is also performed by source driver 18 in very similar manner as quoted below:

> [W]hen the pixel data GN, GN(2) are generated, ***the source driver*** of the driving circuit 10 ***converts*** the pixel data GN, GN(2) ***into two corresponding data impulses***

[1] The terms "source driver" and "data driver" are used interchangeably in the art. They both refer to components that drive the "data lines" of an active matrix LCD panel, which are, in turn, connected to the "source" of a thin film transistor. (*See, e.g.*, Ex. 1001, '843 Patent, Figure 4).

and then applies them to the liquid crystal device 39 via the data line 32 in the frame period N . . . .

(Ex. 1001, '843 Patent, Col. 4:8-14). In addition, "***the source driver 18 generates two corresponding data impulses*** according to the two pieces of pixel data and applies them to the pixel electrode 39 of the corresponding pixel 36 in order to control the transmission rate . . .of the pixel electrode 39." (*Id.* at Col. 4:22-28).

61. Despite the simplicity of the "generating" limitation, and the straightforward teachings of Ham, Patent Owner and Mr. Bohannon raise two arguments in connection with this limitation, namely, that: (1) Petitioners have not construed the word "generating"; and (2) Ham's "data modulator 52," by itself, does not perform the "generating" step. I address these arguments below.

i. "Generating" Is Clear And Does Not Require Construction

62. Patent Owner argues that Petitioners have "offered no evidence of the proper construction of ***'generating'*** as it appears in claim 4" and, therefore "they cannot show by a preponderance of the evidence that Ham discloses at least the 'generating' step of claim 4." (Paper 20, Response at 3 and 28). This argument does not make sense. The term "generating" is readily understood by a person of ordinary skill in the art. As such, there is no reason to rephrase or restate this term in an alternative language.

63. Neither the Patent Owner, Mr. Bohannon, nor Petitioner proposes a construction of this term. As such, there is no dispute as to its meaning. In fact, Mr. Bohannon confirmed during his deposition that the term "generating," as used in the '843 Patent, is clear:

> Q ... [A]re you offering any -- any specific construction for "generating"?
> THE WITNESS: ***No. I think the patent is pretty clear***, in that -- and in the figures and the description pretty much cover "generating." . . .

(Ex. 1009, Bohannon Tr. 88:16-90:8).

64. I agree that the term "generating" is clear to a person of ordinary skill in the art and requires no further construction.

ii. Patent Owner and Mr. Bohannon Do Not Consider Petitioners' Arguments

65. Patent Owner and Mr. Bohannon argue that the Petition "looks ***solely*** to [Ham's] ***data modulator 52*** for 'generating a plurality of data impulses for each pixel within every frame period according to the frame data' feature of claim 4." (Paper 20, Response at 12).

66. Based upon my review of the Petition, I disagree with their contention. The Petition relies on Ham's entire driving circuit (e.g., as shown in Figure 5), including data driver 53, for the generating step. (*See, e.g.,* Paper No. 1, Petition at

45-47 citing Ex. 1005, Ham, Figs. 5 and 7B; *id.* at 48 citing Ex. 1005, Ham ¶¶ 40, 41 and 53).

67. Patent Owner made a similar argument in its Preliminary Response, where Patent Owner argued that the Petition relies ***solely*** on Ham's timing controller 51 to satisfy the "generating" limitation. (Paper 9, Prelim. Resp. at 35). The Board rejected this argument:

> ***Patent Owner*** . . . argues that the normal RGB data is not disclosed as ***"generated" by timing controller 51.*** ... ***Petitioner did not rely on*** the Figure 5 timing controller 51 ***alone*** to meet the limitation. Rather, ***we understand Petitioner to rely on the driving apparatus, for example of Figure 5,*** which is not limited to the timing controller 51, as generating the two data impulses as claimed. *See* Pet. 48, citing Ex. 1005 ¶¶ 40, 41, 53.

(Paper 10, Decision at 13). I agree with the Board. Petitioner has relied upon Ham's entire driving apparatus (e.g., timing controller 51, data modulator 52, line memory 59, switch 58, data driver 53 and gate driver 54) as functioning together to generate two data impulses (i.e., modulated data voltage and normal data voltage), as required by Claim 4.

iii. Patent Owner's Data Modulator Arguments Are Wrong

68. Patent Owner further asserts that Petitioners' "universe of theories of unpatentability is limited to one: that Ham's ***Data Modulator 52 generates the***

normal data RGB that is received by timing controller 51." (Paper 20, Response at 13; *see also id.* at 27). This argument does not appear in the Petition.

69. Patent Owner's argument regarding the digital "normal RGB data" (a digital signal) may have been drawn from a sentence on Page 46 of the Petition that states:

> The apparatus also includes a "timing controller 51" that "receives digital video data" and a "data modulator 52" that generates ***two data impulses*** (i.e., "modulated data" signal and "normal data" signal) for each pixel within one frame period.

(Paper 1, Petition at 48).

70. This sentence does not mention or relate to "normal data RGB." Rather, it merely explains that Ham's "apparatus" generates two "data impulses" for each pixel in one frame period. The "data impulses" referred to in this sentence are the two analog voltages applied to the pixels though the data lines (i.e., the output of the driving circuit to the LCD Panel). Since these voltages are analog signals, they cannot be the same as the digital "normal data RGB" signals. Mr. Bohannon agrees that output to data lines 55 is analog. (Ex. 1009, Bohannon Tr. 114:3-12).

71. I note that Patent Owner's and Mr. Bohannon's arguments ignore the claim charts that appear on pages 47-49 of the Petition. This is evident from Patent

Owner's argument that "Petitioners are improperly looking to the ***same data*** being received by the timing controller 51 to satisfy both of the separate elements of 'receiving' and 'generating' of claim 4." (Paper No. 20, Response at 30). Petitioners' claim charts (reproduced in relevant part below) demonstrate otherwise:

the method comprising: receiving continuously a plurality of frame data;	The method includes continuously "receiv[ing] digital video data." (*E.g.*, Ex. 1005, Ham, ¶¶ [0003], [0037], Fig. 5).
generating a plurality of data impulses for each pixel within every frame period according to the frame data; and	The method includes generating two data impulses (i.e., "modulated data" and "normal data") for each pixel "within one frame period." (E.g., ¶¶ [0040]-[0041], ¶ [0053] ("[T]he LCD drive apparatus and method according to the present invention appl[ies] the normal data to the liquid crystal panel at the initial half period of the frame after supplying of the modulated data to the liquid crystal panel during the later half period of the frame . . . . ").

(Paper 1, Petition at 48) (annotated in yellow).

72. With respect to the "receiving" step, the chart identifies the "***digital video data***" input to Ham's driving circuit (*see* Paragraph 37 and Figure 5 (item 51) of Ham, both cited in the claim chart). In connection with the "generating" step, the chart refers to completely different data—"two data ***impulses***," which, as discussed above, are the ***analog*** signals output from Ham's driving circuit. (Paper 20, Response at 14; Ex. 1005, Ham, ¶41).

73. Mr. Bohannon agreed that Ham teaches the use of different data for the receiving and generating steps:

> Q Okay. So is it correct that the initial ***data coming into timing controller*** is ***digital***?
>
> A It says ... it was from a digital video -- digital video card.
>
> Q And ***the output*** into data lines 55 ***is analog***; correct?
>
> A Yeah. So let's be clear. Yeah, ***converted into analog data*** and applied to the data lines, yep.

(Ex. 1009, Bohannon Tr. 114:3-12).

74. With respect to the portions of Ham cited in Petitioners' claim charts in connection with the "generating" limitation (i.e., ¶¶40, 41 and 53), Patent Owner and Mr. Bohannon state that they only searched for the word "generating" in these paragraphs. (*See, e.g.*, Ex. 1009, Bohannon Tr. 101:16-102:4 ("***hardly*** anywhere in the Ham patent ***is the word 'generating' used.***"); *see also* Paper 20, Response at 12 ("[T]he ***only instance of*** Ham using the term ***'generating'*** in [Paragraphs 40, 41 and 53] appears in a discussion related to the gate driver 54."); *id.* at 37-38 n.5).

75. As stated above, it is my understanding that it is not necessary for a prior art reference to use identical terminology as in the claim in order for that claim to be anticipated. In this regard, as also discussed above, Ham's driving circuit receives a single digital data value and generates two analog data impulses.

76. Moreover, Paragraph 40 of Ham (cited in the Petition) uses the term "generating" in connection with its driving circuit. Specifically, Ham teaches a gate driver 54 for "***generating*** a scanning pulse." (*See* Ex. 1005, Ham ¶40). As Ham correctly explains, "in response to the scanning pulse," "[t]he TFT is turned on . . . to apply video data on the data lines 55 to the pixel electrode of the liquid crystal cell Clc." (*Id.*). This scanning pulse is critical to the operation of Ham's driving circuit. Ham's driving circuit would not function at all without "generating a scanning pulse," let alone output two data impulses in a frame.

77. In summary, Patent Owner appears to ignore Petitioners' actual positions relating to the "generating" step.

C. Limiting Claim 4 To Overdriving Cannot Be The Broadest Reasonable Construction

78. Claim 4 requires "applying ***the data impulses*** to the liquid crystal device of one of the pixels within one frame period via the data line connected to the pixel ***in order to control a transmission rate*** of the liquid crystal device of the pixel." Patent Owner attempts to modify this limitation to further require the application of "two or more ***overdriven*** data impulses in order to control a transmission rate of the liquid crystal device, or ***overdriving.***" (Paper 20, Response at 25-26).

79. Claim 4 is clear; it does not refer to "overdriven" data impulses or the "overdriving" step included in Claim 1. Rather, Claim 4 simply requires applying

"data impulses" in order to ***"control a transmission rate."*** In contrast to Claim 4, independent Claim 1 (which is not under review) explicitly requires overdriving:

Claim 1	Claim 4
... generating a plurality of ***overdriven*** pixel data within every frame period for each pixel;	generating a plurality of data impulses for each pixel within every frame period according to the frame data; ...

80. Mr. Bohannon agrees:

> Q Right. And -- and am I correct that those same words -- that is, "generating a plurality of overdriven pixel data" -- do not appear in Claim 4?
> THE WITNESS: Yes, those words do not appear in Claim 4.

(Ex. 1009, Bohannon Tr. 82:13-18). Given that Claim 4 does not refer to overdriving and Claim 1 explicitly refers to this concept, limiting Claim 4 to overdriving simply cannot be the broadest reasonable construction. Patent Owner's proposed construction would render the "overdriving" term in Claim 1 superfluous.

81. In addition, Mr. Bohannon testifies that the support for his construction was the ***language of Claim 1***, and ***not Claim 4***: "If I read ***Column 6, Line 15 [i.e., Claim 1]***... it says, generating a plurality of data impulses according

to a plurality of overdriven pixel data." (Ex. 1009, Bohannon Tr. 81:6-82:10; *see also id.* at 82:23-83:11 (relying on the same language)).

82. Mr. Bohannon also repeatedly cited Column 2, lines 33-48 of the "Summary of the Invention":

> Q . . . Could you just tell me where it says that you need to apply a plurality of overdriven pulses?
>
> A ***I think that at Column 2 is a good spot.*** So -- so, anyway -- so if we start around -- ***around line 40***, so it says (as read):
>
> > So a source driver generating a plurality of data pulses according to the plurality of overdriven pixel data generated by the blur clear converter and applying those to the -- to the liquid crystal device via the scan line, et cetera, in order to control the transmission rate.
> >
> > So -- so ***this is where I think it's saying that the plurality of overdrive --- driven pulses controls the transmission rate.***

(*Id. at* 127:2-22; *see also id.* at 73:7-15 (relying on Col. 2:40 of the '843 Patent); *id.* at 36:5-19, 37:4-18, 61:18-63:5, 86:22-88:1 (relying on similar passages in the '843 Patent). But these passages merely repeat the text of Claim 1, and do not track the language of Claim 4. (*Compare* Ex. 1001, '843 Patent, Col. 2:33-48, *with id.* at Col. 6:7-24). Notably, Mr. Bohannon did not cite the other, more relevant,

portions in the Summary of the Invention (i.e., Column 2, lines 19-32) that do repeat the language in Claim 4. (*Compare id.* at Col. 2:19-32, *with id.* Col. 7:1-19). These passages do not refer to overdriving and actually confirm that overdriving is not required in Claim 4.

83. There is no clear or deliberate definition of "overdriving" in the '843 Patent. Patent Owner argues that the applying step in Claim 4 "***recalls*** the discussion of 'overdriven' according to the '843 specification," and that there is some "correlation" between overdriving and controlling the transmission rate. (Paper No. 20, Response at 21, 25; *see also* Ex. 2005, Bohannon Decl. ¶12).

84. As discussed above, the '843 Patent provides multiple solutions to the problem of the blurring of video images in an LCD panel. (*See* Supra §III above). One solution is applying two or more data impulses to a pixel within a given frame. This concept is described numerous times in the '843 Patent without any reference to overdriving. Specifically, the Abstract recites:

> A method for driving a liquid crystal display (LCD) panel includes receiving continuously a plurality of frame data, generating a plurality of data impulses for each pixel every frame period according to the frame data, and applying the data impulses to a liquid crystal device of a pixel within a frame period via the data line connected to the pixel in order to control a transmission rate of the liquid crystal device.

(Ex. 1001, '843 Patent, Abstract).

85. The "Field of the Invention," likewise, only mentions the application of two (or more) data impulses to a pixel within a frame period:

> The invention relates to a driving circuit of a liquid crystal display (LCD) panel and its related driving method, and more particularly, to a driving circuit for ***applying over two data impulses*** to a pixel electrode within one frame period, and its related driving method.

(*id.* at Col. 1:7-12; *see also id.* at Col. 5:45-55 (summarizing invention and not mentioning overdriving)).

86. I have also been informed that, since Claim 4 is an original claim (i.e., it was part of the disclosure when the patent was filed) it is also part of the specification. Claim 4 plainly includes an embodiment that does not require overdriving.

87. As also discussed above, another solution to the blurring problem in the '843 Patent is applying two or more data pulses in combination with overdriving. (Paper 1, Petition at 12-13). As discussed above, according to the '843 Patent, the combination of these two techniques reduces blurring by decreasing the amount of time required for a pixel to transition from one gray level to another. (*Id.* at 13). Claim 1, and not Claim 4, covers this combination.

88. Mr. Bohannon correctly recognizes that, in all of the embodiments in the '843 Patent that include overdriving, that function is performed by a "blur clear converter." (Ex. 2005, Bohannon ¶14-21). But Mr. Bohannon does not address the fact that this element is recited in Claim 1, not Claim 4.

1. The '843 Patent Does Not Equate Controlling Transmission Rates With Overdriving

89. Patent Owner and Mr. Bohannon also argue that the reference to "control[ling] a transmission rate" in Claim 4 also requires overdriving to be read into Claim 4. In connection with this argument, Patent Owner incorrectly asserts that there is no way to "control the transmission rate" of a pixel without using an overdriving technique. (*See, e.g.*, Paper No. 20, Response at 26 (stating that the "non-overdriven scenario . . . does not control the transmission rate . . . ")). Patent Owner is mistaken.

90. The '843 Patent specification describes an LCD panel where the "transmission rate" was controlled ***without overdriving***. (Ex. 1001, '843 Patent, Col. 1:53-2:2). For example, Figure 2 of the '843 Patent plots "transmission rate" (vertical axis) versus time (horizontal axis). The '843 Patent explains that "[t]he curve C1 shows the ***transmission rate*** of a pixel ***not overdriven***." (*Id.* at Col. 1:57-60). By contrast, curve C2 shows the transmission rate of a pixel that is overdriven. As such, the '843 Patent recognizes that the term "transmission rate" is not synonymous with overdriving.

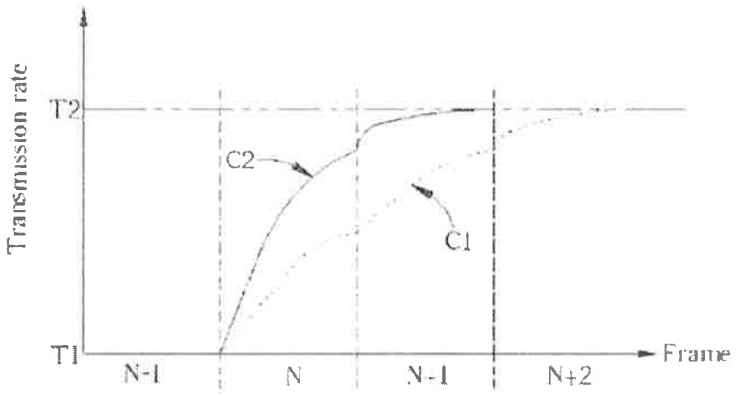


Fig. 2 Prior art

91. Further, Mr. Bohannon testified that he was unfamiliar with the term "transmission rate" until he saw this term in the '843 Patent, and that he has no opinion as to its meaning. (Ex. 1009, Bohannon Tr. 22:13-15 ("Q: And before you--you encountered the Shen '843 Patent had you heard that term used before? A: No."); 28:13-19 ("Q ... Are you offering an opinion on transmission rate? A I'm not offering an opinion on transmission rate.")). In fact, Mr. Bohannon believes that "transmission rate" is not a term of art and that the inventors on the '843 Patent coined this term:

> Q Okay. Is it fair to say the transmission rate of a pixel is the percentage of light that it allows to pass through?
>
> THE WITNESS: I'm -- I don't think I can answer that. I don't think I can say whether it's fair or not fair. I mean, it's -- ***this is the terminology that he's described here.***

(Ex. 1009, Bohannon Tr. 27:4-11).

92. Mr. Bohannon is incorrect. "Transmission rate" is a well known term and concept in the LCD and optics arts, and used in many prior art references. As noted above, the "transmission rate" of a pixel simply indicates the percentage of light from the display panel's backlight that passes through each pixel. (*See* Supra §III). A search of the art confirms that this is the case. (*See, e.g.*, Ex. 1012, U.S. 5,402,143, Col. 10:22-24 (describing prior art panel in which "the ***transmission rate*** of the LCD therein is ***proportional to analog input signals.***") and Ex. 1013, U.S. 6,538,647, Col. 4:64-68 (explaining that, in a normally black LCD display, "***driving voltage***" is directly related to the "optical ***transmission rate***")).

93. In any event, based upon a correct understanding of "transmission rate," "***control[ling]*** a transmission rate" merely refers to applying a particular voltage (or potential difference) to a pixel's electrodes. As discussed above, this is part of the basic operation of ***every*** LCD drive circuit, irrespective of the type of display or whether or not "overdriving" is used. Here again, the literature includes multiple references teaching LCD panels where a transmission rate is controlled without overdriving. (*See* Ex. 1014, U.S. 5,608,556, Col. 2:30-33 ("In each opening 201, ***the transmission rate of light is controlled*** to provide the desired display…") and Ex. 1012, U.S. 5,402,143, Col. 4:15-22 (explaining that, in a "simple matrix type conventional LCD" display, "***the scanning and data signals***

together control the transmission rate of each pixel of light passing therethrough")).

94. When asked whether there are any ways of "controlling the percentage of light that is passed through an ... active matrix liquid crystal display" (i.e., controlling a transmission rate), "other than overdriving," Mr. Bohannon admitted that "there's so many different ways," including "assorted drive methods." (Ex. 1009, Bohannon Tr. 28:20-29:8). I agree with Mr. Bohannon. For example, one could control the transmission rate by applying two or more data impulses in a single frame, as discussed with respect to C1 in Figure 2 of the '843 Patent.

95. In summary, the Patent Owner's and Mr. Bohannon's arguments for incorporating the concept of "overdriving" into Claim 4 have no technical merit.

I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true. I further declare that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of the Title 18 of the United States Code.

Dated: September 10, 2015

By: Michael J. Marentic

Michael J. Marentic

US007202843B2

(12) **United States Patent**
Shen et al.

(10) **Patent No.: US 7,202,843 B2**
(45) **Date of Patent: Apr. 10, 2007**

(54) **DRIVING CIRCUIT OF A LIQUID CRYSTAL DISPLAY PANEL AND RELATED DRIVING METHOD**

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(73) Assignee: **Vastview Technology Inc.**, Hsin-Chu (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 602 days.

(21) Appl. No.: **10/707,741**

(22) Filed: **Jan. 8, 2004**

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(30) **Foreign Application Priority Data**

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(51) **Int. Cl.**
G09G 3/36 (2006.01)

(52) **U.S. Cl.** **345/87**; 345/89

(58) **Field of Classification Search** 345/87, 345/88, 89, 90, 91, 93, 98, 99, 100, 204, 345/589, 596, 600–605
See application file for complete search history.

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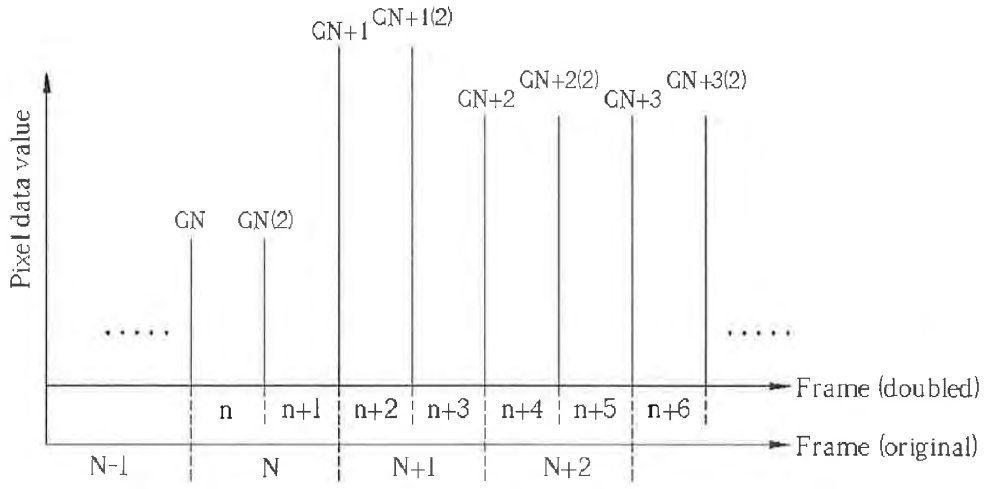
Primary Examiner—Nitin Patel
(74) *Attorney, Agent, or Firm*—Winston Hsu

(57) **ABSTRACT**

A method for driving a liquid crystal display (LCD) panel includes receiving continuously a plurality of frame data, generating a plurality of data impulses for each pixel every frame period according to the frame data, and applying the data impulses to a liquid crystal device of a pixel within a frame period via the data line connected to the pixel in order to control a transmission rate of the liquid crystal device.

9 Claims, 10 Drawing Sheets



SHARP EXHIBIT 1001

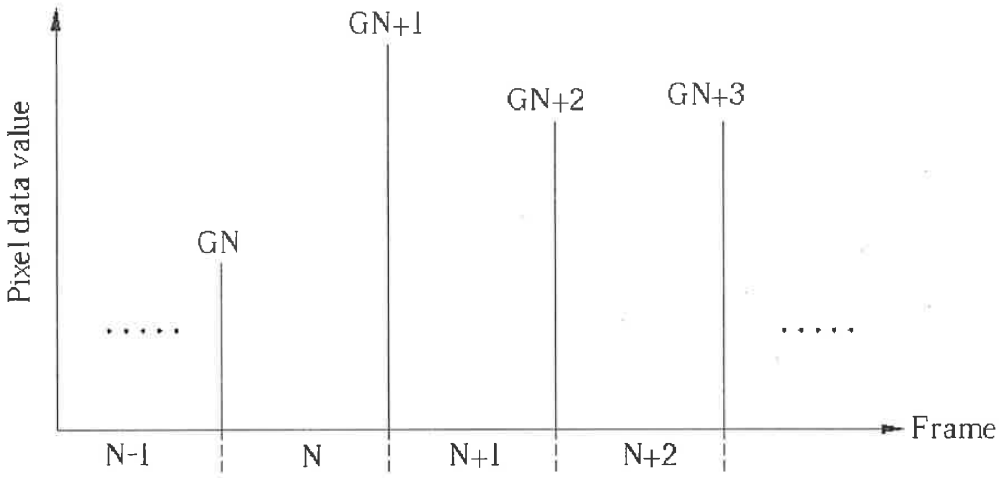


Fig. 1 Prior art

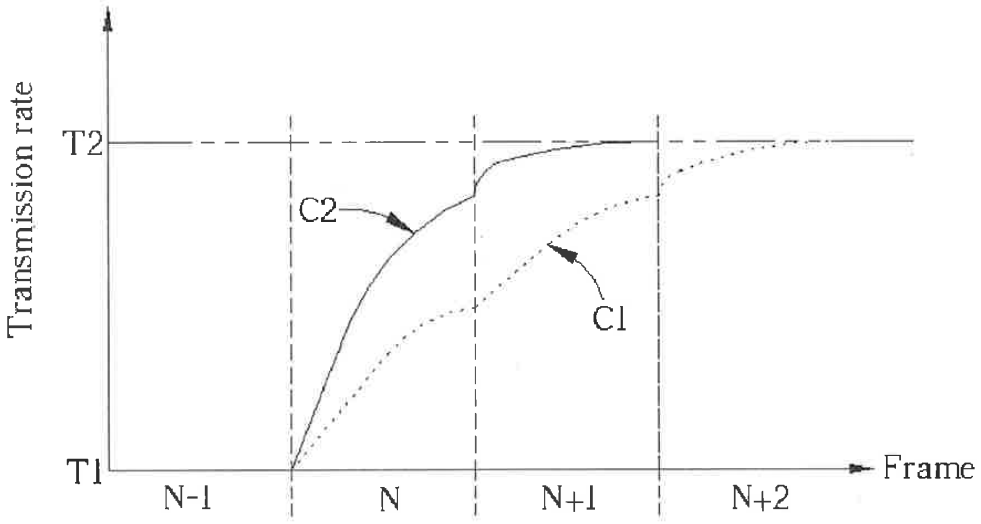


Fig. 2 Prior art

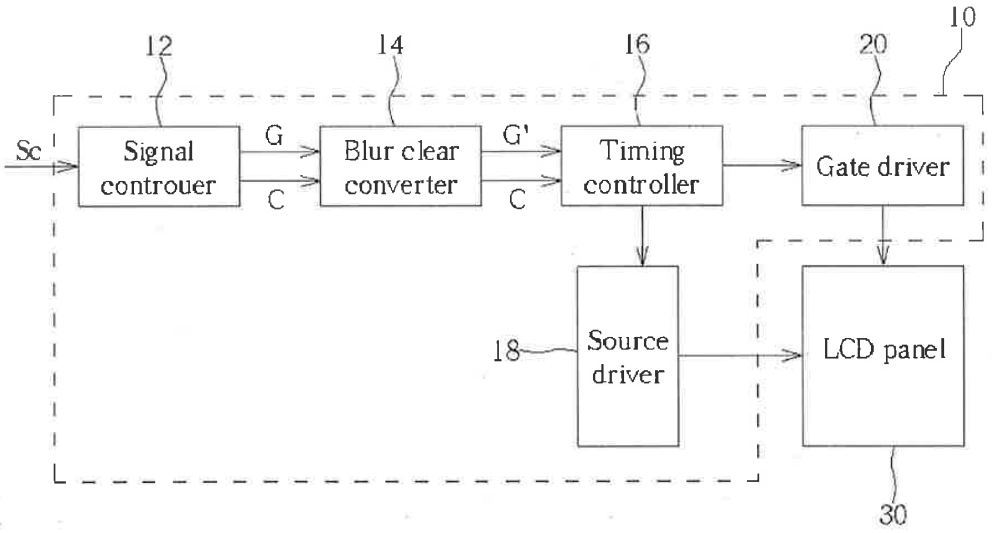

10
12
14
16
20
Sc
Signal controuer
G
C
Blur clear converter
G'
C
Timing controller
Gate driver
18
Source driver
LCD panel
30

Fig. 3

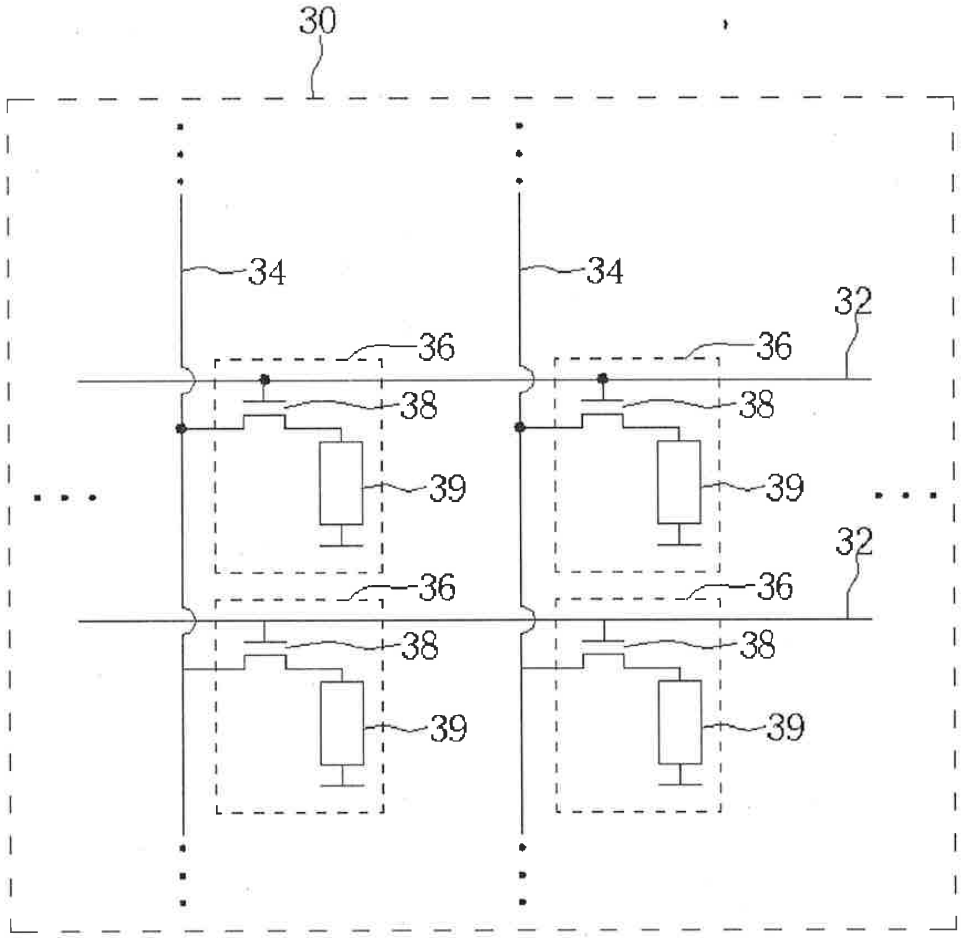


Fig. 4

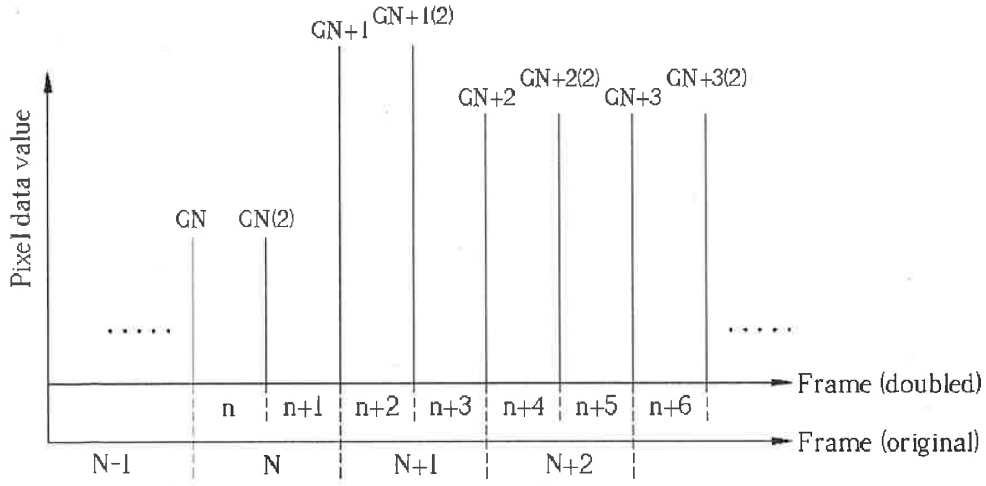

Pixel data value
GN
GN(2)
GN+1
GN+1(2)
GN+2
GN+2(2)
GN+3
GN+3(2)
Frame (doubled)
n
n+1
n+2
n+3
n+4
n+5
n+6
Frame (original)
N-1
N
N+1
N+2

Fig. 5

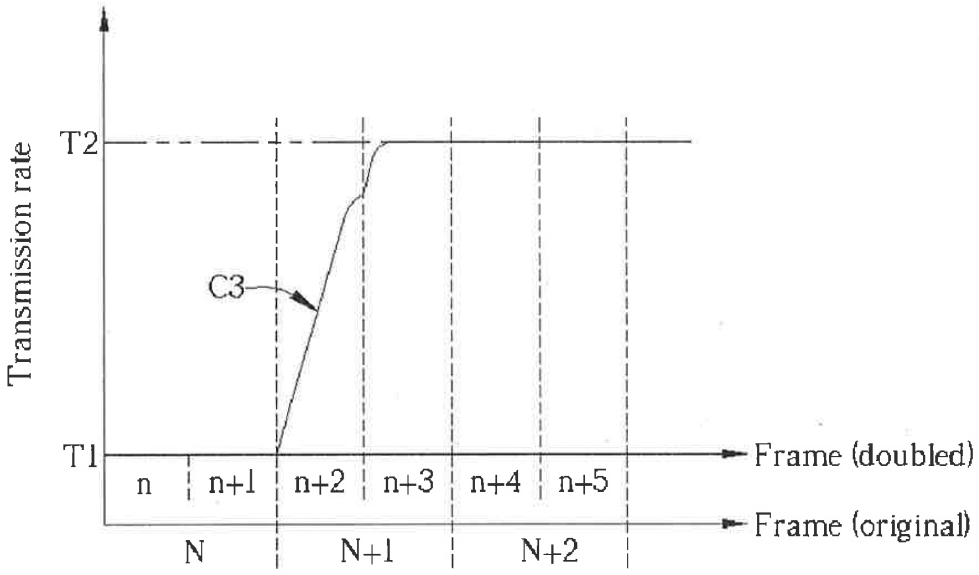

Transmission rate
T2
T1
C3
n
n+1
n+2
n+3
n+4
n+5
N
N+1
N+2
Frame (doubled)
Frame (original)

Fig. 6

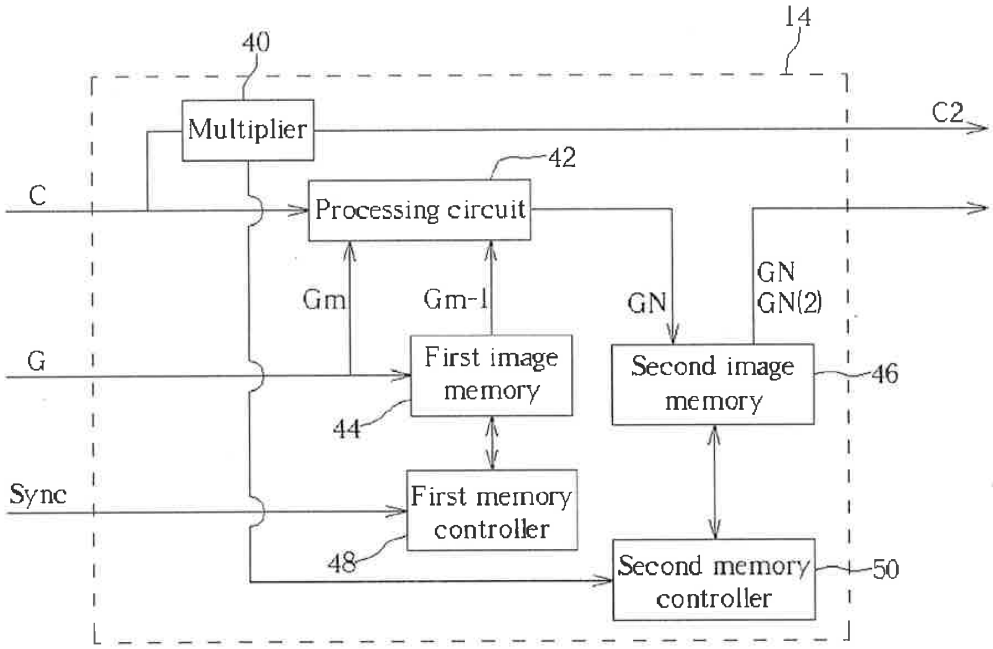

14
40
Multiplier
C2
42
C
Processing circuit
Gm
Gm-1
GN
GN
GN(2)
G
First image memory
Second image memory
46
44
Sync
First memory controller
48
Second memory controller
50

Fig. 7

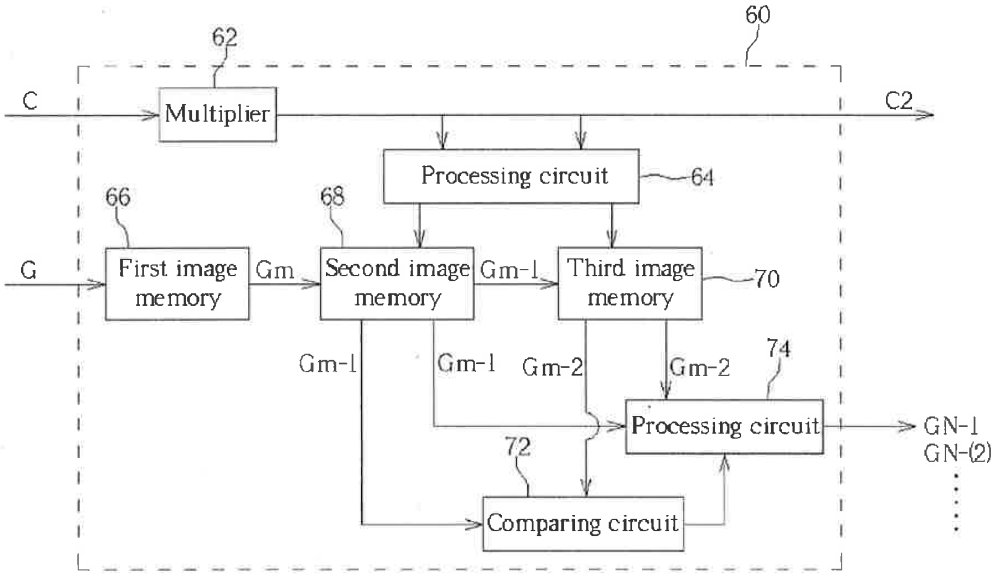

60
62
C
Multiplier
C2
Processing circuit
64
66
68
G
First image memory
Gm
Second image memory
Gm-1
Third image memory
70
Gm-1
Gm-1
Gm-2
Gm-2
74
Processing circuit
GN-1
GN-(2)
72
Comparing circuit

Fig. 8

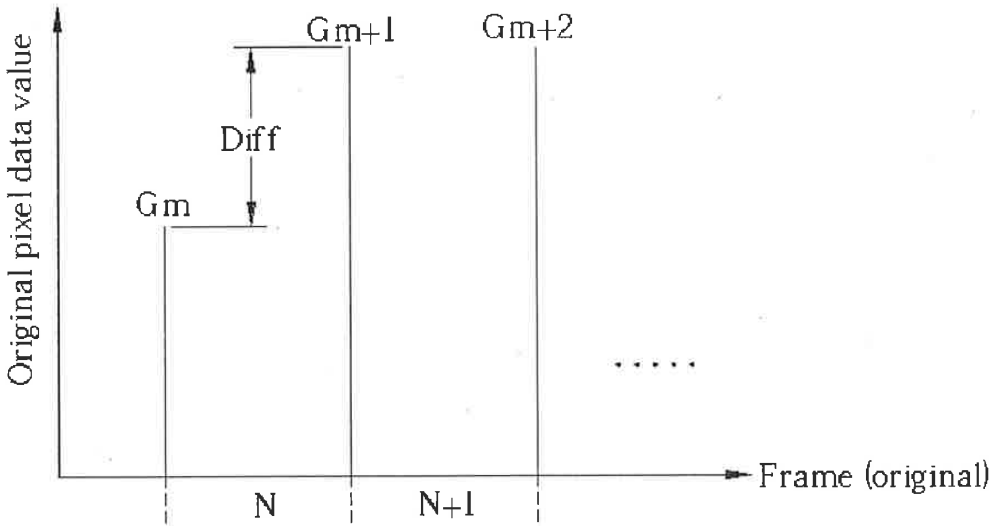


Fig. 9

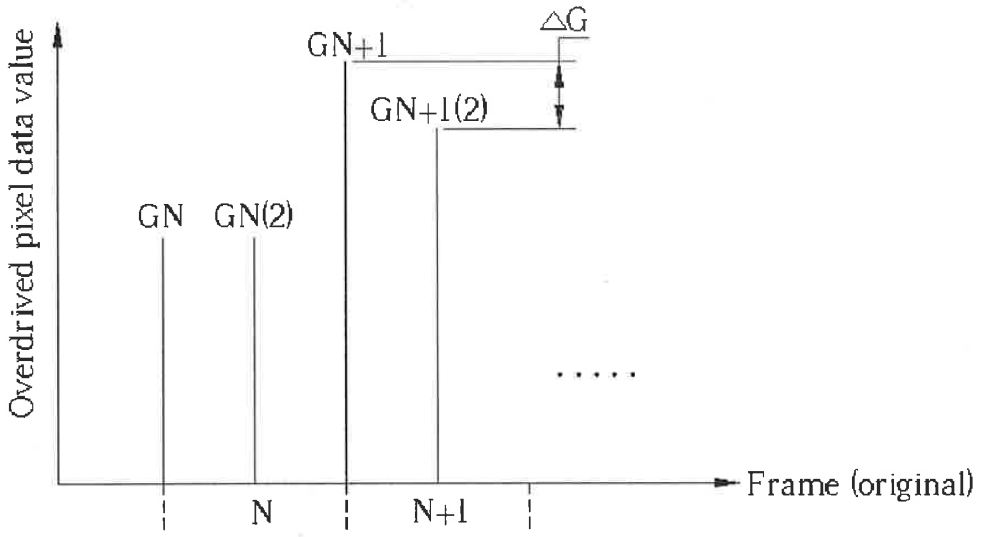

Overdrived pixel data value
GN
GN(2)
GN+1
GN+1(2)
△G
.....
Frame (original)
N
N+1

Fig. 10

DRIVING CIRCUIT OF A LIQUID CRYSTAL DISPLAY PANEL AND RELATED DRIVING METHOD

BACKGROUND OF INVENTION

1. Field of the Invention

The invention relates to a driving circuit of a liquid crystal display (LCD) panel and its related driving method, and more particularly, to a driving circuit for applying over two data impulses to a pixel electrode within one frame period, and its related driving method.

2. Description of the Prior Art

A liquid crystal display (LCD) has advantages of lightweight, low power consumption, and low divergence and is applied to various portable equipment such as notebook computers and personal digital assistants (PDAs). In addition, LCD monitors and LCD televisions are gaining in popularity as a substitute for traditional cathode ray tube (CRT) monitors and televisions. However, an LCD does have some disadvantages. Because of the limitations of physical characteristics, the liquid crystal molecules need to be twisted and rearranged when changing input data, which can cause the images to be delayed. For satisfying the rapid switching requirements of multimedia equipment, improving the response speed of liquid crystal is desired.

Generally when driving an LCD, a driving circuit receives a plurality of frame data and then generates corresponding data impulses, scan voltages, and timing signals, according to the frame data, in order to control pixel operation of the LCD. Each of the frame data includes data for refreshing all of the pixels within a frame period; thus each of the frame data can be regarded as including a plurality of pixel data, and each of the pixel data is for defining the gray level that a pixel is required to reach within a frame period. In the general standard, each pixel can switch among 256 (2^8) gray levels, thus each of the pixel data is 8 bits in length.

Please refer to FIG. **1** showing a timing diagram of pixel data values varying in accordance with the frames. When driving a pixel, the driving circuit receives a plurality of pixel data used for driving the pixel in sequence. As shown in FIG. **1**, GN, GN+1, GN+2 are the pixel data received in frame periods N, N+1, N+2, and the driving circuit determines the gray level of the pixel in the frame periods N, N+1, N+2 according to the values of the pixel data GN, GN+1, GN+2. In general, the larger the value of the pixel data is, the larger the gray level is. The driving circuit generates a data impulse corresponding to a frame period according to the pixel data GN, GN+1, GN+2, and applies the pulse to a pixel electrode of the corresponding pixel to have the pixel be in the appropriate gray level as required within each frame period.

Please refer to FIG. **2** showing a timing diagram of different transmission rates of a pixel, varying in accordance with the frames. Two curves C1, C2 are measured when the driving circuit changes the transmission rate from T1 to T2 beginning at frame period N. The curve C1 shows the transmission rate of a pixel not overdriven corresponding to the frames, and the curve C2 shows the transmission rate of the pixel overdriven corresponding to the frames. The U.S. published application No. 2002/0050965 is one of the references of the conventional overdriving method. There is a time delay when charging liquid crystal molecules, so that they cannot twist at a predetermined angle at a predetermined transmission rate. As shown by the curve C1, in the case of not being overdriven, the transmission rate cannot reach a predetermined level in the frame period N but has to wait until the frame period N+2. Such a delay causes blurring. In order to improve that, some conventional LCD are overdriven, which means applying a higher or a lower data impulse to the pixel electrode to accelerate the reaction speed of the liquid crystal molecules, so that the pixel can reach the predetermined gray level in a predetermined frame period. As shown by the curve C2, in the case of being overdriven, although the reaction speed of the liquid crystal molecules is faster than in case of not being overdriven, the transmission rate has to wait until frame period N+1 to reach T2. Thus, the requirement of reaching T2 in the frame period N still remains unsatisfied.

SUMMARY OF INVENTION

It is therefore a primary objective of the claimed invention to provide a driving circuit of an LCD panel and its relating driving method to solve the problem mentioned above.

Briefly, the present invention provides a method for driving an LCD panel. The LCD panel includes a plurality of scan lines, a plurality of data lines, and a plurality of pixels. Each pixel is connected to a corresponding scan line and a corresponding data line, and each pixel includes a liquid crystal device and a switching device connected to the corresponding scan line, the corresponding data line, and the liquid crystal device. The method includes receiving continuously a plurality of frame data, generating a plurality of data impulses for each pixel in every frame period according to the frame data and applying the data impulses to the liquid crystal device of one of the pixels within one frame period via the data line connected to the pixel in order to control the transmission rate of the liquid crystal device of the pixel.

The present invention further provides a driving circuit for driving an LCD panel including a blur clear converter for receiving frame data every frame period, each frame data comprising a plurality of pixel data and each pixel data corresponding to a pixel, the blur clear converter delaying current frame data to generate delayed frame data and generating a plurality of overdriven pixel data in every frame period for each pixel; a source driver for generating a plurality of data impulses to each pixel according to the plurality of overdriven pixel data generated by the blur clear converter and applying the data impulses to the liquid crystal device of the pixel via the scan line connected to the pixel in order to control the transmission rate of the liquid crystal device; and a gate driver for applying a scan line voltage to the switch device of the pixel so that the data impulses can be applied to the liquid crystal device of the pixel.

These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

BRIEF DESCRIPTION OF DRAWINGS

FIG. **1** is a timing diagram of the pixel data values varying in accordance with the frames according to the prior art.

FIG. **2** is a timing diagram of different transmission rates of the pixel varying in accordance with the frames.

FIG. **3** is a block diagram of a driving circuit and an LCD panel according to the present invention.

FIG. **4** is a circuit diagram of the LCD panel.

FIG. **5** is a timing diagram of pixel data values varying in accordance with frames.

FIG. **6** is a timing diagram of the transmission rate of the pixel varying in accordance with the frames.

FIG. **7** is a block diagram of the blur clear converter according to the first embodiment of the present invention.

FIG. **8** is a block diagram of the blur clear converter according to the second embodiment of the present invention.

FIG. **9** is a timing diagram of original pixel data received by the blur clear converter varying in accordance with the frames.

FIG. **10** is a timing diagram of overdriven pixel data generated by the blur clear converter varying in accordance with the frames.

DETAILED DESCRIPTION

Please refer to FIG. **3** showing a block diagram of a driving circuit **10** and an LCD panel **30** according to the present invention. The driving circuit **10** is for driving the LCD panel **30**, which includes a signal controller **12**, a blur clear converter **14**, a timing controller **16**, a source driver **18**, and a gate driver **20**. The signal controller **12** is for receiving composite video signals Sc, which includes frame data and timing data for driving the LCD panel **30**, and processing the composite video signals Sc to separate them into frame signals G and control signals C. Subsequently, the blur clear converter **14** continuously receives the control signals C and the frame data included in the frame signals G and generates processed frame signals G including a plurality of overdriven data according to the frame data. The timing controller **16** controls the source driver **18** and the gate driver **20** according to the frame signals G and the control signals C so that the source driver **18** and the gate driver **20** generate corresponding data line voltages and scan line voltages according to the plurality of overdriven data included in the frame signals G in order to drive the LCD panel **30** to generate images corresponding to the composite video signals Sc.

Please refer to FIG. **4** showing a circuit diagram of the LCD panel **30**. The LCD panel **30** includes a plurality of scan lines **32**, a plurality of data lines **34**, and a plurality of pixels **36**. Each pixel **36** is connected to a corresponding scan line **32** and a corresponding data line **34**, and each pixel **36** has a switching device **38** and a liquid crystal device **39** a.k.a. a pixel electrode. The switching device **38** is connected to the corresponding scan line **32** and the corresponding data line **34**, and the source driver **18** and the gate driver **20** control the operation of each pixel **36** via the scan line **32** and the data line **34**. To drive the LCD **30**, scan voltages are applied to the scan lines **32** to turn on the switching devices **38**, and data voltages are applied to the data lines **34** and transmitted to the pixel electrodes **30** through the switching devices **38**. Therefore, when the scan voltages are applied to the scan lines **32** to turn on the switching devices **38**, the data voltages on the data lines **34** will charge the pixel electrodes **39** through the switch devices **38**, thereby twisting the liquid crystal molecules. When the scan voltages on the scan lines **32** are removed to turn off the switching devices **38**, the data lines **34** and the pixels **36** will disconnect, and the pixel electrodes **39** will remain charged. The scan lines **32** turn the switching devices **38** on and off repeatedly so that the pixel electrodes **39** can be repeatedly charged. Different data voltages cause different twisting angles and show different transmission rates. Hence, the LCD **30** displays various images.

Please refer to FIG. **5** showing a timing diagram of pixel data values varying in accordance with frames. According to the present invention, when driving any pixel **36** of the LCD panel **30**, the driving circuit **10** generates a plurality of pixel data used for driving the pixel in sequence. As shown in FIG. **5**, GN, GN(**2**), GN+1, GN+1(**2**), GN+2, GN+2(**2**), GN+3, GN+3(**2**) are the pixel data generated in frame periods N, N+1, N+2, N+3. The driving circuit **10** generates two pieces of pixel data for each pixel **36** in every frame period. The driving circuit **10** drives the pixel to reach gray levels in the frame periods N, N+1, N+2, N+3 according to the values of the pixel data GN–GN+2(**2**). For instance, when the pixel data GN, GN(**2**) are generated, the source driver of the driving circuit **10** converts the pixel data GN, GN(**2**) into two corresponding data impulses and then applies them to the liquid crystal device **39** via the data line **32** in the frame period N in order to control the transmission rate of the liquid crystal device **39**. Similarly, data impulses corresponding to the pixel data GN+1–GN+3(**2**) are applied respectively to corresponding pixel electrodes **39** every half a frame period. Same as the prior art, the larger the value of the pixel data is, the higher the voltage of the corresponding data impulse is, and the larger the gray level value is.

Please refer to FIG. **6** showing a timing diagram of the transmission rate of the pixel **36** varying in accordance with the frames. As described above, the driving circuit **10** generates two pieces of pixel data in each frame period, and then the source driver **18** generates two corresponding data impulses according to the two pieces of pixel data and applies them to the pixel electrode **39** of the corresponding pixel **36** in order to control the transmission rate and gray level of the pixel electrode **39**. As shown in FIG. **6**, the driving circuit **10** changes the transmission rate of the pixel electrode **39** of a pixel **36** from T1 to T2 in the frame period N+1. The pixel electrode **39** is applied with two data impulses corresponding to the pixel data GN+1, GN+1(**2**) in the frame period N+1 at a time interval of half a frame period. As shown in FIG. **6**, although the transmission rate of the pixel electrode **39** cannot reach T2 in the first half period n+2 of the frame period N+1, in the later half period n+3 of the frame period N+1, the pixel electrode **39** is applied with another data impulse, so that the transmission rate can reach T2 in the frame period N+1 as required. Therefore, blurring will not occur.

In the present embodiment, the two pieces of pixel data of each pixel in every frame period are generated by the blur clear converter **14**. Please refer to FIG. **7** showing a block diagram of the blur clear converter **14**. The blur clear converter **14** includes a multiplier **40**, a processing circuit **42**, a first image memory **44**, a second image memory **46**, a first memory controller **48**, and a second memory controller **50**. The multiplier **40** is for doubling the frequency of the control signal C to generate a multiplied signal C**2**. The first image memory **44** is controlled by the first memory controller **48** to delay current pixel data Gm for a frame period to generate delayed pixel data Gm–1 according to the control signal C. The processing circuit **42** generates a plurality of overdriven pixel data GN according to the current pixel data Gm and the delayed pixel data Gm–1. The second image memory **46** stores the overdriven pixel data GN, and the second memory controller **50** controls the second image memory **46** to output two overdriven pixel data GN, GN(**2**) to each pixel **36** within a frame period according to the multiplied signal C**2** in order to have the source driver **18** apply two data impulses to a specific pixel **36** within a frame period according to the two overdriven pixel data GN, GN(**2**).

Please refer to FIG. **8** showing a block diagram of the blur clear converter **60** according to the second embodiment of the present invention. The blur clear converter **60** functions the same as the blur clear converter **14**, which includes a

multiplier **62**, a first image memory **66**, a second image memory **68**, a third image memory **70**, a memory controller **64**, a processing circuit **74**, and a comparing circuit **72**. The multiplier **62** is for doubling the frequency of the control signal C to generate a multiplied signal C**2**. The first image memory **66** is for receiving and temporarily storing a plurality of pixel data G. The second image memory **68** delays the plurality of pixel data G for a frame period to generate delayed pixel data Gm−1. The third image memory **70** delays the pixel data Gm−1 for a frame period to generate delayed pixel data Gm−2. Thus the pixel data Gm−2 lags the pixel data Gm−1 for a frame period, and so does the pixel data Gm−1 with respect to the pixel data Gm. The memory controller **64** controls the second image memory **68** and the third image memory **70** to output two overdriven pixel data in each frame period according to the multiplied signal C**2**. The processing circuit **74** generates two pieces of overdriven pixel data GN**1**, GN−1(**2**) for each pixel **36** in every frame period according to the pixel data Gm−1, Gm−2. The comparing circuit **72** compares the pixel data Gm−1 with the pixel data Gm−2 to determine the values of the overdriven pixel data GN−1, GN−1(**2**).

Please refer to FIG. **9** showing a timing diagram of original pixel data received by the blur clear converter **60** varying in accordance with the frames, and FIG. **10** showing a timing diagram of overdriven pixel data generated by the blur clear converter **60** varying in accordance with the frames. As shown in FIG. **9**, the original pixel data received by the blur clear converter **60** in the frame periods N and N+1 are respectively Gm and Gm+1, with a difference Diff between each other. The blur clear converter **60** generates the two overdriven pixel data GN+1, GN+1(**2**) with a difference ΔG between each other according to the original pixel data Gm, Gm+1. The difference ΔG is determined by the comparing circuit **72** in FIG. **8** for driving the pixels **36** according to difference conditions. The difference ΔG is determined according to the difference Diff between the original pixel data Gm and Gm+1. For instance, when the difference Diff is less than a specific value, the comparing circuit **72** determines the difference ΔG as 0, that is equating the overdriven pixel data GN+1 to the overdriven pixel data GN+1(**2**). Or when the difference Diff is larger than a specific value, the comparing circuit **72** modulates the difference ΔG to drive the LCD panel **30** properly.

In contrast to the prior art, the present invention discloses a driving circuit and relating driving method to generate two pieces of pixel data in each frame period for every pixel on an LCD panel and then to generate two data impulses according to the two pieces of pixel data and to apply them to each pixel within a frame period in order to change the transmission rate of a pixel electrode. Thus, each of the pixels of the LCD panel is applied of a plurality of data impulses within a frame period, so that liquid crystal molecules of the pixels can twist to reach a predetermined gray level within a frame period, and blurring will not occur.

Those skilled in the art will readily observe that numerous modifications and alterations of the device and method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.

The invention claimed is:

1. A driving circuit for driving an LCD panel, the LCD panel comprising:

a plurality of scan lines;

a plurality of data lines; and

a plurality of pixels, each pixel being connected to a corresponding scan line and a corresponding data line, and each pixel comprising a liquid crystal device and a switching device connected to the corresponding scan line, the corresponding data line, and the liquid crystal device,

the driving circuit comprising:

a blur clear converter for receiving frame data every frame period, each frame data comprising a plurality of pixel data and each pixel data corresponding to a pixel, the blur clear converter delaying current frame data to generate delayed frame data and generating a plurality of overdriven pixel data within every frame period for each pixel;

a source driver for generating a plurality of data impulses to each pixel according to the plurality of overdriven pixel data generated by the blur clear converter and applying the data impulses to the liquid crystal device of the pixel via the scan line connected to the pixel within one frame period in order to control transmission rate of the liquid crystal device; and

a gate driver for applying a scan line voltage to the switch device of the pixel so that the data impulses can be applied to the liquid crystal device of the pixel.

2. The driving circuit of claim **1** wherein the blur clear converter further comprises:

a multiplier for multiplying a frequency of a control signal to generate a multiplied signal;

a first image memory for delaying the pixel data for a frame period;

a processing circuit for generating the plurality of overdriven pixel data according to the pixel data and the pixel data delayed by the first image memory;

a second image memory for storing the overdriven pixel data;

a memory controller for controlling the second image memory according to the multiplied signal to output the plurality of overdriven pixel data to any pixel so that the source driver generates the data impulses to each pixel within one frame period according to the overdriven pixel data output by the second image memory.

3. The driving circuit of claim **1** wherein the blur clear converter further comprises:

a multiplier for multiplying a frequency of a control signal to generate a multiplied signal;

a first image memory for receiving and temporarily storing the pixel data;

a second image memory for delaying the pixel data stored and output by the first image memory for a frame period;

a third image memory for delaying the pixel data stored and output by the second image memory for a frame period;

a memory controller for controlling the second image memory and the third image memory according to the multiplied signal;

a processing circuit for generating the plurality of overdriven pixel data according to the pixel data delayed and output by the second image memory and the third image memory; and

a comparing circuit for comparing the pixel data delayed by the second image memory with the pixel data delayed by the third image memory in order to determine data values of the overdriven pixel data generated by the processing circuit.

4. A method for driving a liquid crystal display (LCD) panel, the LCD panel comprising:

a plurality of scan lines;

a plurality of data lines; and

a plurality of pixels, each pixel being connected to a corresponding scan line and a corresponding data line, and each pixel comprising a liquid crystal device and a switching device connected to the corresponding scan line, the corresponding data line, and the liquid crystal device, and

the method comprising:

receiving continuously a plurality of frame data;

generating a plurality of data impulses for each pixel within every frame period according to the frame data; and

applying the data impulses to the liquid crystal device of one of the pixels within one frame period via the data line connected to the pixel in order to control a transmission rate of the liquid crystal device of the pixel.

5. The method of claim 4 further comprising:

delaying the frame data to generate a plurality of corresponding delayed frame data; and

comparing current frame data and corresponding delayed data to determine voltage values of the data impulses when generating the data impulses.

6. The method of claim 5 wherein the data impulses are a first data impulse and a second data impulse applied to the liquid crystal device of the pixel in sequence within the frame period.

7. The method of claim 6 further comprising:

determining a difference between the first data impulse and the second data impulse according to the current frame data and the corresponding delayed frame data.

8. The method of claim 4 further comprising:

applying a scan line voltage to the switch device of the pixel via the scan line connected to the pixel in order to have the data impulses be applied to the liquid crystal device of the pixel.

9. The method of claim 4 wherein each frame data comprises a plurality of pixel data, and each pixel data corresponds to a pixel.

* * * * *

MICHAEL J. MARENTIC

EDUCATION:
M.S. Degree - Electrical Engineering, University of Illinois
Thesis: Electron Density Measurements of an AC Plasma Panel Using Laser Interferometry.

B.S. Degree - Engineering Physics, University of Illinois

ORGANIZATIONS AND ACHIEVEMENTS:
Multiple Excellence Awards at QinetiQ
Testifying Expert Witness
President's Award at Hitachi America
Chairman VESA Board of Directors in 1997
Interstate Electronics Special Achievement Awards
Member of Society for Information Display since 1977

CAREER SUMMARY: Extensive industrial and theoretical experience in product engineering, system engineering, display electronics design, and device fabrication. Support various infrastructure groups with technology evaluations during acquisitions and equity position investment. Supported customers with application engineering and marketing with technical reports and assessments.

EXPERIENCE:

2002 – 2011 QINETIQ NORTH AMERICA – TECHNOLOGY SOLUTIONS GROUP
Company: Provider of innovative and cost-effective hardware solutions to US Government agencies. 600 employees

Principal Electronic Engineer for underwater submarine to aircraft laser communications; System and lead engineer for airborne multi-spectral imaging payload used for detection of land mine fields: Lead electrical and system engineer for medical device used for cervical cancer detection and treatment.

2001 – 2002 ALIEN TECHNOLOGY, Morgan Hill, California
Company: Start-up with unique low cost silicon packaging technology; 110 employees

Senior System Developer in IC Design team. Developed innovative LCD driver architecture for very low cost, mechanically flexible, ultra low power LCD.
Member of IC design team that designed first Nanoblock, modular OLED display driver.
Member of team that designed and manufactured first class 1, UHF, EPC Global protocol, passive RFID tag and reader.

1999 – 2001 PHILIPS COMPONENTS, Sunnyvale, California
Company: Multi-national component manufacturing conglomerate; 50,000 employees

Director of Engineering for new product creation business group. Projects include Video monitor design, large LCD TV, optical backlighting, and human interfaces.
Project timing was several months from concept to working prototypes.
Designs were documented and handed off to pertinent factory for volume manufacture.
Member of team that performed due diligence for acquisition of LG LCD.
Technical consultant to market development, venture capital investment, and CTO organizations.

1995 - 1999 HITACHI ELECTRONIC DEVICES (USA), INC., San Jose, California
Company: Sales and manufacturing subsidiary of Japanese conglomerate; 1,200 employees

Manager of small design group for flat panel monitors. Projects included LVDS, TMDS digital and analog video interfaces for LCD notebooks and monitors.
Liaison office between three Japanese LCD design departments and various partnered Silicon Valley companies.
Very active in Video Electronics Standards Association as chairman of Flat Panel Display Interface working group.
Wrote quarterly market and technical position report on video chips for LCD's.

1993 - 1995 SCIENCE APPLICATIONS INTERNATIONAL CORPORATION, San Diego, California
Company: Employee owned, technical services provider; 17,000 employees

Principal Engineer responsible for transfer of LCD backlight from prototype fabrication to high yielding production. Assignment areas included process engineer for phosphor deposition, UV lamp design and cathode engineering; device engineer for characterization of life, environmental operating window, optical efficacy;
System engineer for support of marketing group.

1987 - 1993 PLASMACO, INCORPORATED, Highland, New York
Company: Start-up using IBM's former plasma panel manufacturing line; 80 employees

Founder and Vice-president responsible for development, design, and manufacture of high voltage driver chip on glass technology. Responsible for all post clean room assembly, burn-in, characterization, yield management, and cost containment.
Managed purchasing, coordinated vendor contracts for PCB assembly, power supply procurement, and process equipment purchases.
Participated in business plan writing, obtaining financing, construction, start-up, and staffing of 65,000 sq. ft. factory.

1986 - 1987 SIGMATRON NOVA, INCORPORATED, Thousand Oaks, California
Company: Thin film electroluminescent manufacturer; 40 employees

Product Engineering Manager responsible for quick design and manufacture of custom TFEL displays. Characterized device failure modes and designed tolerant drive electronics to aid in long life displays.
One-third time accompanied Marketing Manager on trips to customers.

1985 - 1986 PLASMA DISPLAYS, INCORPORATED, Orange, California
Company: Consulting corporation

AT&T Technologies, Incorporated, Reading, Pennsylvania
Assisted Bell Laboratories with technical leadership to the development, design and manufacturing groups involved with transferring unique 3-Electrode per pixel plasma display from prototype to high volume production.

Data View, Incorporated, Champaign, Illinois
Designed and prototyped custom plasma display electronics and packaging in six months.

1979 - 1985 INTERSTATE ELECTRONICS CORPORATION, Anaheim, California
Company: Military contractor for US Navy; 1,800 employees

Engineer responsible for design, prototyping, and initial production of analog drive electronics in militarized plasma display terminal family; designing and documenting IEC's nuclear hardened display terminal; technical interface for procurement of electronic components and assemblies; liaison with other groups within company such as Quality Assurance, Manufacturing, and Parts Standards.

1977 - 1979 NCR CORPORATION, Electronic Display Systems, Colorado Springs, Colorado
Company: Manufacturing division for displays used in point of sale terminal; 60 employees

Specifying, designing, tooling, and scheduling of all new AC plasma panels; Process Engineer for vacuum backfill, overcoat application, and wet processing; principal Development Engineer for NCR second-generation plasma panels (shift type).

1973 - 1976 UNIVERSITY OF ILLINOIS, Coordinated Science Labs, Urbana, Illinois
Employer Profile: Multidiscipline laboratory where AC Plasma Panel was invented.

Design, construct and perform experiments leading to successful electron density and discharge activity measurements of a plasma panel.

PUBLICATIONS:

Plastic Film Displays with Nanoblock™ IC Drivers Integrated by Fluidic Self Assembly™ Process, Jacobsen, et al., SID 2002

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Brightness Control of the AC Plasma Panel; Suste and Marentic; SID. 1982

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Advanced Waveform Techniques for Plasma Display Panels, M.J. Marentic. U.S. Patent #4,415,892

Modular Waveform Generator for Plasma Display Panels, M.J. Marentic, D.A. Manseau. U.S. Patent #4,464,657

US005402143A

United States Patent [19]

Ge et al.

[11] Patent Number: 5,402,143

[45] Date of Patent: Mar. 28, 1995

[54] **COLOR FLUORESCENT LIQUID CRYSTAL DISPLAY**

[75] Inventors: **Shichao Ge**, Santa Clara; **Jemm Liang**, San Jose, both of Calif.

[73] Assignee: **Panocorp Display Systems**, Sunnyvale, Calif.

[21] Appl. No.: **245,454**

[22] Filed: **May 18, 1994**

Related U.S. Application Data

[63] Continuation of Ser. No. 812,730, Dec. 23, 1991, abandoned.

[51] **Int. Cl.**[6] **G09G 3/36**

[52] **U.S. Cl.** **345/102**; 345/75; 345/5

[58] **Field of Search** 345/4, 5, 74, 75, 102

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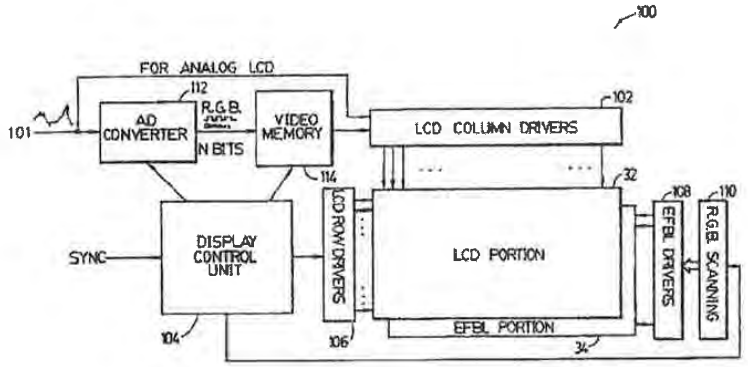
Primary Examiner—Jeffery Brier

Attorney, Agent, or Firm—Majestic, Parsons, Siebert & Hsue

[57] **ABSTRACT**

An electronic fluorescent device (EFD) is used as the back light source for a black/white LCD. Where the EFD provides red, green and blue light, the LCD displays multi-color or full-color images. The EFD includes a number of cathodes disposed in a vacuum chamber, an anode, phosphor strips near the anode, and grid electrodes for controlling the timing of the light generation and sequential color addressing. The control system may be such that the transmission rate of the LCD is proportional to the amplitude of the input signal forming an analog system; the EFD then simply provides sequential red, green and blue light pulses of constant intensity. Alternatively, selected pixels of the LCD may be addressed digitally to be either on or off, and the intensities of the red, green and blue pulses provided by the EFD are varied. In both instances, full scale gray tone monochromatic, multi-color or full-color images can be achieved.

40 Claims, 12 Drawing Sheets



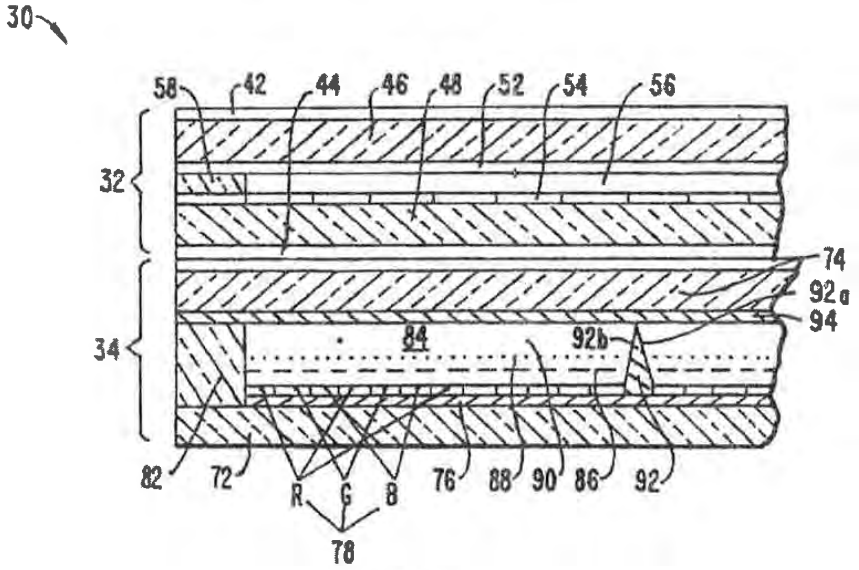


FIG. 1.

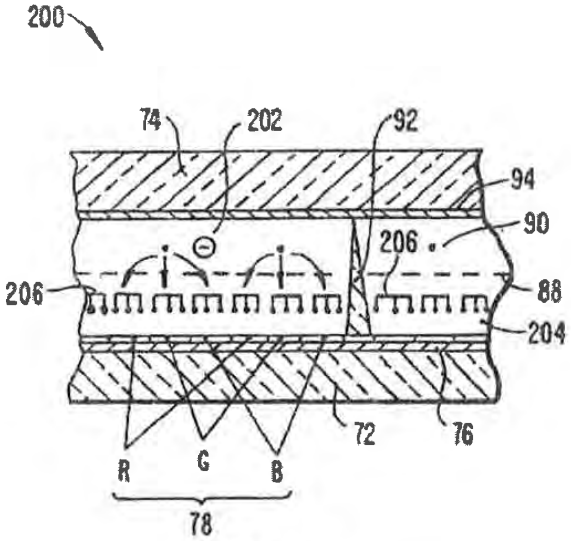


FIG. 5.

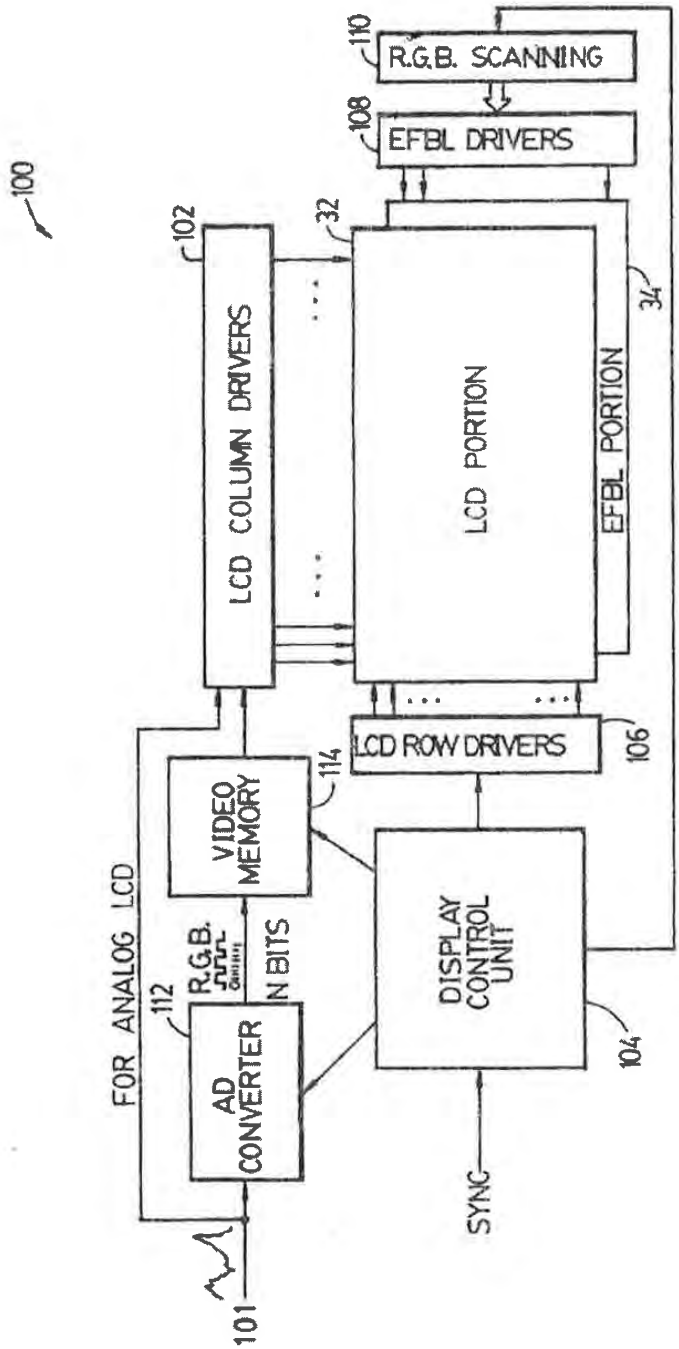

100
110
R.G.B. SCANNING
108
EFBL DRIVERS
102
LCD COLUMN DRIVERS
32
LCD PORTION
34
EFBL PORTION
LCD ROW DRIVERS
106
114
VIDEO MEMORY
R.G.B.
N BITS
112
AD CONVERTER
FOR ANALOG LCD
DISPLAY CONTROL UNIT
104
SYNC
101

FIG._2

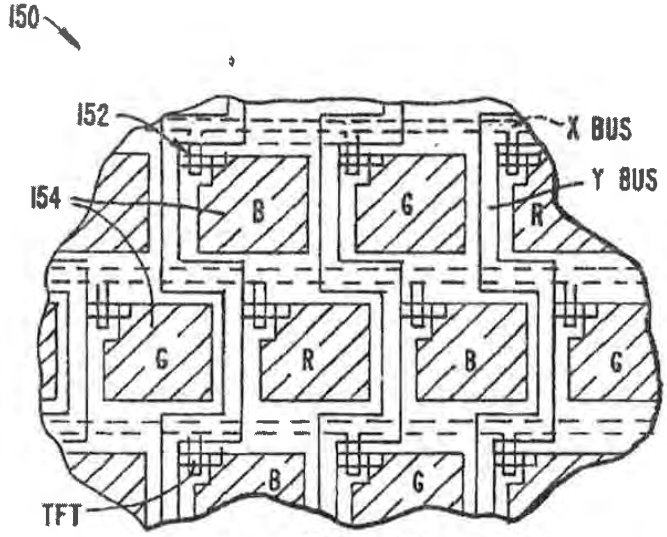


FIG. 3. PRIOR ART

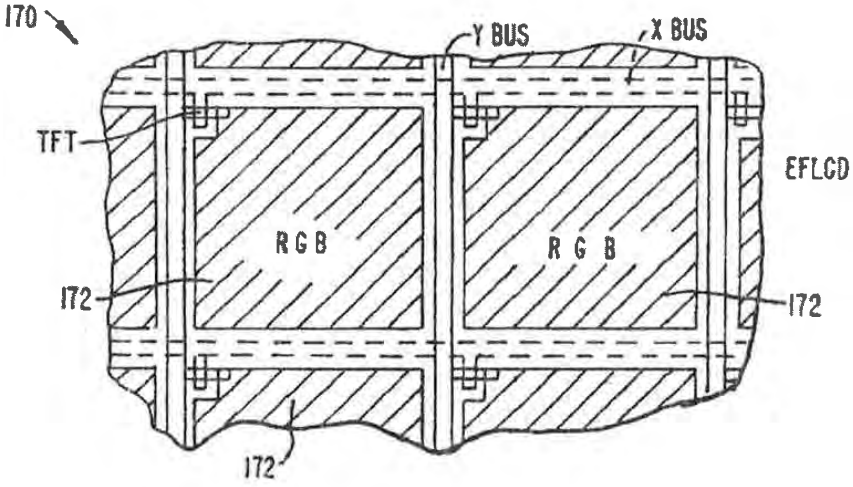


FIG. 4.

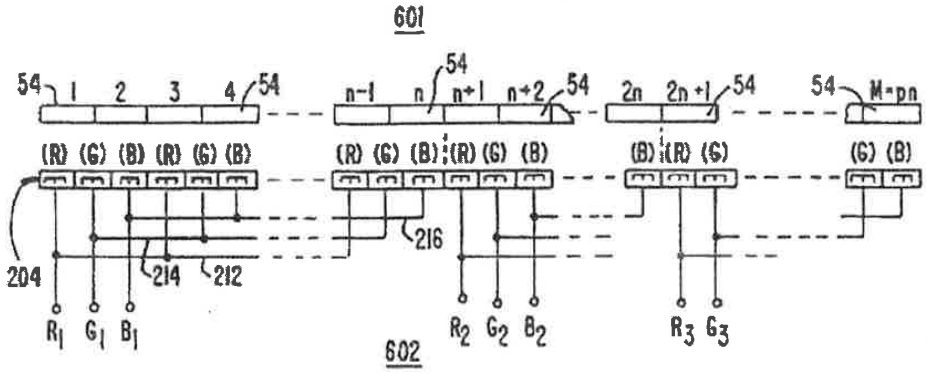

601
54
1
2
3
4
54
n-1
n
54
n+1
n+2
54
2n
2n+1
54
54
M=pn
(R) (G) (B) (R) (G) (B)
(R) (G) (B) (R) (G) (B)
(B) (R) (G)
(G) (B)
204
214
212
216
R1 G1 B1
R2 G2 B2
R3 G3
602

FIG. 6.

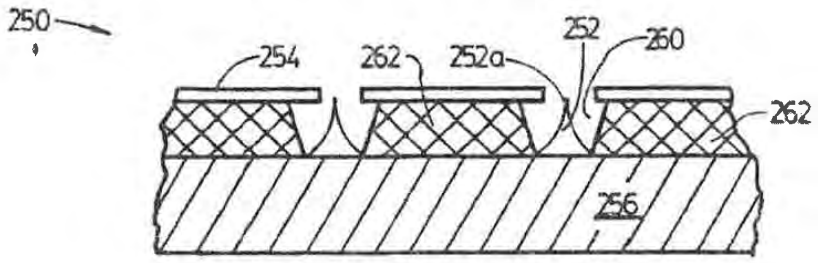


FIG. 7.

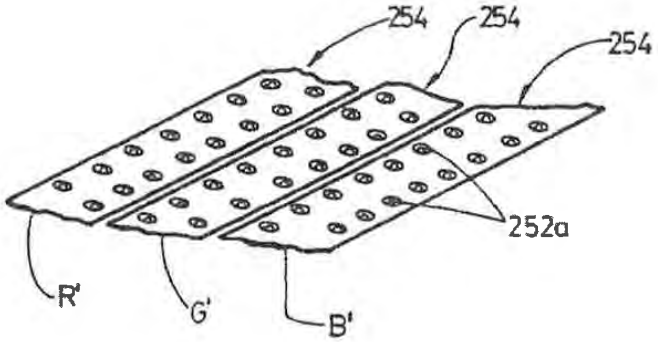


FIG. 8.

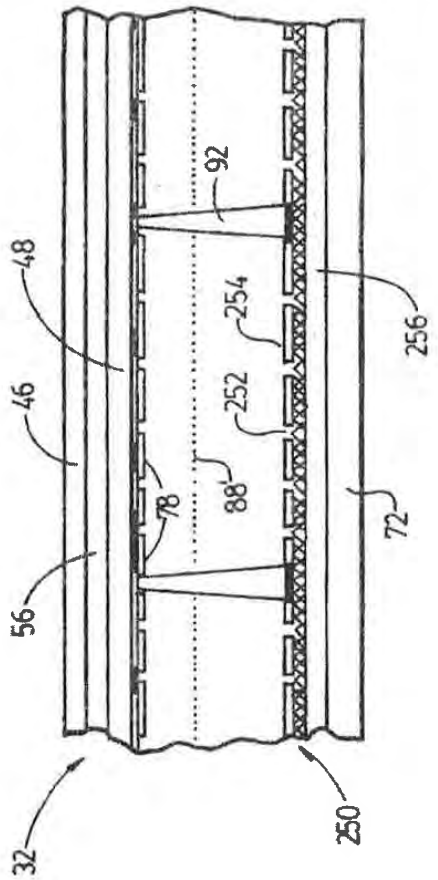


FIG. 9.

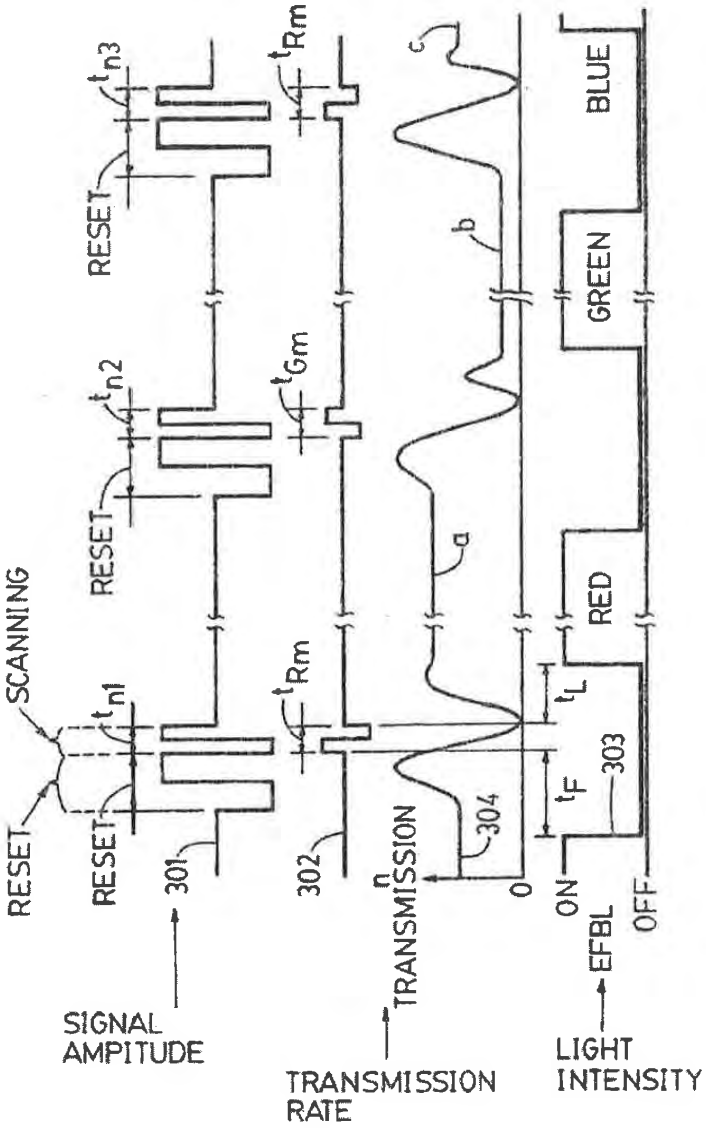


FIG._10.

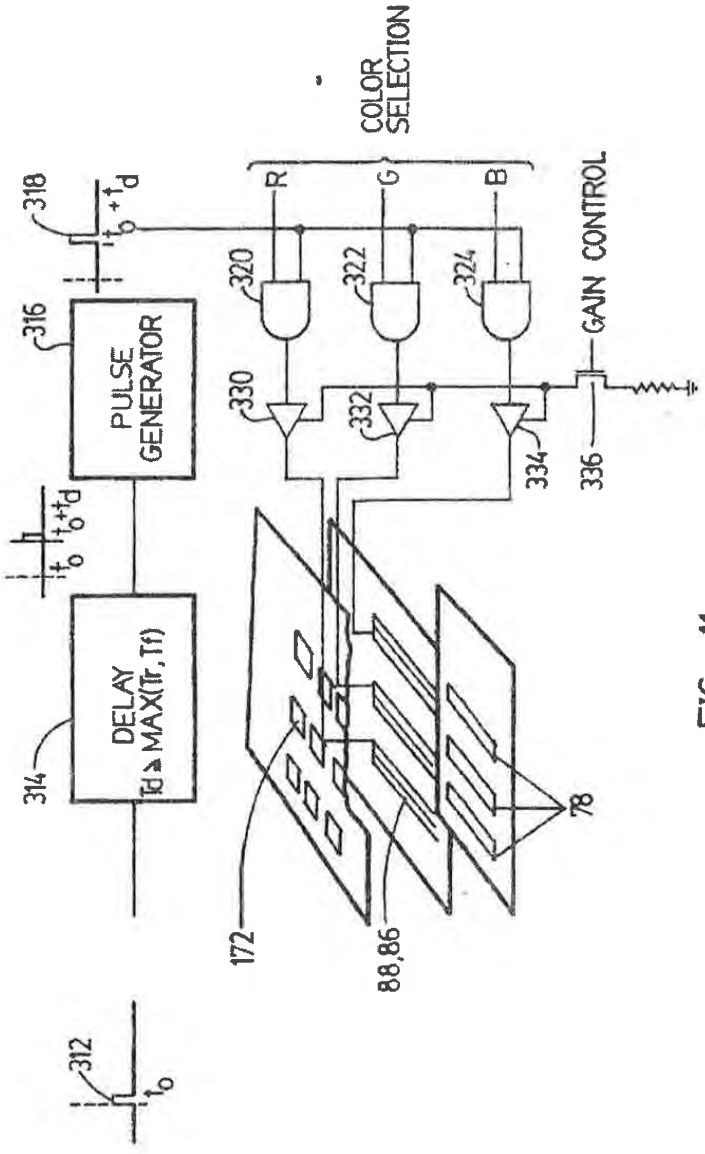


FIG. 11.

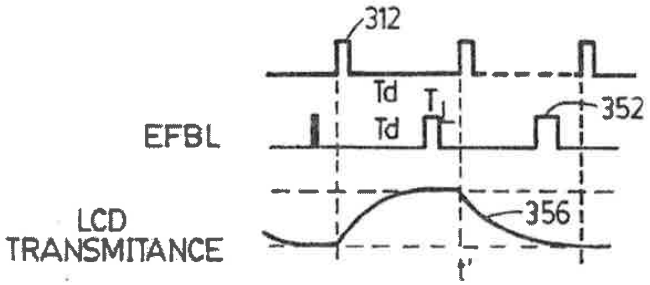


FIG. 12.

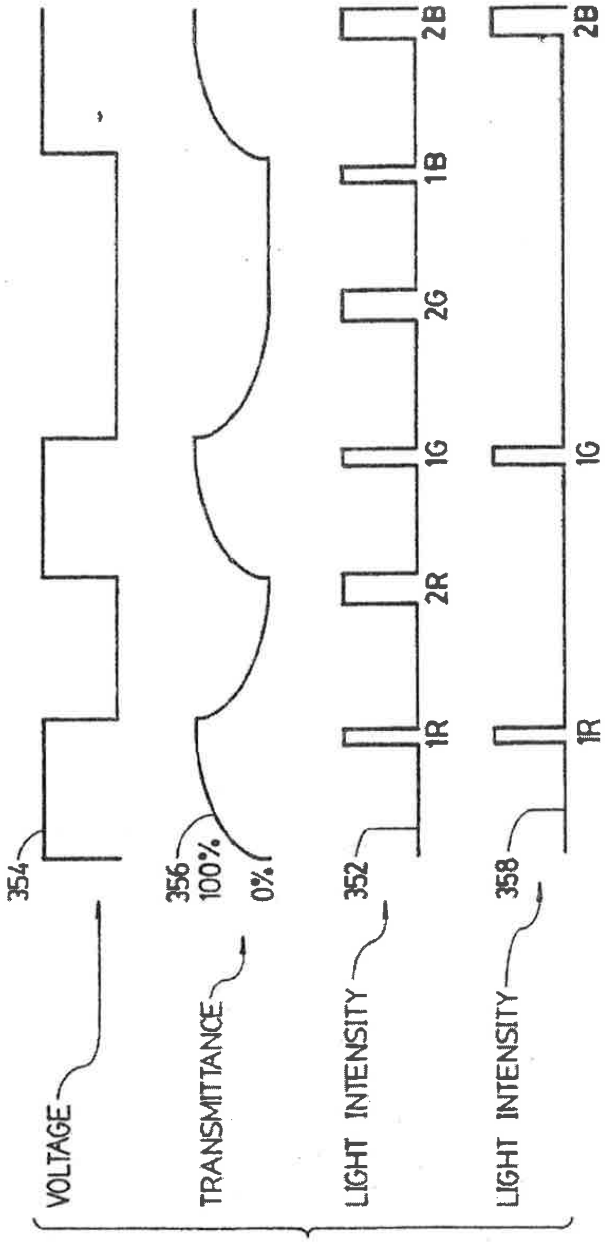


FIG._13.

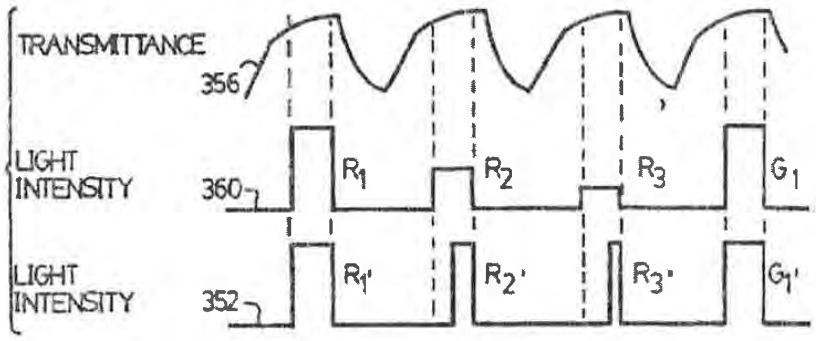


FIG. 14.

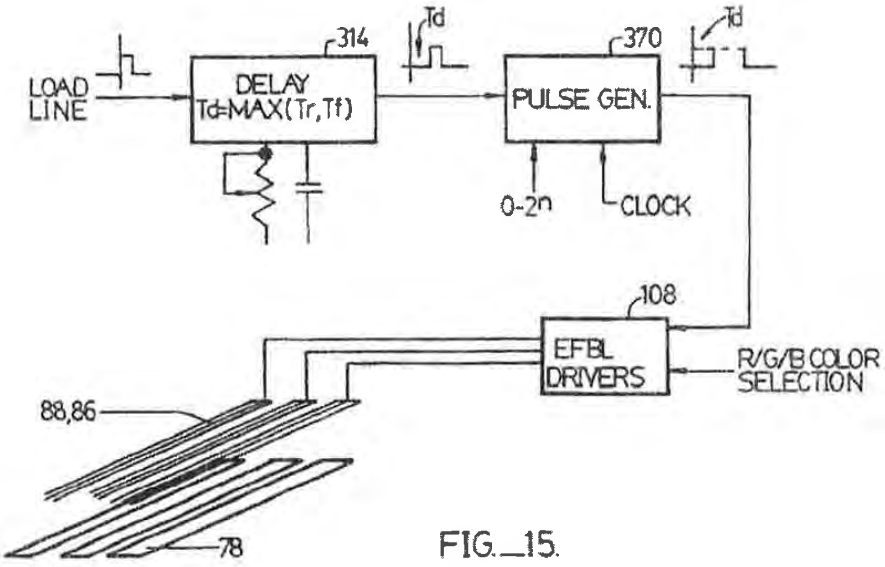


FIG. 15.

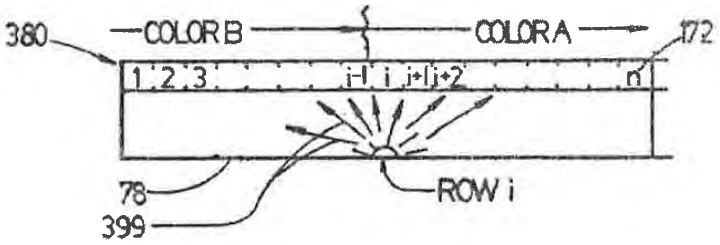


FIG. 16.

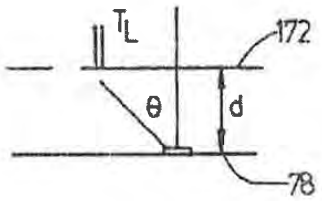


FIG. 17.

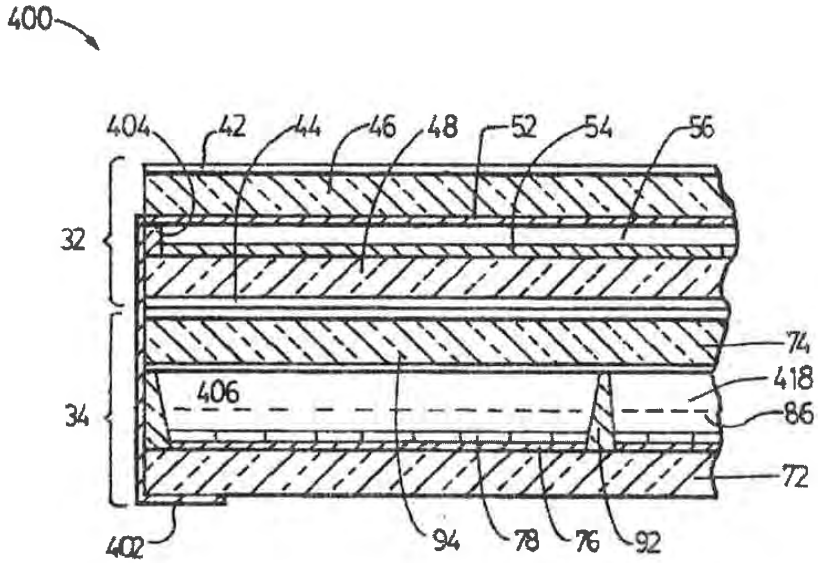


FIG. 18.

COLOR FLUORESCENT LIQUID CRYSTAL DISPLAY

This is a continuation of application Ser. No. 812,730, filed Dec. 23, 1991, now abandoned.

BACKGROUND OF THE INVENTION

This invention relates in general to an efficient display device capable of displaying monochromatic, multi-color and full-color images of high brightness and resolution. Specifically, the invention relates to a liquid crystal device (LCD) without color filters, where the LCD is illuminated by a back lighting source, which is an electronic fluorescent source emitting monochromatic light or light of multiple colors, such as the three primary colors of red, blue and green.

LCDs are one of the most widely used type of devices. However, most of the LCDs used today are monochromatic. While multi-color and full-color LCDs have been proposed, their development has been hindered by a number of technical difficulties. In most of the multi-color and full-color LCDs proposed, a back light source is employed. However, in most cases, the back light source employed is white light. Therefore, to produced composite images of different color, red, blue and green filter arrays have been used. For each pixel, the white light directed towards a portion of the pixel is filtered to permit only red light to pass, and white light directed toward another portion of the same pixel is filtered to permit only blue light to pass and the white light directed towards the remaining portion is filtered to permit only green light to pass. Thus only a small part of the energy of the white light is transmitted through the LCD. If relatively pure red, blue and green light is desired, the filters employed must have narrow pass bands, so that the percentage of the energy of the white light utilized is further reduced. Alternatively, if a brighter display is desired, the user may have to compromise on the color quality and utilize red, blue and green filters with broader pass bands.

LCD cells respond slowly to voltages applied across them. Typically, when scanning voltages are first applied to a LCD cell, the cell has low transmission rate. The transmission rate rises slowly during the scanning cycle so that a low percentage of light is passed by the red, blue and green filters and transmitted through the LCD cells during the scanning cycle. This is a notable drawback of passive matrix type LCD color displays, where no drivers are used contiguous to the LCD cells for driving the cells.

To improve display brightness, active matrix LCD cells are proposed by adding at least three thin film transistors for each LCD cell or pixel for accelerating the turning on and off of the three portions of the cell or pixel for light transmission of the three different colors. Such transistors, however, are opaque and occupy a significant area of the LCD cell. In other words, whatever the designer may have gained by increasing the transmission rate, the designer will lose at least part of the advantage because of the reduction of the area of the cell that actually transmits light.

A further complication in the active matrix LCD type displays is in manufacturing. Thus if a thin film transistor in one of the LCD pixels or cells is defective, the entire display is useless and must be discarded. Because of yield problems, redundant transistors are implemented. However, adding more thin film transistors further reduces the light transmitting portion of the pixel and is undesirable. For a display with many pixels, the reduction in area is considerable. For example, for a 480 by 240 pixel display, $480\times240\times3$ transistors must be used even without any redundancy in transistors. If redundunt transistors are included, such as by using two transistors for each color in a pixel, $480\times240\times3\times2$ transistors must be used.

For the reasons above, it is difficult to use the above-described conventional designs to achieve efficient color LCD displays of high brightness, good color and high resolution. This is particularly the case for large displays. It is therefore desirable to provide an alternative design for color LCD displays which are inexpensive and where the above-described difficulties are avoided or alleviated.

SUMMARY OF THE INVENTION

This invention is based on the observation that the above-described difficulties of conventional color LCDs can be alleviated or avoided altogether by using an electronic fluorescent device (EFD) as the back light source in place of a white light source with filters. The flat panel color display apparatus of this invention comprises a layer of liquid crystal material, means for addressing locations on said layer to cause said layer to modulate the intensity of light transmitted through said layer at selected locations, and a back light source for supplying light towards the liquid crystal layer. The back light source comprises a housing defining therein a vacuum chamber, a plurality of cathodes disposed in the chamber, means for causing the cathodes to emit electrons and an anode in the chamber. The source further includes control means in the chamber for causing the electrons emitted by the cathodes to travel towards the anode at selected locations, and means disposed in the chamber at or near the anode and responsive to said electrons- for generating and directing light toward the layer of liquid crystal material.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross-sectional view of a portion of a passive matrix electronic fluorescent LCD to illustrate an embodiment of the invention.

FIG. 2 is a block diagram of an electronic control system for applying various voltages and signals to the device of FIG. 1 to illustrate the invention.

FIG. 3 is a schematic view of a portion of an active matrix conventional LCD device.

FIG. 4 is a schematic view of a portion of an active matrix electronic fluorescent LCD device to illustrate an embodiment of the invention.

FIG. 5 is a cross-sectional view of an electronic fluorescent LCD device to illustrate further features of the invention.

FIG. 6 is a schematic view showing electrical connections between the grid electrodes of an EFD for addressing different phosphor strips that correspond to M pixel arrays to illustrate the invention.

FIG. 7 is a cross-sectional view of a portion of an electronic fluorescent LCD device employing cone-shaped field electron emitting cathode structures to illustrate another embodiment of the invention.

FIG. 8 is a perspective view of the top surfaces of the gates and the tip portions of the cathodes of the electronic fluorescent LCD device of FIG. 7.

FIG. 9 is a cross-sectional view of a portion of the electronic fluorescent LCD device of FIGS. 7 and 8.

FIG. 10 is a timing diagram illustrating the addressing and control signals applied by an address and control system such as that of FIG. 2 to an analog gradation electronic fluorescent LCD device to illustrate the invention.

FIG. 11 is a block diagram of a control system for operating an analog gray scale electronic fluorescent LCD to illustrate the invention.

FIG. 12 is a timing diagram of control signals and the transmittance of the LCD to illustrate a digital gray scale electronic fluorescent LCD to illustrate the invention.

FIG. 13 is a timing diagram of control signals for electronic fluorescent LCD device to illustrate in more detail the scheme of FIG. 12 for generating digital gray tone values.

FIG. 14 is a timing diagram of control signals to illustrate alternative schemes to that of FIGS. 12, 13 for implementing digital gray tone values.

FIG. 15 is a schematic circuit diagram illustrating a control circuit for generating the control signals of FIGS. 12, 13.

FIG. 16 is a schematic view of a portion of an electronic fluorescent LCD device to illustrate an aspect of the invention for reducing crosstalk.

FIG. 17 is a schematic view illustrating the effect of turning off early the data-pulse to the electronic fluorescent device in reducing crosstalk.

FIG. 18 is a cross-sectional view of an electronic fluorescent LCD to illustrate a mosaic type display.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. 1 is a cross-sectional view of the portion of an electronic fluorescent LCD (EFLCD) to illustrate one embodiment of the invention where the LCD device therein is the passive type with no devices contiguous to the LCD pixels or cells for driving the cells. As shown in FIG. 1, EFLCD 30 comprises the passive matrix LCD 32 and an electronic fluorescent device (EFD) 34. LCD 32 is a black/white LCD without color filters and EFD 34 emits substantially monochromatic light or light of different colors as a back light source. The addressing and control systems for addressing and controlling LCD 32 and EFD 34 are synchronized so that, where EFD emits light of different colors, the combination of the devices of 32 and 34 turn an originally black/white LCD 32 into a high brightness and efficient multi-color or full-color display with good color. While in the preferred embodiment, EFD 34 emits light of multiple colors, such as red, blue and green light, it will be understood that EFD 34 may also be monochromatic.

In FIG. 1, LCD 32 may be a black and white digital LCD, or a single-matrix or multi-matrix passive LCD, or an active matrix LCD with thin film transistors (TFT) but can also be a digital modulation or analog modulation LCD. When combined with an electronic fluorescent back lighting source 34, the combination can achieve many different display functions.

LCD 32 comprises polarizers 42, 44, face plate 46 and back plate 48, and two groups of preferably mutually perpendicular x, y electrodes 54, 52 respectively, a layer of liquid crystal material 56, and side sealing walls 58. As in conventional LCDs, the row or x electrodes are elongated and form a substantially coplanar array where the electrodes are preferably substantially parallel to one another. The y or column electrodes 52 are similarly elongated and form a substantially coplanar array of preferably substantially parallel electrodes. Thus each column electrode overlaps each of the row electrodes, where the overlapping square or rectangular area of a row electrode and a column electrode defines a pixel of LCD 32 and of the EFLCD 30. Thus the pixels of EFLCD form an array with linear rows of pixels parallel to and aligned with the array of row electrodes 54. While in the description above in reference to FIG. 1, the row electrodes 54 are the scanning electrodes, it will be understood that the column electrodes 52 may be used for scanning, in which case the array of corresponding pixels will be scanned column by column instead. All such variations are within the scope of the invention. As described in detail below, scanning signals are applied to the row electrodes 54 and data signals are applied to the column electrodes 52 where the scanning and data signals together control the transmission rate of each pixel of the light passing therethrough. The above-described structure and operation of LCD 32 is that of a passive, simple matrix type conventional LCD.

In the embodiment of FIG. 1, EFD 34 is a full-color electronic fluorescent back light (EFBL) source which provides red, green and blue luminescence. EFD 34 comprises a back plate 72 and a face plate 74, anode 76 on the internal surface of back plate 72, and elongated red, green and blue primary color phosphor strips 78 on the anode. Back plate 72, face plate 74 and side plate 82 form a housing which enclose therein a sealed chamber 84 which is evacuated. Disposed in vacuum chamber 84 is a first set of grid electrodes 86 and a second group of grid electrodes 88, and cathodes 90.

Filaments of cathodes 90 may be the type that are provided with direct heating oxide coatings. In the embodiment of FIG. 1, when filaments 90 are heated by means of rated heating voltage, the filaments emit electrons. A voltage difference is applied between the cathodes 90 and anode 76 so that the electrons emitted by the cathodes will travel towards the anode. When these electrons impinge on the phosphor strips 78, the phosphor strips will respond by generating red, green or blue light. The surface of the anode facing the LCD 32 is highly light reflective to increase the efficiency of the device.

Three types of phosphor strips are employed: the first type generates red light, the second type green light, and the third type blue light, in response to electrons. The light generated by phosphor strips 78 are transmitted across chamber 84 through face plate 74 to the LCD 32. When selected pixels of LCD 32 are rendered light transmitting, the light emitted by the phosphor strips 78 will be transmitted through such pixels to display images of the required colors. To achieve uniform back lighting intensity, it is preferable to employ denser narrow arrays of phosphor strips 78 where the width of the individual strips are small compared to the widths of electrodes 52 or 54 of LCD 32. The outside surface and/or inside surface (that is, the surface closer and adjacent to vacuum chamber 84) are diffusion surfaces to increase the uniformity of the back lighting intensity.

To provide support to the face and back plates 74, 72 against atmospheric pressure, spacers 92 are employed to provide sufficient mechanical strength to the housing of EFD 34 and so that the face and back plates can be made relatively thin even when they have large surface areas. In such manner, a flat panel color electronic fluo-

rescent LCD **30** is provided where the total thickness of device **30** may be less than 2 cm.

Preferably, to reduce any dark areas that may be visible on the display screen, spacers **92** are elongated members with a wedge-shaped cross-section with a thinner side **92***a* facing LCD **32** as shown in FIG. **1**. The two slanting side surfaces **92***b* are highly reflective diffusing surfaces in order to reflect light impinging thereon towards the LCD **32**, in order to further reduce any dark areas that may be visible through LCD **32**, in order to achieve uniform intensity back lighting. Preferably, as shown in FIG. **1**, layer **94** is a transparent conductive film on the internal surface of face plate **74**; conductive film **94** reduces any effect of extraneous electric and magnetic fields on the EFBL **34**.

LCD device **32** is addressed in a conventional manner. Typically, row electrodes **54** and the corresponding rows of pixels are scanned one at a time and sequentially, for example, from the top row towards the bottom row, until the bottom row is reached at which time the top to bottom scanning process is repeated. At the same time, data signals are provided to column electrodes **52**, where the scanning signals to row electrodes **54** and data signals to column electrodes **52** together would determine whether any particular pixel is rendered light transmitting or not as well as determining the transmission rate of the pixel as is known to those skilled in the art. For this reason, the detailed working mechanism of LCD **32** will not be elaborated here. Since the LCD **30** is typically scanned one row electrode or one column electrode at a time, for improved efficiency, it may be desirable to provide back lighting only to the portion of the LCD which is being scanned. For this reason, preferably the elongated phosphor strips **78** are arranged substantially parallel to the array of electrodes being scanned; in the case of FIG. **1**, strips **78** are arranged parallel to the array of row electrodes **54** which are scanned one at a time from top to bottom. In FIG. **1**, for example, during operation of the device, the left edge of device **30** is rotated to become the top surface so that the leftmost row electrode **54** becomes the top electrode and the scanning proceeds from the top electrode downwards.

For improved efficiency, during the scanning of the topmost four or five row electrodes **54** (that is, the four or five near side wall **58**, all shown in FIG. **1**), only the cathodes **90** and the grid electrodes between the side plate **82** and spacer **92** need to be used for generating back light. Thus the plurality of spacers **92** may be provided in chamber **84** to divide the chamber into a number of subchambers. A control means described in detail below is then used for applying different voltages to the cathodes and the grid electrodes to cause the cathodes and grid electrodes in each subchamber to generate electrons so that only the phosphor strips disposed within the subchamber will emit light towards through the row electrodes **54** which are being scanned at the same time. In this manner, the operation of device **30** is made more efficient. Moreover, the phosphor strips are arranged to alternate periodically in the repetitive order (e.g. R, G, B, R, G, B, . . .) as illustrated in the figures.

FIG. **2** is a block diagram of a system **100** illustrating one embodiment of the addressing and control system of the EFLCD device of this invention. For simplicity, identical components in the different figures of this application are referred to by the same numerals. The LCD **32** may be controlled via analog signals where the transmission rates of a number of selected pixels in a row of pixels being scanned are proportional to the amplitudes of analog input signals. In such event, the LCD column drivers **102** are controlled directly by the analog input to generate the analog data signals applied to the column electrodes of LCD **32**. In such case, the EFBL **34** would simply provide constant amplitude and fixed width red, green and blue pulses in synchronism with the LCD addressing to provide red, green and blue light of different gray tones that are transmitted through the LCD **32**. Such analog addressing will be described in more detail below in reference to FIGS. **10** and **11**.

Alternatively, each scanning cycle will be divided into three, six, nine, twelve, . . . , (increasing as multiples of three) segments, and during each segment of the scanning cycle, each pixel in the pixel row scanned is either entirely closed to light transmission or fully turned on for maximum light transmission. In synchronism therewith, the display control unit **104** then generates a fixed sequential pattern of voltage pulses applied to the EFBL **34** for generating a fixed pattern of varying intensities of red, green and blue light pulses. Each segment of the scanning cycle of the LCD **32** corresponds to each of the red, green and blue light pulses. By selecting to pass or not to pass each of such pulses during each segment of the scanning cycle, different gray tone red, green and blue light transmission through the LCD **32** is accomplished. Such digital operation will be described below in reference to FIGS. **12–15**.

In reference to FIG. **2**, display control unit **104** generates scanning pulses for driving the LCD row drivers **106** which in turn generate the scanning pulses for scanning the rows of electrodes LCD **32**. Display control unit **104** also generates the RGB data pulses which are fed to EFBL drivers **108** through RGB scanning unit **110**. Where the scanning cycle is to be divided into a number of scanning segments, the input signal fed at **101** is converted by A/D converter **112** into a sequence of bits for controlling whether the pixels in the scanned pixel row should be on or off. Such sequence of bits are stored in the video memory **114** and are then fed to LCD column drivers **102** for controlling turning on and off the pixels in the scanned pixel row in LCD **32**. The operation of AD converter **112** and memory **114** are controlled by display control unit **104**. The display control unit **104** also generates a stream of digital signals to RGB scanning unit **110** and EFBL drivers **108** for generating fixed patterns of voltage signals for application to the cathodes and grid electrodes of the EFBL **34** for generating a selected one of a number of fixed patterns of red, green and blue light pulses

In the embodiment of FIG. **1**, LCD **32** is a passive matrix device with no active devices implemented adjacent to the LCD layer **36** for driving the LCD pixels. As indicated above, passive matrix LCD devices are slow. For this reason, active matrix LCD devices have been proposed such as those illustrated in FIG. **3**. As shown in FIG. **3**, **150** is a schematic view of a portion of a conventional active matrix LCD where thin film transistors **152** are implemented contiguous to the pixels for driving the pixels. As can be seen from FIG. **3**, since conventional color LCD devices employ filters which permit only one of either red, green or blue light to pass, these filters cannot overlap so that each individual pixel must comprise subpixels each designated to transmit only red, green or blue light. For this reason, in order to produce a full range of multi-color or full-color images,

each pixel must comprise at least three subpixels **154**. These subpixels are typically sequentially addressed one row at a time at a relatively high frequency so that, to the eyes of an observer, all three colors are stably displayed. Where the subpixels are sufficiently small, the red, green and blue subpixels will appear to merge to give the uniform color of a particular color with gray tones.

In FIG. 3, the x bus carries scanning signals for scanning rows of subpixels and the y bus carries data signals which together with the scanning signals modulate the transmission rate of each pixel. As can be observed from FIG. 3, in order to address the three subpixels of each pixel individually, a significant percentage of the display area is occupied by the x and y buses. If thin film transistors such as transistors **152** are employed to speed up the LCD, additional areas of the LCD display screen will be occupied by these transistors, thereby further reducing the percentage of the display screen which can transmit light. As noted above, because of yield problems, sometimes two thin film transistors are employed for each subpixel; in such event, even a larger percentage of the area of LCD display screen is occupied by opaque circuit elements. For the above reasons, conventional color LCD does not provide images of good brightness and is inefficient.

FIG. **4** is a schematic view of a portion of an active matrix color LCD device to illustrate this invention. In contrast to the conventional device **150**, in device **170** of this invention, no color filters are employed and each pixel is used to transmit all colors of the back light source. Thus if the back light source emits red, green and blue light, each pixel such as pixels **172** will all transmit red, green and blue light throughout their entire areas. The back light source may be caused to emit sequentially red, green and blue light at a sufficiently high frequency so that to an observer, a multi-color or full-color image will be observed. To achieve the same resolution as conventional device **150**, the pixels **172** may each be three times larger than the subpixels **154** of device **150** so that pixels in device **150** are roughly of the same size as pixels **172**. However, in comparison to device **150**, device **170** devotes much less percentage of its area to the x and the y buses than the y device **150** since only one set of lines will be adequate to address each pixel **172** instead of three sets required for device **150**. Alternatively, if the pixels **172** are made to be of the same size as subpixels **154** of device **150**, device **170** can achieve three times the resolution of device **150** with the same overhead devoted to the x and y buses and to the thin film transistors.

FIG. **5** is a cross-sectional view of a portion of an EFD **200** suitable for use in the EFLCD of this invention to illustrate the preferred embodiment of the invention. As noted above, the generation of electrons and the control of their passage to the phosphor strips are such as to cause the phosphor strips to generate red, green and blue light sequentially, but not all at the same time. For this purpose, it is desirable for the electrons generated to be directed only towards the phosphor strips that generate one of red, green or blue light and not at the same time directed towards phosphor strips that generate the other two kinds of light. As shown in FIGS. **1** and **5**, the phosphor strips that generate only red light are labeled R, those that generate only green light labeled G, and those that generate only blue light labeled B. Thus the cathodes **90** are heated by rated heating voltage from unit **104** through EFBL drivers **108** to generate electrons **202**.

When red light is to be generated, appropriate voltages are then applied to the first set of grid electrodes **204** in FIG. **5** to thereby cause electrons **202** to be directed only towards the phosphor strips R, and not towards the phosphor strips G, B. During the time interval during which green light is to be emitted by the EFD **200**, the voltages applied to the grid electrodes **204** should be such that the electrons should be directed only towards the phosphor strips labeled G. The same is true during the time interval for generating blue light, during which the electrons are to be directed only towards the phosphor strips B. Typically, this can be achieved by applying a more positive voltage to the grid electrodes in the first set **204** that are aligned with and correspond to the appropriate set of phosphor strips and a more negative voltage to the remaining grid electrodes in the first set. Thus as shown in FIG. **5**, each phosphor strip has aligned with it and corresponding thereto, three grid electrodes in the first set **204**, where the three corresponding electrodes are connected together by an electrical conductor **206** so that when the appropriate voltage is applied to one of the three grid electrodes, all three grid electrodes will be at the same voltage. Such connection renders the voltage uniform between the three grid electrodes corresponding to a phosphor strip and improves the uniformity of the light emission of the EFD **200** and therefore the overall quality of the display using the EFD. So aligning the three corresponding grid electrodes with their corresponding phosphor strip and applying appropriate voltages reduce the number of electrons directed towards other phosphor strips, and also reduce the intensity of light of other colors generated unintentionally. Such feature therefore reduces crosstalk between adjacent phosphor strips and the extraneous light of other unwanted colors will be reduced.

As noted above, spacers **92** divide chamber **84** into a number of subchambers so that light emitted by phosphor strips will be transmitted only through the pixels in the pixel row and not towards the pixels that correspond to the phosphor strips in a different subchamber. Thus the light passing through the pixels in the scanned pixel row may originate from a number of different phosphor strips in the same subchamber. To further improve the uniformity of the display, it is desirable to provide substantially the same voltage to the grid electrodes in the subchamber that correspond to and align with each of the phosphor strips in the subchamber that generate light of the same color. FIG. **6** is a schematic view illustrating a scheme of connections which is particularly useful to accomplish such purpose. As shown in FIG. **6**, the first set of grid electrodes **204** are divided into a number of subgroups of three grid electrodes each, where each subgroup is aligned with and correspond to a phosphor strip, where a subgroup corresponding to a phosphor strip for generating red light is labeled "R", the subgroup aligned with and corresponding to a phosphor strip for generating green light is labeled "G", and a subgroup aligned with and corresponding to a phosphor strip for generating blue light is labeled "B". Each subchamber contains a number of phosphor strips and a corresponding number of subgroups of grid electrodes of three grid electrodes each. As shown in FIG. **6**, all the subgroups labeled "R" are connected together by electrical connector **212** and to a terminal R_1. All the subgroups labeled "G" are con-

nected together by an electrical connector **214** to a terminal G_1. All the subgroups labeled "B" are connected by an electrical connector **216** to a terminal B_1. Therefore, by applying the appropriate voltage to the three terminals R_1, G_1, B_1, the subgroups that are connected to the appropriate terminal will all be at the same voltage which improves the uniformity of the light intensity generated by phosphor strips of the same color within the same subchamber.

As shown in FIG. **6**, the EFLCD has a total number of M pixel arrays, corresponding to M row or column electrodes in the LCD. The M row or column electrodes therefore correspond to M pixel arrays. The M row or column electrodes are divided into p groups of n rows or columns each, wherein the phosphor strips (not shown in FIG. **6**) are also divided into p groups, each aligned and corresponding with one of the p groups of row or column electrodes, where the grid electrodes for controlling electrons directed towards each of the p groups are controlled by signals applied to the corresponding three terminals in the following sets of terminals: R_1, G_1, B_1; R_2, G_2, B_2; . . . . . ; R_p, G_p, B_p. For example, as also shown in FIG. **6**, as for the subgroups of grid electrodes corresponding to the next group of pixel arrays or row or column electrodes (n+1) through (2n+1), again all the subgroups of grid electrodes corresponding to phosphor strips for emitting light of the same color are connected by electrical connectors to the same terminals R_2, G_2, and B_2. The same is true for all the remaining subgroups of the grid electrodes corresponding to the p groups of phosphor strips. Thus when a pixel array corresponding to a row or column electrode in the first of the p groups is addressed, appropriate voltages are applied sequentially to the terminals R_1, G_1, and $B_1$to generate the desired back light for displaying a monochromatic, multi-color, or full-color image. When a pixel array corresponding to a row or column electrode in a different one of the p groups is addressed, then the terminals connected to the subgroups of grid electrodes for addressing such particular group of row or column electrodes are addressed in the same manner for supplying the appropriate back light.

The above-described system for generating electrodes employs heated filaments. Another type of system for generating electrons is known as field emission cathodes or cold cathodes, such as the Microtip structure first introduced by Spindt in the Journal of Applied Physics, Vol. 47, No. 12, p. 5248. See Technical Note 1, Oct. 1990 from the Coloray Display Corp., entitled "Field Emission Display Technology Review." A cross-sectional view of EFBL device **250** is shown in FIG. **7**. As shown in FIG. **7**, instead of using elongated filaments that are heated, the Microtip cold cathode structures are cone-shaped structures **252** with apex **252***a* which emits electrons which can then be accelerated by the voltage difference between the cathodes and the anodes and controlled by grid structures **254**. The cone-shaped cathodes may be located on the conductive substrate **256** and the cone structures **252** are located within holes **260** in electrically insulating layer **262**.

FIG. **8** is a perspective view of the grid electrodes **254** and the tips **252a** of the cathodes, where the grid electrode for directing the electrons towards a phosphor strip for generating red light is labeled R, and so on. FIG. **9** is a cross-sectional view of an EFLCD employing the EFD **250** of FIG. **7**. For simplicity, some of the layers have been omitted from FIG. **9**, it being understood that the presence of such omitted layers may be desirable to improve the performance of the device. The surface of grid electrodes **254** are highly light reflective so as to reflect light towards the LCD **32** to increase efficiency of the device.

As shown in FIGS. **1** and **5**, a second group of grid electrodes **88** is employed. Substantially the same voltage is applied to all the grid electrodes in the second set **88** to evenly distribute the electrons generated by cathodes **90** throughout the lateral extent of the subchamber between spacer **92** and side plate **82** This improves the uniformity of the display. It will be understood, however, that if desired, this second set **88** of grid electrodes may be omitted, particularly if the thickness of the EFD is to be reduced. In FIG. **9**, however, since the second set **88'** of electrodes are closer to phosphor strips **78** than electrodes **254**, set **88'** is used instead of set **254** for controlling the paths of electrons and to direct them only to the strips whose light emission is desired at any particular time.

FIGS. **10** and **11** illustrate an analog EFLCD where the transmission rate of the LCD therein is proportional to analog input signals. In reference to FIGS. **2**, **10** and **11**, display control unit **104** applies pulses **301** each composed of a reset component and a scanning component periodically, including at times t_{n1}, t_{n2} and t_{n3} as shown in FIG. **10**. These reset and scanning pulses **301** are applied to LCD **32** by LCD row controllers **106** as controlled by unit **104**. In response to the analog input **101**, LCD column drivers **102** apply three sequential pulses t_{Rm}, t_{Gm} and t_{Rm} labeled **302** in FIG. **10**. To synchronize the timing of pulses **301**, **302**, a synchronization signal SYNC is applied to unit **104**. In response to pulses **301**, **302**, the transmission rate of a selected pixel addressed by pulses **301**, **302** is shown as curve **304** in FIG. **10**. As shown in FIG. **10**, the steady transmission rate (the level of the plateau such as at a, b, c) in curve **304** is proportional to the amplitude of pulses **302**. In synchronism therewith, EFBL **34** generates red, green and blue pulses of constant width and amplitude during the time period at which the transmission rate of the selected pixel is substantially constant.

LCDs are relatively slow devices. As seen in FIG. **10**, the LCD requires a certain time period after the application of pulses **301**, **302** before its transmission rate reaches a certain constant level. For this reason, it is desirable to cause the EFBL **34** to generate light of the appropriate color at a selected time t_L after the application of pulses **301**, **302** so that the back light is generated only when the transmission rate of the selected pixel has reached maximum level. This improves the efficiency of the EFLCD. In one embodiment, the electrons destined for the strips from the corresponding subgroup of grid electrodes are not directed towards the strips until the transmission rate **304** of the selected pixels reach 50%. Since t_L is a constant for any LCD, any LCD **32** used can be tested to determine the time t_L and the timing for application of voltages is adjusted so that the timing of pulses **303** of red, green and blue light is adjusted accordingly through unit **104**. Display control unit **104** generates scanning pulses **301** in response to the synchronization signal SYNC. LCD column drivers **102** derive data pulses **302** in response to reference pulses **312** said reference pulses being synchronized with scanning pulses **301**. "FIG. **11** is a schematic circuit diagram illustrating in some detail a circuit for generating pulses for operating the back light portion of an electronic

fluorescent LCD." First, the reference pulse is delayed by a delay **314** by a time period Td which should be the same as t_L of FIG. **10**. Pulse generator **316** then generates a corresponding pulse **318** which is similar to pulse **312** in shape but delayed relative to it by the time period Td (i.e., t_L). Such pulse **318** is applied to AND-gates **320, 322, 324**. Color selection signals R, G, B are also applied to the remaining inputs of the AND-gates so that when a particular color is desired, the corresponding AND gate is enabled. The output of the AND-gate enabled drives the corresponding one of three amplifiers **330, 332, 334**. The gains of the amplifiers are controlled by a gain control signal applied to the gate of a FET **336**. The outputs of the amplifiers **330, 332, 334** are pulses **302**. The gain control signal is derived from input **101** by the column drivers **102** in FIG. **2** in a conventional manner so that it will not be elaborated here. It will be noted in FIG. **10** that the pulses **303** are turned off during the time period t_F before the next scanning pulse. This reduces crosstalk in a manner described below.

FIGS. **12–15** illustrate another addressing and control scheme for generating various gray tones of red, green and blue to form a multi-color or full-color display in an EFLCD to illustrate another embodiment of the invention. In reference to FIGS. **2** and **13**, display control unit **104** of FIG. **2** generates a fixed pattern of red, green and blue pulses **352** illustrated in FIG. **13**. As shown in FIG. **13**, pulses **352** are composed of a red light pulse followed by another red light pulse of twice the width which is followed by a green pulse of the same width as the first red pulse and another green pulse of twice the width as the first green pulse, where the last green pulse is followed by a blue pulse of the same width as the shorter red and green pulses and is in turn followed by a blue pulse of twice its width. This pattern then is repeated indefinitely. Display unit **104** may cause this to happen by applying appropriate voltages to the appropriate group (**86, 204, 88'**) of grid electrodes.

However, light pulses **352** will not be visible through the LCD **32** unless the particular pixels scanned do transmit light. In FIG. **13**, each scanning cycle is divided into six segments, where during each segment, the selected pixel is either completely turned off so that it is opaque to light or it is fully turned on so as to transmit light at the maximum level. Each segment corresponds in timing to one of the six pulses **352**. Thus depending on whether during such segment of the scanning cycle, the pixel being scanned is rendered light transmitting or not, the corresponding light pulse **352** will either be transmitted or blocked.

In FIG. **13**, during the first, third and sixth segments of the scanning cycle, the selected pixel is rendered light transmitting to transmit three light pulses (**1R, 1G** and **2B**) to transmit light of a color of R:G:B ratio 1:1:2 (a blue-shaded gray). Thus by choosing to transmit or not transmit each one of the six pulses, a number of colors and color combinations can be generated.

Thus in FIG. **13**, during the first, third and sixth segments of the scanning cycle, data stored on the LCD electrode is a "1" while during the second, fourth and fifth segments, the data stored on the LCD electrode is a "0," as illustrated by the square signal **354** in FIG. **13**. Such signal is produced by column drivers **102** in response to the digitized input signal through converter **112** and memory **114**, and is applied to LCD **32**. The curve **356** for the transmittance of the LCD **32** in response to data **354** is also illustrated in FIG. **13**. The light pulses that are transmitted through the LCD **32** is illustrated by pulses **358**.

From the above illustration in reference to FIG. **13**, it will be noted that each of the red, green and blue colors may be selected in four different intensities of brightness (0 to 3). In other words, the gray tones for each of the colors may be represented by two bits. In order to provide a 3 bit gray tone for each color, the EFBL color pulse light **352** should instead comprise nine pulses (**1R, 2R, 4R; 1G, 2G, 4G; 1B, 2B, 4B**). The scanning cycle should then be divided into nine segments instead of six. If four bit gray tones are desired, the EFBL color pulse lights **352** should comprise indefinite repetitions of twelve pulses (**1R, 2R, 4R, 8R; 1G, 2G, 4G, 8G; 1B, 2B, 4B, 8B**) and the scanning cycle should be divided into twelve cycles. Thus in general, the number of pulses and the number of segments in the scanning cycle are equal to three times the number of bit gray tone values desired.

FIG. **14** illustrates an alternative scheme to FIG. **13** in essentially the same addressing and control system. In FIG. **13**, the gray tone values in pulses **352** are obtained by varying light pulse widths where the pulses are of constant amplitude. Instead of varying the pulse widths, the light pulse amplitudes may be varied instead as illustrated by pulses **360** in FIG. **14**. Thus pulses **360** have constant widths; however, their amplitudes vary. Therefore, instead of providing pulses **352** as described above, display control unit **104**, RGB scanning **110**, and EFBL drivers **108** may cause EFBL **34** to emit light pulses **360** instead and the above description in reference to FIG. **13** still applies for creation of various gray tones of red, green and blue.

FIG. **12** illustrates the relative timing of the LCD scanning or reference pulses **312**, the EFBL pulses **352**, and the LCD transmittance **356**. As in the case of an analog LCD illustrated in FIG. **10**, it is desirable to delay the generation of the EFBL light pulses **352** until the time when the transmittance of the LCD **356** is at its maximum. The EFD device **34** and **250** of this application generate back lighting pulses of brightness of over about 100,000 cd/m^2, so that even narrow pulses whose widths are small compared to the duration of the scanning cycle produce images of adequate brightness. For this reason, the efficiency of the display can be vastly improved by providing light from the EFLCD only through a small percentage of the scanning cycle.

In FIG. **12**, t' is the time at which a scanning cycle ends so that the next scanning cycle is for scanning the next row of pixels. From the shape of the curve **356**, it may appear that it will be desirable to delay pulse **352***a* until it is almost at the end of the scanning cycle, which is just before time t' at which time the LCD transmittance is maximum. However, doing so would cause undesirable crosstalk between the pixel row presently addressed and the adjacent pixel rows which have just been addressed immediately before time t', where the color or light intensities change at time t'. This aspect is illustrated in FIGS. **16** and **17**.

FIG. **16** is a schematic diagram of a subchamber **380** of EFD **34**. As noted above, spacers **92** would be effective in reducing or even preventing crosstalk between light generated from phosphor strips within one subchamber and the LCD pixels corresponding to a different subchamber. The feature of the invention illustrated in FIGS. **16, 17** further reduces crosstalk between pixel rows corresponding to phosphor strips within the same subchamber. Again there are a total of M row elec-

trodes corresponding to M pixel rows, where the M pixel rows are divided into p groups of n each within each subchamber. Subchamber **380** of FIG. **16** illustrates one of such subchambers. As shown in FIG. **16**, each of the n pixel rows is represented by a square box labeled by one of the numbers: 1, 2, 3, . . . i−1, i, i+1, i+2, . . . , n. The scanning direction is from 1 towards n.

The quantity Td (FIG. 12) is the delay between the scanning pulse for the ith row in FIG. 16 and the time at which pulse light generated by EFBL is fired to transmit light through the ith row. During one scanning field cycle beginning with the scanning pulse for the ith row, data will be fed sequentially into the i+1th row . . . , nth row, row 1 . . . , row i−1, where towards the end of the field cycle, row i−1 will also have been fed data to open the selected pixels in such rows. Therefore, in the extreme case illustrated in FIG. **16**, where rows **1** through i−1 are holding data for color B and rows i through n are holding data for color A, if the firing of the pulse light of EFBL is delayed until the end of the field cycle, the pulse light will be transmitted through one or more of the previously addressed rows i−1, i−2, . . . , where the number of rows affected depends on the viewing angle of the liquid crystal material and the spacing between the LCD layer and the phosphor layer in the EFLCD. Thus in order to reduce such crosstalk, it will be desirable for the EFBL to have finished emitting the light pulse (falling edge of light intensity) at the latest at a time T_L before the end of the field cycle where T_L is given by $kd.\tan\theta$, where d is the spacing between the LCD layer and the phosphor layer, θ being the viewing angle of the liquid crystal material, and k being a predetermined constant proportional to the scanning speed of the LCD in the EFLCD. Such configuration is illustrated in the schematic diagram of FIG. **16**.

The above-described EFLCD device may be used in many applications. For example, it may be used for generating alphanumeric digital displays to displays numbers, language characters or letters, and graphics. It can also be used to emit different color light as a function of the amplitude of an input signal such as speed. For example, when the EFLCD is used in a speedometer, at low speed, blue light is displayed. As the speed increases, the color of light emitted by the EFLCD changes from blue to bluish green to green, and then to yellowish green and yellow. When the speed is such as to require a user or driver to be warned, the light emitted changes color to orange. When the speed is in the danger zone, the color of the light emitted by the EFLCD becomes red, which may be emitted intermittently as a flashing red light as warning to users, drivers or other observers. The above-described scheme is particularly useful at a control center with many instrument panel displays. Thus if the large number of systems controlled by the control center are functioning properly, the light emitted by the EFLCD devices used in the display panels would all display green light. If one particular system deviates from normal operation, the EFLCD in the display panel for controlling such system may be used to display orange light. If the abnormality reaches into the danger zone, the EFLCD in the display panel for such system displays red light. Thus if one of many subsystems is not functioning properly, by displaying orange or red light amongst a large number of green light displays, improper functioning of systems can be easily discovered, and measures can be taken to remedy the situation. The particular sequence desired can be easily accomplished using software control in either the analog or digital manner described above. Such implementation is believed to be easily accomplished by those skilled in the art and would not be elaborated here. It will be evident in the above-described color transitions, that not the entire sequence is necessary and that some of the colors such as blue, bluish green or yellowish green may be omitted if desired. One may simply base the choice of colors on the fact that in the traffic light convention accepted all over the world today, green usually means that it is safe to proceed, yellow being a warning signal, and that red usually means danger.

FIG. **18** is a cross-sectional view of a portion of one of many panels arranged in an array of a flat mosaic color display apparatus. Each of such panels is essentially similar in construction to the EFLCD device described above. The LCD in the above-described EFLCD device may employ zone scanning. For example, each group of grid electrodes within a subchamber confided between spacers or between the spacers and the sidewall may be independently scanned relative to other groups of grid electrodes. For this reason, the LCD employed does not need high switching speeds to display high resolution video images. As indicated above, the surface of the anode **76** facing the LCD may be made of a high reflection coefficient material, such as aluminum film.

One common problem in mosaic type displays the dark lines or areas between adjacent panels in the panel array from which the mosaic display is constructed. To reduce such dark lines or areas, the electrical conductors **402** for connecting a control system such as system **100** of FIG. 2 to panel **400** may be employed on the outside surface of the sides of the panel **400** extending towards the back plate **72** of the EFD device **34'**. The side walls **404**, **406** are thinner compared to those of EFLCD **30** of FIG. **1**. Aside from such differences, LCD **32'** and EFD **34'** are essentially the same as LCD **32** and EFD **34** of FIG. **1**. With such construction, the dark areas caused by the side walls **404**, **406** and conductors **402** are minimized. The sidewall **404** has a thickness of less than about 5 mm. As in device **30**, the sidewalls and spacers employed in EFD **34'** are slanted or tapered and have diffusive reflection surfaces facing the LCD **32'** so as to further reduce any dark areas between panels. With such construction, a high resolution, the efficient mosaic flat panel monochromatic, multi-color or full-color display is provided.

While the invention has been described by reference to various embodiments, it will be understood that various modifications may be made without departing from the scope of the invention which is to be limited only by the appended claims.

What is claimed is:

1. A method for image display employing an apparatus comprising:

a front end unit including:

(a) an array of row electrodes and an array of column electrodes transverse to the row electrodes;

(b) a layer of liquid crystal material placed between and overlapping the two arrays at a pixel plane, wherein the row electrodes intersect the column electrodes over areas of intersection of the layer at the pixel plane to define a spatial sequence of a first through nth linear arrays of pixels, n being a positive integer, said n arrays arranged spa-

tially consecutively in the plane from the first array to the nth array;

a back light unit adjacent to the front end unit and having an array of elongated light emitting elements arranged in a light emitting plane alongside the pixel plane so that each light emitting element is spatially aligned and corresponds to at least one array of pixels, said elements including at least elements that emit light of a first color defining first color elements, and elements that emit light of at least one additional color defining additional color elements, wherein the total thickness of the apparatus is less than 2 cm;

said method comprising:

applying electrical signals to the two arrays of electrodes to cause each of the n arrays of pixels to modulate their light transmittance and one at a time during a corresponding scanning cycle defining the scanning of each such pixel array and so that the pixel arrays are sequentially scanned from the first to the nth array to sequentially modulate their light transmittance, said applying step applying a first sequence of first color data signals to modulate the light transmittance of the pixels for displaying and controlling the brightness of images of the first color, said applying step applying at least one additional sequence of other color data signals to modulate the light transmittance of the pixels for displaying images of said at least one additional color, said at least one additional sequence of signals being applied subsequent to or preceding the application of the first sequence of signals;

during the application of the first sequence, causing each of the first color elements aligned with and corresponding to at least one pixel array to emit light at a time delay after electrical signals are applied to the electrodes during the scanning cycle for such at least one pixel array to modulate the light transmittance of the corresponding at least one array of pixels for displaying and controlling the brightness of images of the first color; and

during the application of the at least one additional sequence, causing each of the additional color elements aligned with and corresponding to at least one pixel array to emit light at a time delay after electrical signals are applied to the electrodes during the scanning cycle for such at least one pixel array to modulate the light transmittance of the corresponding at least one array of pixels for displaying and controlling the brightness of images of said at least one additional color, so that different elements emitting light of the same color are caused to emit light sequentially over time and sequentially spatially across the light emitting plane;

said time delay or delays being such that each element emits light substantially at or near the end of the corresponding scanning cycle of the corresponding at least one array of pixels.

2. The method of claim 1, wherein the causing steps cause the elements to emit light pulses that are short in duration compared to the duration of the scanning cycles.

3. The method of claim 1, further comprising performing sequentially and repeatedly said applying step for applying said first sequence and said at least one additional sequence and performing sequentially and repeatedly said causing steps to cause the elements to emit sequentially light of the first color and said additional color, for a full color or multicolor display.

4. The method of claim 1, wherein said first color elements are grouped into groups of elements, and said additional color elements are grouped into groups of elements, the elements in each group being adjacent to one another and overlapping a corresponding group of array of pixels, said causing steps being such that they cause the elements in each group to emit light at the same time after electrical signals are applied to the electrodes to change the light transmittance of the arrays of pixels in the corresponding group of arrays of pixels to become light transmitting.

5. The method of claim 1, wherein said back light unit includes:

a housing defining a vacuum chamber therein, said light emitting elements being in said chamber;

an anode in the chamber, said anode overlapping entirely a plurality of arrays of pixels;

a plurality of cathodes in the chamber; and

a plurality of control electrodes in the chamber, said control electrodes aligned with and corresponding to the light emitting elements, wherein said causing steps include applying electrical signals to the anode, cathodes, and control electrodes.

6. The method of claim 5, wherein at least one of the cathodes does not spatially overlap at least one of the light emitting elements, said method further comprising causing the cathodes to generate electrons, wherein said step of applying electrical signals to the anode, cathodes, and control electrodes is such that electrons generated by said at least one cathode are directed towards said at least one of the elements to cause light emission therefrom.

7. The method of claim 6, wherein said step of applying electrical signals to the anode, cathodes, and control electrodes is such that electrons generated by said cathodes are spread out laterally before they are directed towards the elements.

8. The method of claim 5, wherein said elements are phosphor strips that generate light of a first, second or third color, and wherein said set of control electrodes comprises a plurality of subsets of control electrodes, each subset being aligned with and corresponding to a phosphor strip, said causing steps comprising applying a time sequence of predetermined voltages to said subsets of control electrodes to direct electrons sequentially towards phosphor strips that generate sequentially light of a first color, light of a second color, and then light of a third color.

9. The method of claim 5, wherein each of the first or additional sequence comprises a time sequence of first color or other color LCD data pulses and other data signals wherein said causing steps include applying a time sequence of electrical pulses, each electrical pulse being applied at a first time delay after the application of and corresponds to a first color or other color LCD data pulse,

wherein each electrical pulse is applied at a second predetermined time period preceding the LCD data pulse that succeeds the LCD data pulse corresponding to such electrical pulse to reduce crosstalk.

10. The method of claim 9, wherein the LCD data pulses are applied at a scanning speed, and wherein said second time period is greater than kd(tan0), where d is

the distance between the elements in the light emitting plane and the liquid crystal layer, θ the liquid crystal viewing angle, and k a constant inversely proportinal to the scanning speed of the LCD data pulses.

11. The method of claim 9, wherein said first predetermined time delay is such that each electrical pulse is applied when the transmission rate of the selected pixels through which light transmission is modulated exceeds about 50% of the light transmittance of such pixels upon settlement.

12. The method of claim 8, wherein said array of row or column electrodes includes M row or column electrodes divided into p groups of n rows or columns each, wherein said phosphor strips are divided into p groups each aligned and corresponding with one of the p groups of row or column electrodes, wherein the step for applying signals to the row or column electrodes and the step for applying voltages to the subsets of control electrodes are such that when such signals are applied to electrodes in a group, electrons destined for the strips of the corresponding group are not directed towards the strips until the transmission rate of the selected pixels corresponding to the selected group of row or column electrodes exceeds 50% of the light transmittance of such pixels upon settlement.

13. The method of claim 1, wherein said causing steps generate and direct sequentially red, blue and green light towards each pixel, so that when any pixel is light transmitting, red, blue or green light is permitted to pass through the entire pixel area to display multi-color or full color images.

14. An apparatus for image display comprising:

a front,end unit including:

(a) an array of row electrodes and an array of column electrodes transverse to the row electrodes;

(b) a layer of liquid crystal material placed between and overlapping the two arrays at a pixel plane, wherein the row electrodes intersect the column electrodes over areas of intersection of the layer at the pixel plane to define a spatial sequence of a first through nth linear arrays of pixels, n being a positive integer, said n arrays arranged spatially consecutively in the plane from the first array to the nth array;

a flat panel back light-unit adjacent to the front end unit and defining a vacuum chamber therein and an array of elongated light emitting elements in the chamber arranged in a light emitting plane alongside the pixel plane so that each light emitting element is spatially aligned and corresponds to at least one array of pixels, said elements including at least elements that emit light of a first color defining first color elements, and elements that emit light of at least one additional color defining additional color elements, wherein the total thickness of the front end and back light units is less than 2 cm;

a first device applying electrical signals to the two arrays of electrodes to cause each of the n arrays of pixels to modulate their light transmittance one at a time during a corresponding scanning cycle defining the scanning of each such pixel array and so that the pixel arrays are sequentially scanned from the first to the nth array to sequentially modulate their light transmittance, said first device applying a first sequence of first color data signals to modulate the light transmittance of the pixels for displaying and controlling the brightness of images of the first color, said first device applying at least one additional sequence of other color data signals to modulate the light transmittance of the pixels for displaying images of said at least one additional color, said at least one additional sequence of signals being applied subsequent to or preceding the application of the first sequence of signals;

a second device causing each of the first color elements aligned with and corresponding to at least one pixel array to emit light at a time delay after electrical signals are applied to the electrodes during the scanning cycle for such at least one pixel array and during the application of the first sequence, to modulate the light transmittance of the corresponding at least one array of pixels for displaying and controlling the brightness of images of the first color; and

wherein during the application of the at least one additional sequence, said second device causes each of the additional color elements aligned with and corresponding to at least one pixel array to emit light at a time delay after electrical signals are applied to the electrodes during the scanning cycle for such at least one pixel array to modulate the light transmittance of the corresponding at least one array of pixels for displaying and controlling the brightness of images of said at least one additional color, so that elements emitting light of the same color are caused to emit light sequentially over time and sequentially spatially across the light emitting plane;

said time delay or delays being such that each element emits light at a time substantially at or near the end of the scanning cycle of the corresponding at least one array of pixels.

15. The apparatus of claim 14, wherein said back light unit includes:

a housing defining said vacuum chamber therein, said light emitting elements being in said chamber;

an anode in the chamber;

a plurality of elongated cathodes in the chamber, wherein at least one of said cathodes does not spatially overlap at least one light emitting element; and

a plurality of control electrodes in the chamber, said control electrodes aligned with and corresponding to the light emitting elements, wherein said causing steps include applying electrical signals to the anode, cathodes including said at least one cathode, and control electrodes.

16. The apparatus of claim 15, further comprising a third device causing the cathodes to generate electrons, wherein said first device applies electrical signals to the anode, cathodes including said at least one cathode, and control electrodes such that electrons generated by said at least one cathode are directed towards said at least one of the elements to cause light emission therefrom.

17. The apparatus of claim 16, wherein said first device applies electrical signals to the anode, cathodes, and control electrodes such that electrons generated by said cathodes are spread out laterally before they are directed towards the elements.

18. The apparatus of claim 15, wherein said elements are phosphor strips that generate light of a first, second or third color, and wherein said set of control electrodes comprises a plurality of subsets of control electrodes, each subset being aligned with and correspond-

ing to a phosphor strip, said second device applying a time sequence of predetermined voltages to said subsets of control electrodes to direct electrons sequentially towards phosphor strips that generate sequentially light of a first color, light of a second color, and then light of a third color.

19. The apparatus of claim 15, wherein each of the first or additional sequence comprises a time sequence of first color or other color LCD data pulses and other data signals wherein said causing steps include applying a time sequence of electrical pulses, each electrical pulse being applied at a first time delay after the application of and corresponds to a first color or other color LCD data pulse,

wherein each electrical pulse is applied at a second predetermined time period preceding the LCD data pulse that succeeds the LCD data pulse corresponding to such electrical pulse to reduce crosstalk.

20. The apparatus of claim 19, wherein the LCD data pulses are applied at a scanning speed, and wherein said second time period is greater than kd(tan0), where d is the distance between the elements in the light emitting plane and the liquid crystal layer, 0 the liquid crystal viewing angle, and k a constant inversely proportinal to the scanning speed of the LCD data pulses.

21. A flat panel display apparatus comprising:

a layer of liquid crystal material;

a first device for addressing locations on said layer to cause said layer to modulate the intensity of light transmitted through said layer at selected pixel locations, said locations arranged in linear pixel arrays; and

a back light source comprising:

a plurality of cathodes disposed in a chamber;

a second device for causing the cathodes to emit electrons;

an anode in the chamber overlapping entirely a plurality of the arrays of pixels;

at least a first and a second set of control electrodes in the chamber substantially parallel to the layer, said two sets of control electrodes being on different planes between the anode and cathodes;

elements disposed in the chamber at or near the anode and responsive to said electrons for generating and directing light towards the layer of liquid crystal material, said elements arranged in arrays aligned with and corresponding to the linear pixel arrays, at least one of said cathodes not overlapping or aligned with any element; and

a third device for applying electrical signals to the anode, cathodes and control electrodes, causing the electrons emitted by the cathodes to travel towards the anode, and electrons emitted by said at least one cathode to travel toward an element;

wherein the electrical signals applied to the first or the second set of control electrodes are such that electrons emitted by the cathodes are caused to spread out laterally in the chamber and the cathodes and control electrodes and the electrical signals are such that electrons from different cathodes are directed towards a selected element to cause light emitted by the selected element to be directed to the corresponding pixel array to generate images.

22. The apparatus of claim 21, said elements generating and directing sequentially red, blue and green light towards each pixel, so that when any pixel is light transmitting, red, blue or green light is permitted to pass through the entire pixel area to display multi-color or full color images.

23. The apparatus of claim 21, wherein said elements comprises phosphor strips that emit light in one of three colors, said colors including red, blue and green, towards the anode in response to electrons, said strips being substantially parallel to the contol electrodes.

24. The apparatus of claim 23, wherein said set of control electrodes comprises a plurality of subsets of grid electrodes, each subset overlapping and corresponding to a phosphor strip, said third device applying a time sequence of predetermined voltages to said subsets of grid electrodes to direct electrons sequentially towards phosphor strips that generate sequentially light of a first color, light of a second color, and then light of a third color.

25. The apparatus of claim 23, said strips being arranged in an array where strips for emitting light of the three colors alternate periodically.

26. The apparatus of claim 21, wherein said back light source includes a housing comprising a face plate facing the liquid crystal layer and a back plate, said two plates defining between them the chamber, said housing further comprising a plurality of elongated spacers between the two plates dividing the chamber into a number of subchambers.

27. The apparatus of claim 26, wherein said spacers extend between the two plates to support the plates against atmospheric pressure, said spacers being wedge-shaped with thicker and thinner sides, their thinner sides being attached to the face plate to reduce any dark areas caused thereby.

28. The apparatus of claim 26, said spacers having diffusive light reflecting surfaces.

29. The apparatus of claim 21, said first device comprising an array of row electrodes and an array of column electrodes transverse to the row electrodes, said layer of liquid crystal material placed between and overlapping the two arrays at a pixel plane, wherein the row electrodes intersect the column electrodes over areas of intersection of the layer at the pixel plane to define a spatial sequence of a first through nth linear arrays of pixels, n being a positive integer, said n arrays arranged spatially consecutively in the plane from the first array to the nth array;

said first or second set of control electrodes divided into groups of control electrodes with each group corresponding to and aligned with a group of elements, wherein during at least one cycle of a scanning operation:

said first device applying scanning pulses to a selected electrode in the row or column electrode array and LC data pulses to the electrodes in the remaining electrode array to select pixels of the pixel array corresponding to said one selected electrode, through which transmission of light is modulated, and

said third device applying electrical data potential pulses to the group of control electrodes corresponding to and aligned with said selected electrode for sequentially emitting light of one or more colors through said selected pixels in the pixel row, said electrical data potential pulses being of predetermined time relationship with the scanning pulses for displaying monochromatic, multi-color or full color data in said pixel row.

30. The apparatus of claim 29, wherein selected pixels corresponding to the selected electrode during said at least one cycle are not in the nth array, and wherein during the next cycle of the scanning operation,

said first device applies additional LCD scanning pulses to the selected electrode adjacent to the electrode scanned in the previous cycle and LCD data pulses to the remaining electrode array to select pixels of the corresponding next pixel array through which transmission of light is permitted, and

said third device applies data potential pulses to the group of control electrodes corresponding to and aligned with said next row electrode for sequentially emitting light of one or more colors through said selected pixels in the next pixel array, said data potential pulses being of predetermined time relationship with the additional scanning pulses for displaying monochromatic, multicolor or full color data in said next pixel array.

31. The apparatus of claim 30, wherein the third device applies each data potential pulse at a first predetermined time delay after the previous scanning LCD pulse and at a second predetermined time period preceding the next LCD scanning pulse to reduce crosstalk.

32. The apparatus of claim 31, wherein said second time period is greater than kd(tan0), where d is the distance between the phosphor strips and the liquid crystal layer, 0 the liquid crystal viewing angle, and k a constant inversely proportinal to the scanning speed.

33. The apparatus of claim 31, wherein said first predetermined time delay is such that the transmission rate of the selected pixels through which light transmission is permitted exceeds about 50% of the transmission rate at settlement when each data potential pulse is applied.

34. The apparatus of claim 29, said elements including phosphor strips, wherein one of said arrays includes M row or column electrodes divided into p groups of n rows or columns each, wherein said phosphor strips are divided into p groups each aligned and corresponding with one of the p groups of row or column electrodes, wherein the third device is such that when the voltages are applied to electrodes in a group, electrons destined for the strips of the corresponding group are not directed towards the strips until the transmission rate of the selected pixels corresponding to the selected group of row or column electrodes reach 50% of the transmission rate upon settlement.

35. The apparatus of claim 21, wherein said second device includes means for heating the cathodes.

36. The apparatus of claim 35, wherein said cathodes include an array of elongated oxide coated filaments arranged substantially parallel to one another.

37. The apparatus of claim 21, said cathodes comprising cone-shaped field electron emitting structures, one of said sets of control electrodes including at least one set of grid electrodes substantially parallel to said row or column electrodes, wherein said grid electrodes define holes therein, said cone-shaped cathodes being located in said holes with their tips exposed for emitting electrons.

38. The apparatus of claim 21, said anode being located between the cathodes and the liquid crystal layer, said anode being substantially transparent, wherein said control electrodes have light reflecting surfaces facing the layer for reflecting light towards the layer.

39. The apparatus of claim 21, said cathodes being located between the anode and the liquid crystal layer, said anode having a light reflecting surface facing the layer for reflecting light towards the layer.

40. The apparatus of claim 21, back light source including a housing having a face plate adjacent to the liquid crystal layer so that light emitted by the elements passes through said face plate before it travels to the layer, said face plate having an internal surface in the chamber and an external surface outside the chamber, wherein the internal or external surface or both surfaces are light diffusive to evenly distribute light transmitted from the back lighting source to the layer.

* * * * *

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(12) **United States Patent**
Chen et al.

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(45) **Date of Patent: Mar. 25, 2003**

(54) **LOW-POWER LCD DATA DRIVER FOR STEPWISELY CHARGING**

(75) Inventors: **Shang-Li Chen**, Hsinchu (TW); **Chien-Yu Yi**, Taoyuan (TW)

(73) Assignee: **Industrial Technology Research Institute** (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 211 days.

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(52) **U.S. Cl.** 345/211; 345/98
(58) **Field of Search** 345/204, 208–215, 345/690–693, 87, 94–96, 98–100

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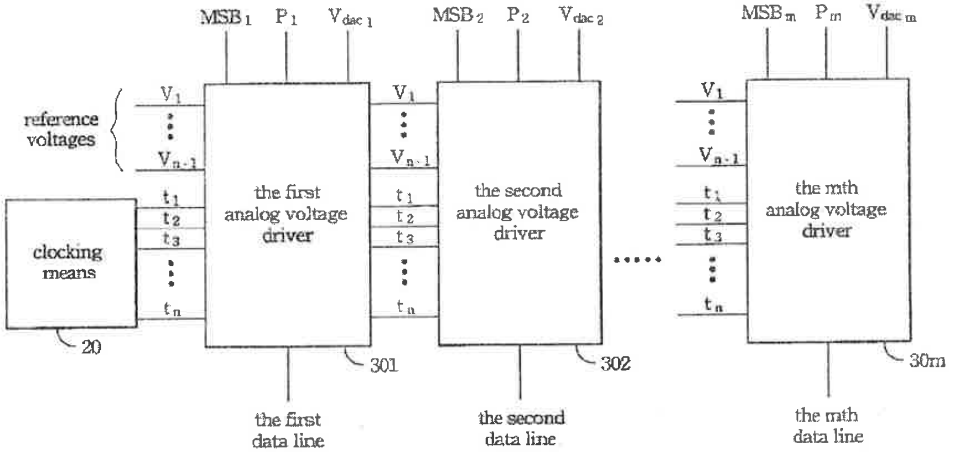
(57) **ABSTRACT**

A power-saving data driver for stepwisely applying alternating driving voltages with a predetermined number of steps to a plurality of data lines in a liquid crystal display is disclosed. The data driver is comprised of a clocking means, a plurality of reference voltages, and a plurality of analog voltage driver. The clocking means is used for providing clock signals for stepwisely charging and discharging. The plurality of reference voltages work as steps of said stepwisely charging and discharging. The reference voltages are distributed between the system voltage and the ground. Each of the analog voltage driver corresponds to one of the data lines. A given pixel is stepwisely driven from a driving voltage of the last pixel as a beginning voltage to a driving voltage of the given pixel as a target voltage. The reference voltages between the beginning voltage and the target voltage are turned-on in order according to the clock signals generated by the clocking means.

30 Claims, 4 Drawing Sheets



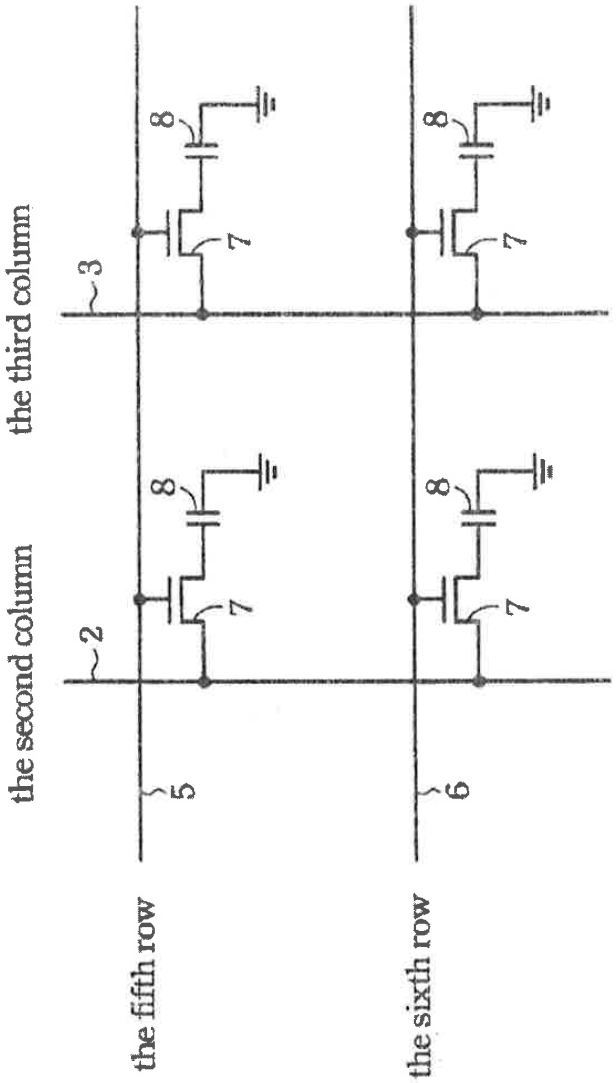


Fig. 1
(Prior Art)

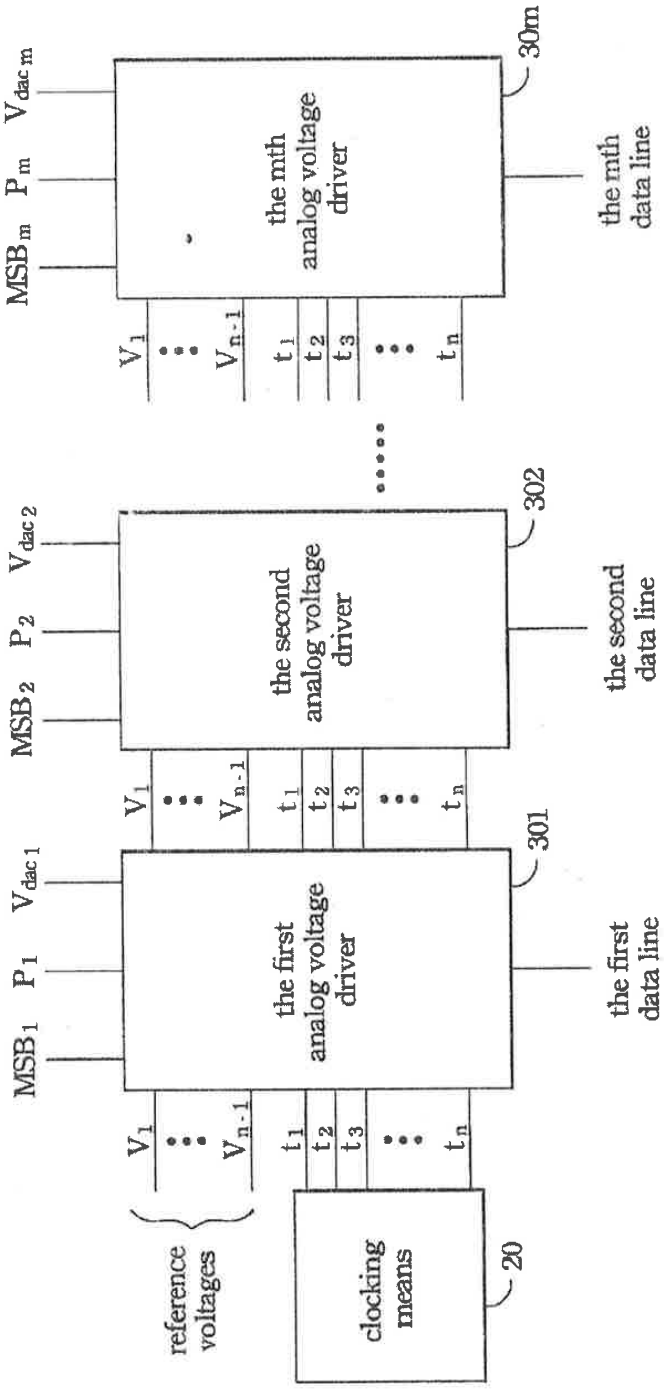


Fig. 2

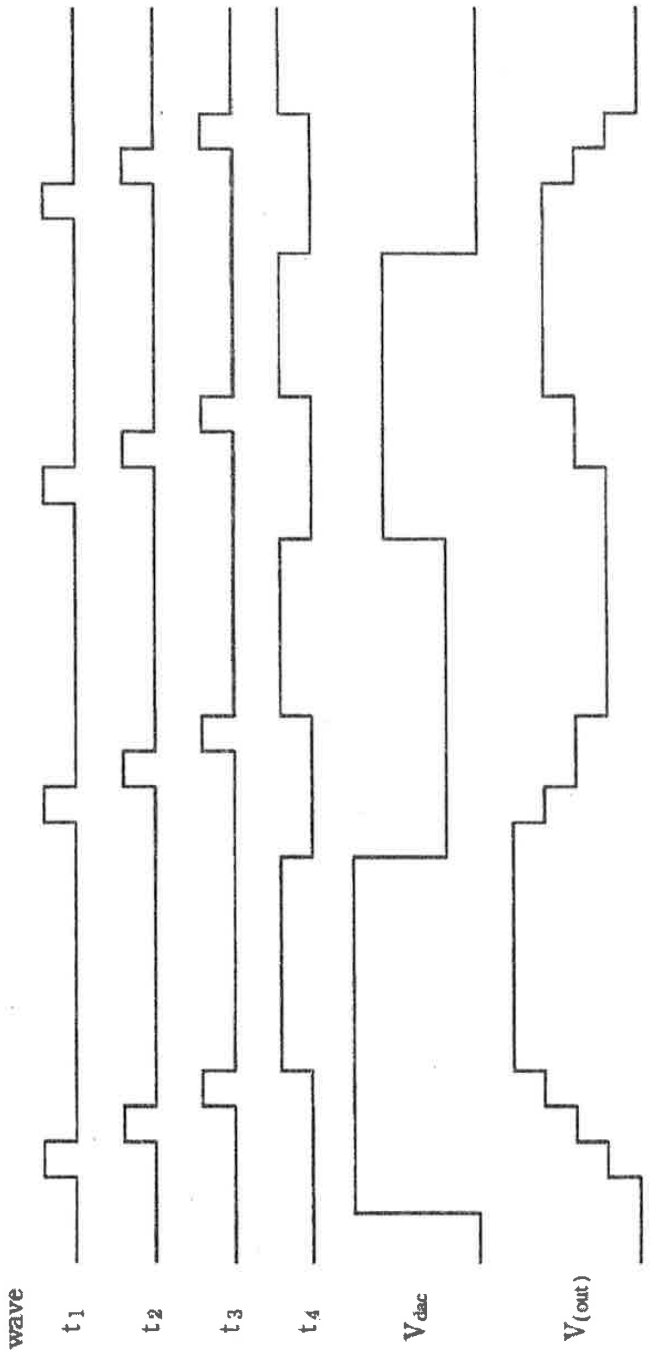


Fig. 3

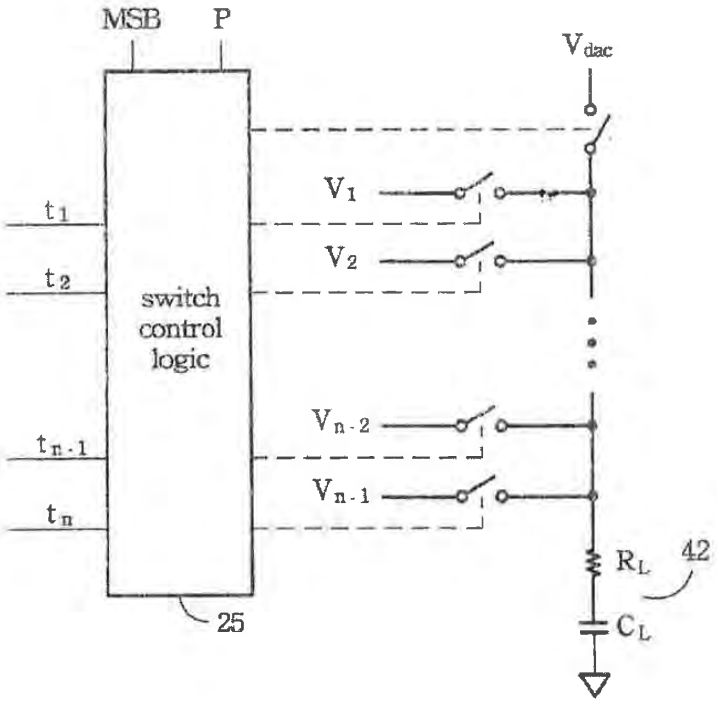

MSB
P
V_{dac}
V_1
V_2
t_1
t_2
switch control logic
V_{n-2}
t_{n-1}
V_{n-1}
t_n
R_L
42
25
C_L

Fig. 4

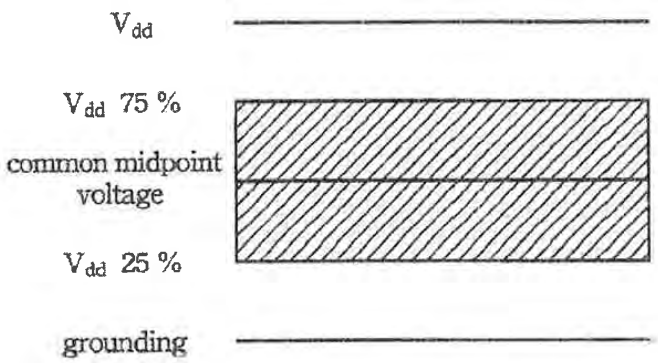

V_{dd}
V_{dd} 75 %
common midpoint voltage
V_{dd} 25 %
grounding

Fig. 5

LOW-POWER LCD DATA DRIVER FOR STEPWISELY CHARGING

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The present invention relates generally to circuitry for driving an liquid crystal display (LCD) or the like, and more particularly, to a circuit and a method which largely reduce the consumed power for driving the data lines of the LCD display.

(2) Description of the Related Art

The breathtaking growth of the information and communication industries push forward the fast development of LCD displays, which are used in a large variety of products including notebook computers, hand-held computers, cellular phones, and many kinds of personal digital assistants (PDAs). The LCD displays are available in both gray-scale and color panels, and are typically arranged as a matrix of intersecting hundreds or thousands of rows and columns. Generally, the intersection of each row and column forms a pixel, whose brightness and color are defined by the electronic voltage applied thereto.

The LCD monitors used in the notebook computers requires a relatively large number of such pixels to form a pixel array. Referring now to FIG. 1, a portion of a pixel array of an active matrix liquid crystal display according to the prior art is shown. The four pixels connected in the fifth row 5, the sixth row 6, the second column 2, and the third column 3 of the array are shown. Each pixel is comprised of a switch 7 and a capacitor 8. The switch of each pixel in the same row is connected by a scan line, and the switch of each pixel in the same column is connected by a data line. The method of controlling the image displayed on the screen is to select one scan line at a time, and to apply control voltages through each data line to each column of the selected scan line. After all columns of the selected scan line are applied the control voltages, the next scan line will be selected to apply control voltages through each data line to its corresponding column. After the completion of one display cycle during which each row in the array has been selected, a new display cycle begins, and the process is repeated to refresh the displayed image.

The data lines are driven by a data driver, which is typically formed upon monolithic integrated circuits. Actually, a color LCD monitor requires three times as many data driver outputs as the monochrome LCD monitor. The color LCD monitor requires three data driver outputs per pixel , one of each of the three primary colors (red, green, blue) to be displayed. Thus, a typical VGA color liquid crystal display with 480 rows×640 columns includes 1920 data lines which must be driven by a like number of column data driver outputs.

The liquid crystal displays are capable of displaying images because the optical transmission characteristics of liquid crystal material change in accordance with the magnitude of the applied electronic voltage. However, the application of a steady DC voltage to a liquid crystal material for a long; period will permanently change and degrade its physical properties. For this reason, it is common to drive the liquid crystal displays using drive techniques which charge each liquid crystal with voltages of alternating polarities relative to a common midpoint voltage value. The voltages greater than and less than the common midpoint voltage represent the positive polarity and the negative polarity, respectively.

Image quality displayed by the LCDs and the complexity of the driver circuitry are highly related to the methods of polarity inversion. There are four major types of inversion of alternating polarities relative to the common midpoint voltage, i.e. frame inversion, column inversion, row inversion, and dot inversion. According to the frame inversion, every pixel on the display frame is first driven to its positive polarity during a first display cycle, and then driven to its negative polarity during the second display cycle. The column inversion implies that each pixel in a data line is driven to the positive polarity, and the adjacent data line is driven to the negative polarity. According to the row inversion, if the pixels in a row are driven to the positive polarity during the first row drive period, the pixels in the next row will be driven to the negative polarity during the second row drive period. According to the dot inversion, if a pixel is charged with the positive polarity, the next pixel within the same row will be charged to the negative polarity, and the adjacent pixel in the same column but in the preceding or following row is also charged to the negative polarity. Although the drive circuitry of the dot inversion is the most complex one, it displays the best image property. For this reason, the dot inversion will be the main stream of the drive circuitry in the field of the liquid crystal displays.

The data driver suffers a relatively large capacity from the data line. In accordance with conventional teachings, power dissipation of a circuit is directly related to the operating frequency (f), the capacitance (C) and the square of the voltage (V^2) applied to the capacitive element. For this reason, the power dissipation of a data driver is significant. Especially, in the inversion schemes of the row inversion and the dot inversion, the charging/discharging processes for alternating polarities results in a very large power dissipation.

For this reason, it is very important for LCD industries to develop a low-power LCD data driver.

SUMMARY OF THE INVENTION

Accordingly, it is a primary object of the present invention to provide a low-power LCD data driver.

It is another object of the present invention to provide a method of driving LCD's data lines with low power dissipation.

A power-saving data driver for stepwisely applying alternating driving voltages with a predetermined number of steps to a plurality of data lines in a liquid crystal display is disclosed. The data driver is comprised of a clocking means, a plurality of reference voltages, and a plurality of analog voltage driver. The clocking means is used for providing clock signals for stepwisely charging and discharging. The plurality of reference voltages work as steps.of the stepwisely charging and discharging. The reference voltages are distributed between the system voltage and the ground. Each of the analog voltage driver corresponds to one of the data lines. A given pixel is stepwisely driven from the driving voltage of the last pixel as a beginning voltage to the driving voltage of the given pixel as a target voltage. The reference voltages between the beginning voltage and the target voltage are turned-on in order according to the clock signals generated by the clocking means.

In one embodiment of the present invention, the predetermined number of steps is four and thus there are three reference voltages, i.e. the first reference voltage, the second reference voltage, and the third reference voltage. The second reference voltage is the common midpoint voltage of the alternating driving voltages. The first reference voltage

is 75% of the system voltage and the third reference voltage is 25% of the system voltage.

In another embodiment of the present invention, the first reference voltage is a voltage corresponding to the positive polarity with 50% of optical transmission rate, and the third reference voltage is a voltage corresponding to the negative polarity with 50% of optical transmission rate.

In another embodiment of the present invention, the first reference voltage is the positive voltage obtained by charging/discharging a capacitor connected to the analog voltage driver for a plurality of times, and the third reference voltage is a negative voltage obtained by charging/discharging a capacitor connected to the analog voltage driver for a plurality of times.

BRIER DESCRIPTION OF THE DRAWINGS

The accompanying drawings forming a material part of this description, in which

FIG. 1 schematically illustrates a portion of a pixel array of an active matrix liquid crystal display according to the prior art.

FIG. 2 schematically illustrate the block diagram of the stepwise charge/discharge driver according to the present invention.

FIG. 3 schematically illustrates the wave diagrams of t1, t2, t3, t4, Vout, and Vdac according to the present invention.

FIG. 4 schematically illustrates the block diagram of the analog voltage driver according to the present invention.

FIG. 5 schematically illustrates the reference voltages according to an embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention is related to a power-saving data driver for stepwisely applying alternating driving voltages with a predetermined number of steps to a plurality of data lines in a liquid crystal display.

As mentioned above, the liquid crystal display should be driven by alternation polarities relative to the common midpoint voltage value. For this reason, the data line driver should keep charging and discharging the data lines continuously, especially in the case of row inversion and dot inversion. According to the present invention, a plurality of switches in the analog voltage driver are controlled by the polarities (P) and the MSBs of the digital data of the driving voltage so as to largely reduce the power dissipation.

The driving voltage Vdac is derived from the traditional digital-analog-converter for driving the data lines. As mentioned in the background of the invention, the driving voltage Vdac is directly coupled to the data lines according to the prior art. That will result in large power dissipation. In order to reduce the power dissipation, the method of stepwise charge and discharge is applied in the present invention.

The energy dissipated is $1/2(CV^2)$ for each charge/discharge process applied to a capacitive element, where C is the capacitance of the capacitive element and V is the maximum voltage in the charge or discharge process. In case the charge or discharge process is divided into n steps and the voltage variation of each step is V/n, the energy dissipation for each step is $(1/2)(CV^2)/n^2$. As a result, the energy dissipate of n steps is $(1/2)(CV^2)/n$, which is the conventional energy dissipation divided by n. For example, if the predetermined number of steps is four, the energy dissipation will be the conventional energy dissipation divided by four, and thus largely reduced. About this theory, please refer to U.S. Pat. No. 5,473526 for more detailed.

Referring now to FIG. 2, the block diagram of the driver circuitry for stepwisely charging and discharging according to the present invention is disclosed. The driver circuitry is comprised of a clocking means 20, a plurality of reference voltages, and a plurality of analog voltage drivers 30. Each analog voltage driver corresponds to one of the plurality of data lines, wherein the first analog voltage drivers 301, the second analog voltage drivers 302, and the mth analog voltage driver 30 m are shown in FIG. 2.

The clocking means 20 is used for generating clock signals for stepwisely charging and discharging. The input terminal of the clocking means 20 is coupled to system clock CLK and RST, and its output terminal provides clock signals t1, t2, t3. . . , tn for stepwisely charging and discharging to all of the analog voltage drivers including the first analog voltage drivers 301, the second analog voltage drivers 302, and the mth analog voltage driver 30 m, wherein n implies the predetermined number of steps. For example, if the predetermined number of steps is four, the clocking means 20 will provide four clock signals of t1, t2, t3, and t4, as shown in FIG. 3.

The number of the plurality of reference voltages is the predetermined number of steps minus one, and the plurality of reference voltages are distributed between the system voltage (Vdd) and the ground.

The input terminal of the first analog voltage driver 301 is coupled to the clocking means, the plurality of reference voltages V1, . . . , Vn−1, the driving voltage Vdac1, the polarity P, and the brightness information MSB (most significant bit). The output terminal of the first analog voltage driver 301 is coupled to the first data line for driving it. In addition, the other analog voltage drivers such as the second analog voltage driver 302 to the mth analog voltage driver 30m have the same connection relationship. The output terminal of each analog voltage is coupled to its corresponding data line.

Referring now to, FIG. 4, the block diagram of the analog voltage driver according to the present invention is disclosed. The input terminal of the analog voltage driver 30 is coupled to the driving voltage Vdac1 and the plurality of reference voltages V1, . . . , Vn−1 from the switch control logic 25. Its output terminal is coupled to its corresponding data line, i.e. the load 42. The analog voltage driver 30 includes the first switch element and the other n−1 switch elements, which can be MOS transistors. The n switch elements in the analog voltage driver 30 are turned on or off in sequence depending on the polarity P and the brightness information MSB. As a result, the stepwise charge and discharge can be well achieved, as shown in FIG. 3.

The driving method according to the present invention is described as follows. As mentioned above, it is common to drive the liquid crystal displays using drive techniques which charge each liquid crystal with voltages of alternation polarities relative to the common midpoint voltage value, which is 50% of the system voltage Vdd. The positive polarity voltages imply the driving voltages between the system voltage Vdd and the common midpoint voltage, and the negative polarity voltages imply the driving voltages between the common midpoint voltage and the ground. According to the normally black LCD panels, the liquid crystal layer transmits no light if no driving voltage is applied to. The larger the driving voltage, the higher the optical transmission rate is. This implies that a given pixel

is brighter when the driving voltage is closer to the system voltage Vdd or the ground. On the other hand, a pixel is darker when the driving voltage is near the common midpoint voltage.

According to the first embodiment of the present invention, the predetermined number of steps is four, which implies that there are four steps for the analog voltage driver 30 to stepwisely charge and discharge. Referring now to FIG. 5, the reference voltages according to the first embodiment of the present invention is disclosed. The midpoint voltage is between the system voltage Vdd and the ground, and called Vdd 50%. The other two reference voltages, i.e. 75% of the system voltage (called Vdd 75%) and 25% of the system voltage (called Vdd 25%), are also shown in FIG. 5. Generally, the brightness of two adjacent pixels are close. For this reason, we suppose that the present pixel and the last pixel have nearly the same brightness and thus have the same MSB and opposite polarities. The four switch elements for turning-on Vdd 25%, Vdd 50%, Vdd 75%, and the driving voltage are turned on depending on the combinations of polarities P and the brightness MSB of the current pixel as follows.

1. Positive polarity (P=1)-bright (MSB=1): turning on Vdd 25%, Vdd 50%, Vdd 75%, and Vdac in order.
2. Negative Polarity (P=0)-bright (MSB=1): turning on Vdd 75%, Vdd 50%, Vdd 25%, and Vdac in order.
3. Positive polarity (P=1)-dark (MSB=0): turning on Vdd 50%, and Vdac in order.
4. Negative Polarity (P=0)-dark (MSB=0): turning on Vdd 50%, and Vdac in order.

In the first case, a bright pixel will be driven by the positive polarity, so the driving voltage output from the digital-analog-converter (Vdac) is located between Vdd and Vdd 75%. In this embodiment, the MSB of the last pixel is supposed to be the same with that of the present pixel but with opposite polarity, so the driving voltage of the last pixel is located between the ground and Vdd 25%. For this reason, the present pixel is stepwisely driven from the driving voltage of the last pixel to Vdd 25%, Vdd 50%, Vdd 75%, and Vdac in order. As mentioned above, the power dissipation of the data line driver can be largely reduced by means of the stepwise charge.

In the second case, a bright pixel will be driven by the negative polarity, so the driving voltage output from the digital-analog-converter (Vdac) is located between the ground and Vdd 25%. In this embodiment, the MSB of the last pixel is supposed to be the same with that of the present pixel but with opposite polarity, so the driving voltage of the last pixel is located between Vdd and Vdd 75%. For this reason, the present pixel is stepwisely driven from the driving voltage of the last pixel to Vdd 75%, Vdd 50%, Vdd 25%, and Vdac in order. As mentioned above, the power dissipation of the data line driver can be largely reduced by means of the stepwise discharge.

In the third case, a dark pixel will be driven by the positive polarity, so the driving voltage output from the digital-analog-converter (Vdac) is located between Vdd 50% and Vdd 75%. In this embodiment, the MSB of the last pixel is supposed to be the same with that of the present pixel but with opposite polarity, so the driving voltage of the last pixel is located between Vdd 50% and Vdd 25%. For this reason, the present pixel is stepwisely driven from the driving voltage of the last pixel to Vdd 50% and Vdac in order. As mentioned above, the power dissipation of the data line driver can be largely reduced by means of the stepwise charge.

In the fourth case, a dark pixel will be driven by the negative polarity, so the driving voltage output from the digital-analog-converter (Vdac) is located between Vdd 50% and Vdd 25%. In this embodiment, the MSB of the last pixel is supposed to be the same with that of the present pixel but with opposite polarity, so the driving voltage of the last pixel is located between Vdd 50% and Vdd 75%. For this reason, the present pixel is stepwisely driven from the driving voltage of the last pixel to Vdd 50% and Vdac in order. As mentioned above, the power dissipation of the data line driver can be largely reduced by means of the stepwise discharge.

According to the first embodiment of the present invention, the MSB of the last pixel is supposed to be the same with that of the present pixel. However, in the actual practice, the MSB of the last pixel can be different to that of the present pixel. In order to take this issue into consideration for further reducing the power dissipation, the circuit of the analog voltage driver is modified according to the second embodiment, so that Vdd 25%, Vdd 50%, Vdd 75%, and Vdac can be turned on depending on the polarity, MSB of the present pixel, and MSB of the last pixel (called Mp). There are total eight cases as follows:

1. P=1, MSB=Mp=1: turning on Vdd 25%, Vdd 50%, Vdd 75%, and Vdac in order.
2. P=0, MSB=Mp=1: turning on Vdd 75%, Vdd 50%, Vdd 25%, and Vdac in order.
3. P=1, MSB=Mp=0: turning on Vdd 50%, and Vdac in order.
4. P=0, MSB=Mp=0: turning on Vdd 50%, and Vdac in order.
5. P=1, MSB=1, Mp=0: turning on Vdd 50%, Vdd 75%, and Vdac in order.
6. P=0, MSB=1, Mp=0: turning on Vdd 50%, Vdd 25%, and Vdac in order.
7. P=1, MSB=0, Mp=1: turning on Vdd 25%, Vdd 50%, and Vdac in order.
8. P=0, MSB=0, Mp=1: turning on Vdd 75%, Vdd 50%, and Vdac in order.

In the first case, a bright pixel will be driven by the positive polarity, so the driving voltage output from the digital-analog-converter (Vdac) is located between Vdd and Vdd 75%. In this case, the MSB of the last pixel is the same with the present pixel but with opposite polarity, so the driving voltage of the last pixel is located between the ground and Vdd 25%. For this reason, the present pixel is stepwisely driven from the driving voltage of the last pixel to Vdd 25%, Vdd 50%, Vdd 75%, and Vdac in order. As mentioned above, the power dissipation of the data line driver can be largely reduced by means of the stepwise charge.

In the second case, a bright pixel will be driven by the negative polarity, so the driving voltage output from the digital-analog-converter (Vdac) is located between the ground and Vdd 25%. In this case, the MSB of the last pixel is the same with the present pixel but with opposite polarity, so the driving voltage of the last pixel is located between Vdd and Vdd 75%. For this reason, the present pixel is stepwisely driven from the driving voltage of the last pixel to Vdd 75%, Vdd 50%, Vdd 25%, and Vdac in order. As mentioned above, the power dissipation of the data line driver can be largely reduced by means of the stepwise discharge.

In the third case, a dark pixel will be driven by the positive polarity, so the driving voltage output from the digital-analog-converter (Vdac) is located between Vdd 50% and

Vdd 75%. In this case, the MSB of the last pixel is the same with the present pixel but with opposite polarity, so the driving voltage of the last pixel is located between Vdd 50% and Vdd 25%. For this reason, the present pixel is stepwisely driven from the driving voltage of the last pixel to Vdd 50% and Vdac in order. As mentioned above, the power dissipation of the data line driver can be largely reduced by means of the stepwise charge.

In the fourth case, a dark pixel will be driven by the negative polarity, so the driving voltage output from the digital-analog-converter (Vdac) is located between Vdd 50% and Vdd 25%. In this case, the MSB of the last pixel is the same with the present pixel but with opposite polarity, so the driving voltage of the last pixel is located between Vdd 50% and Vdd 75%. For this reason, the present pixel is stepwisely driven from the driving voltage of the last pixel to Vdd 50% and Vdac in order. As mentioned above, the power dissipation of the data line driver can be largely reduced by means of the stepwise discharge.

In the fifth case, a bright pixel will be driven by the positive polarity, so the driving voltage output from the digital-analog-converter (Vdac) is located between Vdd and Vdd 75%. In this case, the last pixel is a dark one with opposite polarity, so the driving voltage of the last pixel is located between the Vdd 50% and Vdd 25%. For this reason, the present pixel is stepwisely driven from the driving voltage of the last pixel to Vdd 50%, Vdd 75%, and Vdac in order. As mentioned above, the power dissipation of the data line driver can be largely reduced by means of the stepwise charge.

In the sixth case, a bright pixel will be driven by the negative polarity, so the driving voltage output from the digital-analog-converter (Vdac) is located between the ground and Vdd 25%. In this case, the last pixel is a dark one with opposite polarity, so the driving voltage of the last pixel is located between the Vdd 50% and Vdd 75%. For this reason, the present pixel is stepwisely driven from the driving voltage of the last pixel to Vdd 50%, Vdd 25%, and Vdac in order. As mentioned above, the power dissipation of the data line driver can be largely reduced by means of the stepwise discharge.

In the seventh case, a dark pixel will be driven by the positive polarity, so the driving voltage output from the digital-analog-converter (Vdac) is located between Vdd 50% and Vdd 75%. In this case, the last pixel is a bright one with opposite polarity, so the driving voltage of the last pixel is located between the ground and Vdd 25%. For this reason, the present pixel is stepwisely driven from the driving voltage of the last pixel to Vdd 25%, Vdd 50%, and Vdac in order. As mentioned above, the power dissipation of the data line driver can be largely reduced by means of the stepwise charge.

In the eighth case, a dark pixel will be driven by the negative polarity, so the driving voltage output from the digital-analog-converter (Vdac) is located between Vdd 50% and Vdd 25%. In this case, the last pixel is a bright one with opposite polarity, so the driving voltage of the last pixel is located between Vdd and Vdd 75%. For this reason, the present pixel is stepwisely driven from the driving voltage of the last pixel to Vdd 75%, Vdd 50%, and Vdac in order. As mentioned above, the power dissipation of the data line driver can be largely reduced by means of the stepwise discharge.

In the second embodiment, it is taken into consideration that the gray-scale of the present pixel is different to that of the last pixel. According to the charge/discharge method of the present invention, the MSB difference of the adjacent two pixel will no more result in extra charge or discharge process. As a result, the power dissipation according to this embodiment can be further reduced.

According to the foregoing two embodiment, it is assumed that the liquid crystal has a linear photo-electonic relationship, so as to set the reference voltages as Vdd 75%, Vdd 50%, and Vdd 25%.

Actually, the photo-electronic relationship is not necessary to be linear. In accordance with another embodiment of the present invention, the non-linear photo-electronic relationship is taken into consideration. Besides the common midpoint voltage, two more reference voltages are applied. One of them is a voltage corresponding to the positive polarity with 50% of optical transmission rate, and the other one is a voltage corresponding to the negative polarity with 50% of optical transmission rate.

In accordance with another embodiment of the present invention, besides the common midpoint voltage, two more reference voltages are applied. One of them is a positive voltage obtained by charging/discharging a capacitor connected to the analog voltage driver for a plurality of times, and the other one is a negative voltage obtained by charging/discharging a capacitor connected to the analog voltage driver for a plurality of times.

Of course, the predetermined number of steps is not necessary to be four. According to another embodiment of the present invention, the predetermined number of steps is two. The common midpoint voltage of the alternating driving voltages is defined as the reference voltage, wherein the first region is defined by voltages between the system voltage and the reference voltage and driven by the positive polarity, and the second region is defined by voltages between the reference voltage and the ground, and driven by the negative polarity.

According to another embodiment of the present invention, the predetermined number of steps is eight, and thus the number of the plurality of reference voltages is seven, including the first reference voltage, the second reference voltage, the third reference voltage, the fourth reference voltage, the fifth reference voltage, the sixth reference, and the seventh reference voltage. The fourth reference voltage is a common midpoint voltage of the alternating driving voltages. The first region is defined by voltages between the system voltage and the first reference voltage, and driven by the positive polarity. The second region is defined by voltages between the first reference voltage and the second reference voltage, and driven by the positive polarity. The third region is defined by voltages between the second reference voltage and the third reference voltage, and driven by the positive polarity. The fourth region is defined by voltages between the third reference voltage and the fourth reference voltage, and driven by the positive polarity. The fifth region is defined by voltages between the fourth reference voltage and the fifth reference voltage, and driven by the negative polarity. The sixth region is defined by voltages between the fifth reference voltage and the sixth reference voltage, and driven by the negative polarity. The seventh region is defined by voltages between the sixth reference voltage and the seventh reference voltage, and driven by the negative polarity. The eighth region is defined by voltages between the seventh reference voltage and the ground, and driven by the negative polarity.

According to another embodiment of the present invention, the predetermined number of steps can be sixteen or more larger. However, the predetermined number of steps cannot increase without limit. Otherwise, too many charging/discharging steps would not only lengthen the

charge/discharge duration, but also increase the complexity of the driving circuitry so as to enhance the power dissipation.

It should be understood that the foregoing relates to only preferred embodiments of the present invention, and that it is intended to cover all changes and modifications of the embodiments of the invention herein used for the purposes of the disclosure, which do not constitute departures from the spirit and scope of the invention.

What we claimed is:

1. A power-saving data driver by stepwise applying alternating driving voltages to a plurality of data lines of a liquid crystal display, said data driver comprising:

a clocking means for providing clock signals;

a plurality of reference voltages as steps of stepwise charging and discharging, wherein

the number of said plurality of reference voltages equals to a predetermined number minus one;

said plurality of reference voltages are distributed between a system voltage and a ground; and

a plurality of analog voltage drivers, wherein

each of said plurality of analog voltage driver corresponds to one of said plurality of data lines;

input terminal of each said plurality of analog voltage driver is coupled to said clocking means, said plurality of reference voltages, an analog driving voltage, and information of driving polarity and brightness;

output terminal of each said plurality of analog voltage driver is coupled to its corresponding data line which is connected to a plurality of pixels; wherein a given pixel is driven by a polarity opposite to the polarity for driving last pixel;

said given pixel is driven from a driving voltage of said last pixel as a beginning voltage stepwisely and sequentially through said reference voltages to a driving voltage of said given pixel according to said clock signals generated by said clocking means.

2. The power-saving data driver of claim 1, wherein said predetermined number of steps is four and thus said number of said plurality of reference voltages is three, wherein:

said three reference voltages includes a first reference voltage, a second reference voltage, and a third reference;

said second reference voltage is a common midpoint voltage of said alternating driving voltages;

a first region is defined by voltages between said system voltage and said first reference voltage, and driven by a positive polarity;

a second region is defined by voltages between said first reference voltage and said second reference voltage, and driven by a positive polarity;

a third region is defined by voltages between said second reference voltage and said third reference voltage, and driven by a negative polarity;

a fourth region is defined by voltages between said third reference voltage and said ground, and driven by a negative polarity.

3. The power-saving data driver of claim 2, wherein said first reference voltage is 75% of said system voltage and said third reference voltage is 25% of said system voltage.

4. The power-saving data driver of claim 2, wherein said first reference voltage is a voltage corresponding to positive polarity with 50% of optical transmission rate, and said third reference voltage is a voltage corresponding to negative polarity with 50% of optical transmission rate.

5. The power-saving data driver of claim 2, wherein said first reference voltage is a positive voltage obtained by charging/discharging a capacitor connected to said analog voltage driver a plurality of times; said second reference voltage is obtained by charging/discharging a capacitor connected to said analog voltage driver a plurality of times; and said third reference voltage is a negative voltage obtained by charging/discharging a capacitor connected to said analog voltage driver a plurality of times.

6. The power-saving data driver of claim 2, wherein said given pixel is stepwisely driven from said driving voltage of said last pixel to said third reference voltage, to said second reference voltage, to said first reference voltage, and finally to said driving voltage of said give pixel when said driving voltage of said given pixel is located in said first region and said driving voltage of said last pixel is located in said fourth region.

7. The power-saving data driver of claim 2, wherein said given pixel is stepwisely driven from said driving voltage of said last pixel to said first reference voltage, to said second reference voltage, to said third reference voltage, and finally to said driving voltage of said give pixel when said driving voltage of said given pixel is located in said fourth region and said driving voltage of said last pixel is located in said first region.

8. The power-saving data driver of claim 2, wherein said given pixel is stepwisely driven from said driving voltage of said last pixel to said second reference voltage and finally to said driving voltage of said give pixel when said driving voltage of said given pixel is located in said second region and said driving voltage of said last pixel is located in said third region.

9. The power-saving data driver of claim 2, wherein said given pixel is stepwisely driven from said driving voltage of said last pixel to said second reference voltage and finally to said driving voltage of said give pixel when said driving voltage of said given pixel is located in said third region and said driving voltage of said last pixel is located in said second region.

10. The power-saving data driver of claim 2, wherein said given pixel is stepwisely driven from said driving voltage of said last pixel to said second reference voltage, to said first reference voltage, and finally to said driving voltage of said give pixel when said driving voltage of said given pixel is located in said first region and said driving voltage of said last pixel is located in said third region.

11. The power-saving data driver of claim 2, wherein said given pixel is stepwisely driven from said driving voltage of said last pixel to said second reference voltage, to said third reference voltage, and finally to said driving voltage of said give pixel when said driving voltage of said given pixel is located in said fourth region and said driving voltage of said last pixel is located in said second region.

12. The power-saving data driver of claim 2, wherein said given pixel is stepwisely driven from said driving voltage of said last pixel to said third reference voltage, to said second reference voltage, and finally to said driving voltage of said give pixel when said driving voltage of said given pixel is located in said second region and said driving voltage of said last pixel is located in said fourth region.

13. The power-saving data driver of claim 2, wherein said given pixel is stepwisely driven from said driving voltage of said last pixel to said first reference voltage, to said second reference voltage, and finally to said driving voltage of said give pixel when said driving voltage of said given pixel is located in said third region and said driving voltage of said last pixel is located in said first region.

14. The power-saving data driver of claim 1, wherein said predetermined number of steps is two and a common midpoint voltage of said alternating driving voltages is defined as a reference voltages, wherein a first region is defined by voltages between said system voltage and said reference voltage and driven by positive polarity, and a second region is defined by voltages between said reference voltage and said ground, and driven by negative polarity.

15. The power-saving data driver of claim 1, wherein said predetermined number of steps is eight, and thus said number of said plurality of reference voltages is seven, wherein:

said seven reference voltages includes a first reference voltage, a second reference voltage, a third reference voltage, a fourth reference voltage, a fifth reference voltage, a sixth reference, and a seventh reference voltage;

said fourth reference voltage is a common midpoint voltage of said alternating driving voltages;

a first region is defined by voltages between said system voltage and said first reference voltage, and driven by a positive polarity;

a second region is defined by voltages between said first reference voltage, and said second reference voltage, and driven by a positive polarity;

a third region is defined by voltages between said second reference voltage and said third reference voltage, and driven by a positive polarity;

a fourth region is defined by voltages between said third reference voltage and said fourth reference voltage, and driven by a positive polarity;

a fifth region is defined by voltages between said fourth reference voltage and said fifth reference voltage, and driven by a negative polarity;

a sixth region is defined by voltages between said fifth reference voltage and said sixth reference voltage, and driven by a negative polarity;

a seventh region is defined by voltages between said sixth reference voltage and said seventh reference voltage, and driven by a negative polarity;

a eighth region is defined by voltages between said seventh reference voltage and said ground, and driven by a negative polarity.

16. A power-saving data driving method for stepwisely applying alternating driving voltages with a predetermined number of steps to a plurality of data lines in a liquid crystal display, said driving method comprising:

providing clock signals for stepwisely charging and discharging by a clocking means;

providing a plurality of reference voltages distributed between a system voltage and a ground as steps of said stepwisely charging and discharging; and

providing a plurality of analog voltage driver, wherein each said plurality of analog voltage driver corresponds to one of said plurality of data lines;

stepwisely driving a given pixel from a driving voltage of a last pixel as a beginning voltage to a driving voltage of said given pixel as a target voltage, wherein said reference voltages between said beginning voltage and said target voltage are turned-on in order according to said clock signals generated by said clocking means.

17. The power-saving data driving method of claim 16, wherein said predetermined number of steps is four and there are three reference voltages, wherein:

said three reference voltages includes a first reference voltage, a second reference voltage, and a third reference;

said second reference voltage is a common midpoint voltage of said alternating driving voltages;

a first region is defined by voltages between said system voltage and said first reference voltage, and driven by a positive polarity;

a second region is defined by voltages between said first reference voltage and said second reference voltage, and driven by a positive polarity;

a third region is defined by voltages between said second reference voltage and said third reference voltage, and driven by a negative polarity;

a fourth region is defined by voltages between said third reference voltage and said ground, and driven by a negative polarity.

18. The power-saving data driving method of claim 17, wherein said first reference voltage is 75% of said system voltage and said third reference voltage is 25% of said system voltage.

19. The power-saving data driving method of claim 17, wherein said first reference voltage is a voltage corresponding to positive polarity with 50% of optical transmission rate, and said third reference voltage is a voltage corresponding to negative polarity with 50% of optical transmission rate.

20. The power-saving data driving method of claim 17, wherein said first reference voltage is a positive voltage obtained by charging/discharging a capacitor connected to said analog voltage driver a plurality of times; said second reference voltage is obtained by charging/discharging a capacitor connected to said analog voltage driver a plurality of times, and said third reference voltage is a negative voltage obtained by charging/discharging a capacitor connected to said analog voltage driver a plurality of times.

21. The power-saving data driving method of claim 17, wherein said given pixel is stepwisely driven from said driving voltage of said last pixel to said third reference voltage, to said second reference voltage, to said first reference voltage, and finally to said driving voltage of said give pixel when said driving voltage of said given pixel is located in said first region and said driving voltage of said last pixel is located in said fourth region.

22. The power-saving data driving method of claim 17, wherein said given pixel is stepwisely driven from said driving voltage of said last pixel to said first reference voltage, to said second reference voltage, to said third reference voltage, and finally to said driving voltage of said give pixel when said driving voltage of said given pixel is located in said fourth region and said driving voltage of said last pixel is located in said first region.

23. The power-saving data driving method of claim 17, wherein said given pixel is stepwisely driven from said driving voltage of said last pixel to said second reference voltage and finally to said driving voltage of said give pixel when said driving voltage of said given pixel is located in said second region and said driving voltage of said last pixel is located in said third region.

24. The power-saving data driving method of claim 17, wherein said given pixel is stepwisely driven from said driving voltage of said last pixel to said second reference voltage and finally to said driving voltage of said give pixel when said driving voltage of said given pixel is located in said third region and said driving voltage of said last pixel is located in said second region.

25. The power-saving data driving method of claim 17, wherein said given pixel is stepwisely driven from said driving voltage of said last pixel to said second reference voltage, to said first reference voltage, and finally to said

driving voltage of said give pixel when said driving voltage of said given pixel is located in said first region and said driving voltage of said last pixel is located in said third region.

26. The power-saving data driving method of claim **17**, wherein said given pixel is stepwisely driven from said driving voltage of said last pixel to said second reference voltage, to said third reference voltage, and finally to said driving voltage of said give pixel when said driving voltage of said given pixel is located in said fourth region and said driving voltage of said last pixel is located in said second region.

27. The power-saving data driving method of claim **17**, wherein said given pixel is stepwisely driven from said driving voltage of said last pixel to said third reference voltage, to said second reference voltage, and finally to said driving voltage of said give pixel when said driving voltage of said given pixel is located in said second region and said driving voltage of said last pixel is located in said fourth region.

28. The power-saving data driving method of claim **17**, wherein said given pixel is stepwisely driven from said driving voltage of said last pixel to said first reference voltage, to said second reference voltage, and finally to said driving voltage of said give pixel when said driving voltage of said given pixel is located in said third region and said driving voltage of said last pixel is located in said first region.

29. The power-saving data driving method of claim **16**, wherein said predetermined number of steps is two and a common midpoint voltage of said alternating driving voltages is defined as a reference voltages, wherein a first region is defined by voltages between said system voltage and said reference voltage and driven by positive polarity, and a second region is defined by voltages between said reference voltage and said ground, and driven by negative polarity.

30. The power-saving data driving method of claim **16**, wherein said predetermined number of steps is eight, and there are seven reference voltages, wherein:

said seven reference voltages includes a first reference voltage, a second reference voltage, a third reference voltage, a fourth reference voltage, a fifth reference voltage, a sixth reference, and a seventh reference voltage;

said fourth reference voltage is a common midpoint voltage of said alternating driving voltages;

a first region is defined by voltages between said system voltage and said first reference voltage, and driven by a positive polarity;

a second region is defined by voltages between said first reference voltage and said second reference voltage, and driven by a positive polarity;

a third region is defined by voltages between said second reference voltage and said third reference voltage, and driven by a positive polarity;

a fourth region is defined by voltages between said third reference voltage and said fourth reference voltage, and driven by a positive polarity;

a fifth region is defined by voltages between said fourth reference voltage and said fifth reference voltage, and driven by a negative polarity;

a sixth region is defined by voltages between said fifth reference voltage and said sixth reference voltage, and driven by a negative polarity;

a seventh region is defined by voltages between said sixth reference voltage and said seventh reference voltage, and driven by a negative polarity;

a eighth region is defined by voltages between said seventh reference voltage and said ground, and driven by a negative polarity.

* * * * *

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United States Patent [19]

Koma

[11] Patent Number: 5,608,556

[45] Date of Patent: Mar. 4, 1997

[54] **LIQUID CRYSTAL DISPLAY HAVING ORIENTATION CONTROL ELECTRODES FOR CONTROLLING LIQUID CRYSTAL ORIENTATION**

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[73] Assignee: **Sanyo Electric Co., Ltd.**, Osaka, Japan

[21] Appl. No.: **263,871**

[22] Filed: **Jun. 21, 1994**

[30] **Foreign Application Priority Data**

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Jul. 8, 1993	[JP]	Japan	5-169087
Nov. 25, 1993	[JP]	Japan	5-295731
Apr. 28, 1994	[JP]	Japan	6-092283

[51] **Int. Cl.**[6] **G02F 1/1343**; G02F 1/135; G02F 1/1337

[52] **U.S. Cl.** **349/143**; 349/42; 349/116; 349/123

[58] **Field of Search** 359/54, 59, 75, 359/87, 72

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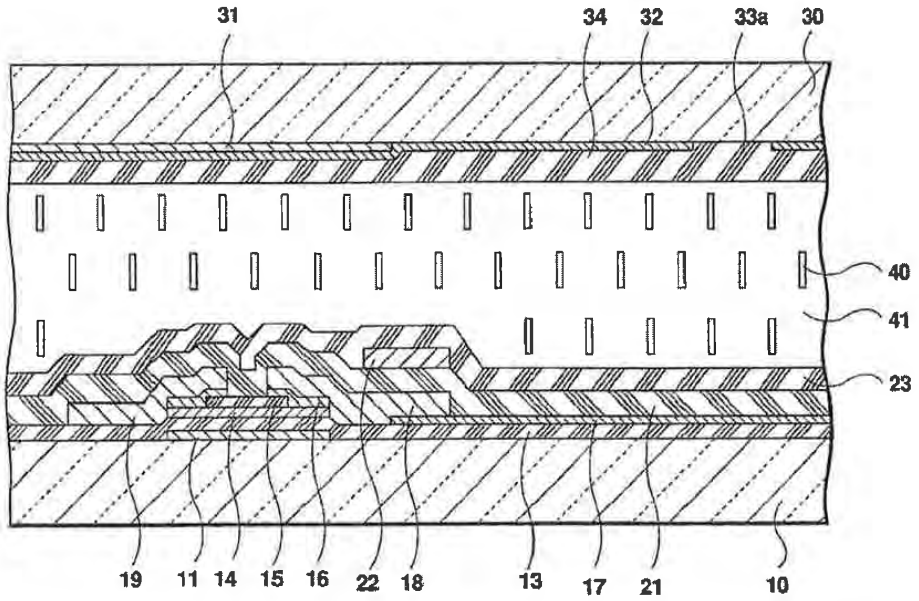
Primary Examiner—Sara W. Crane
Assistant Examiner—Fetsum Abraham
Attorney, Agent, or Firm—Loeb & Loeb LLP

[57] **ABSTRACT**

In a liquid crystal display of TFT active matrix type, the direction of orientation vectors of liquid crystal molecules are controlled for providing a wide viewing angle and preventing occurrence of disclination from making a rough display screen. With an orientation control electrode disposed on the periphery of a display electrode, an orientation control window, an electrode nonexistent portion, is formed in a common electrode and the potential difference between the orientation control electrode and the common electrode is set smaller than that between the display electrode and the common electrode. Alternatively, an orientation control window is likewise formed in the display electrode and the potential difference between the orientation control electrode, and the common electrode is set larger than that between the display electrode and the common electrode.

22 Claims, 14 Drawing Sheets



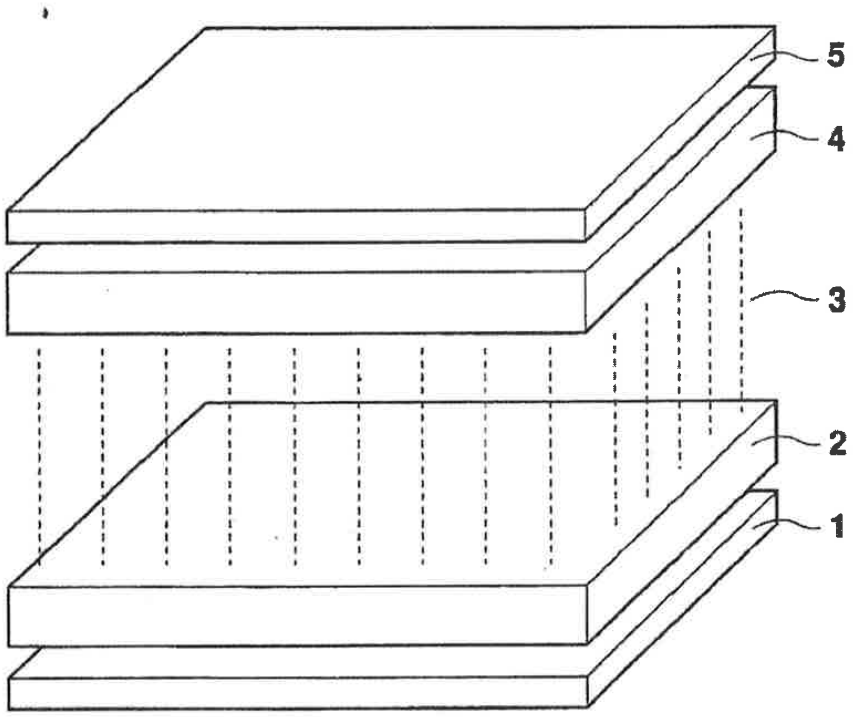


Fig. 1 PRIOR ART

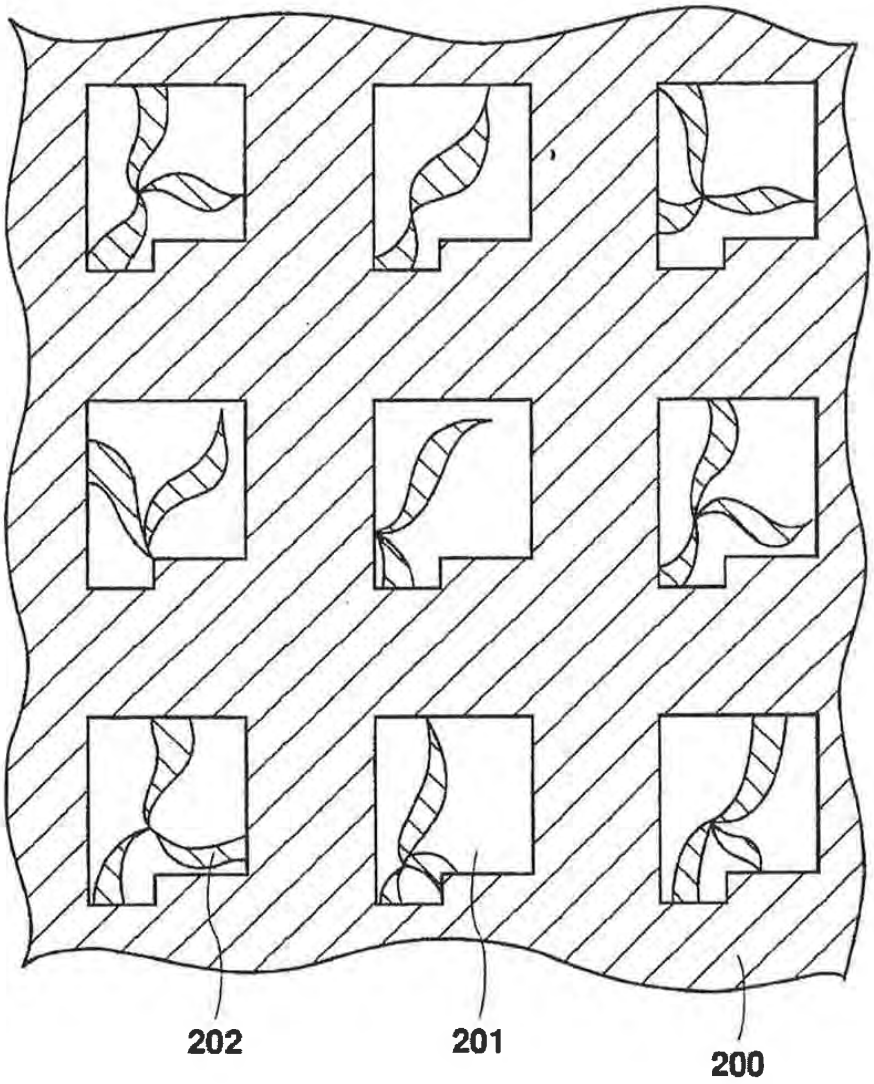


Fig. 2 PRIOR ART

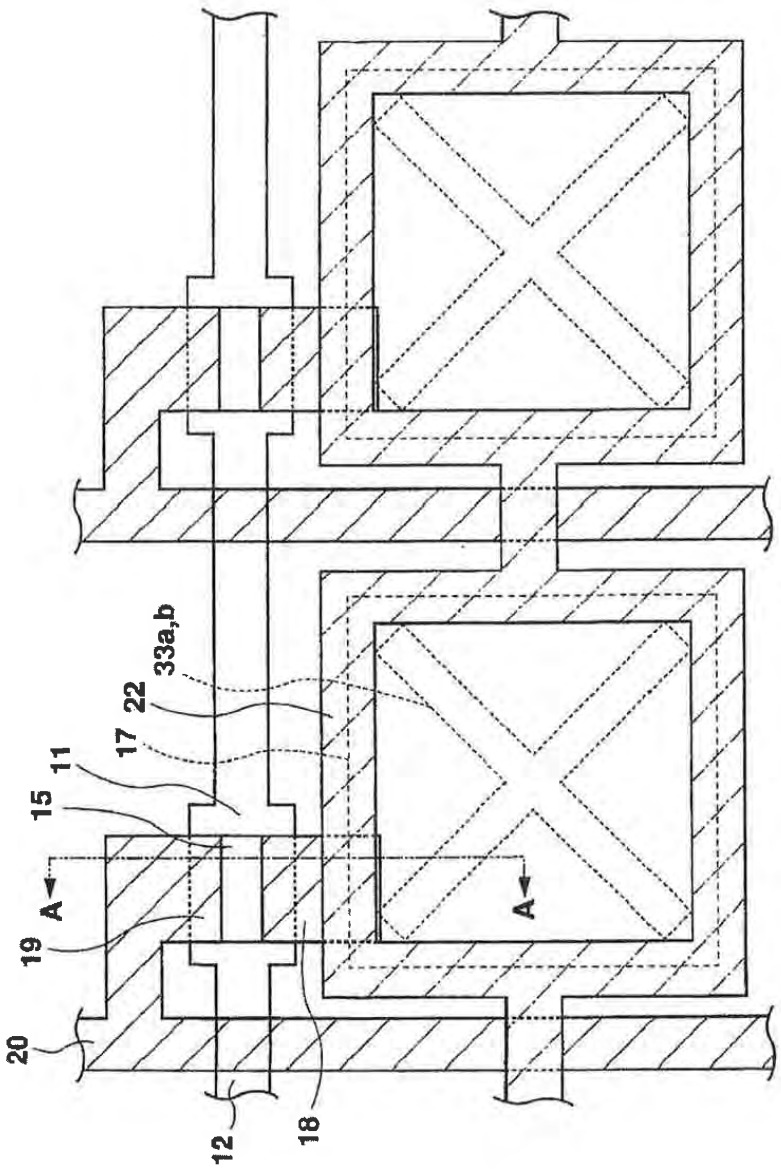


Fig. 3

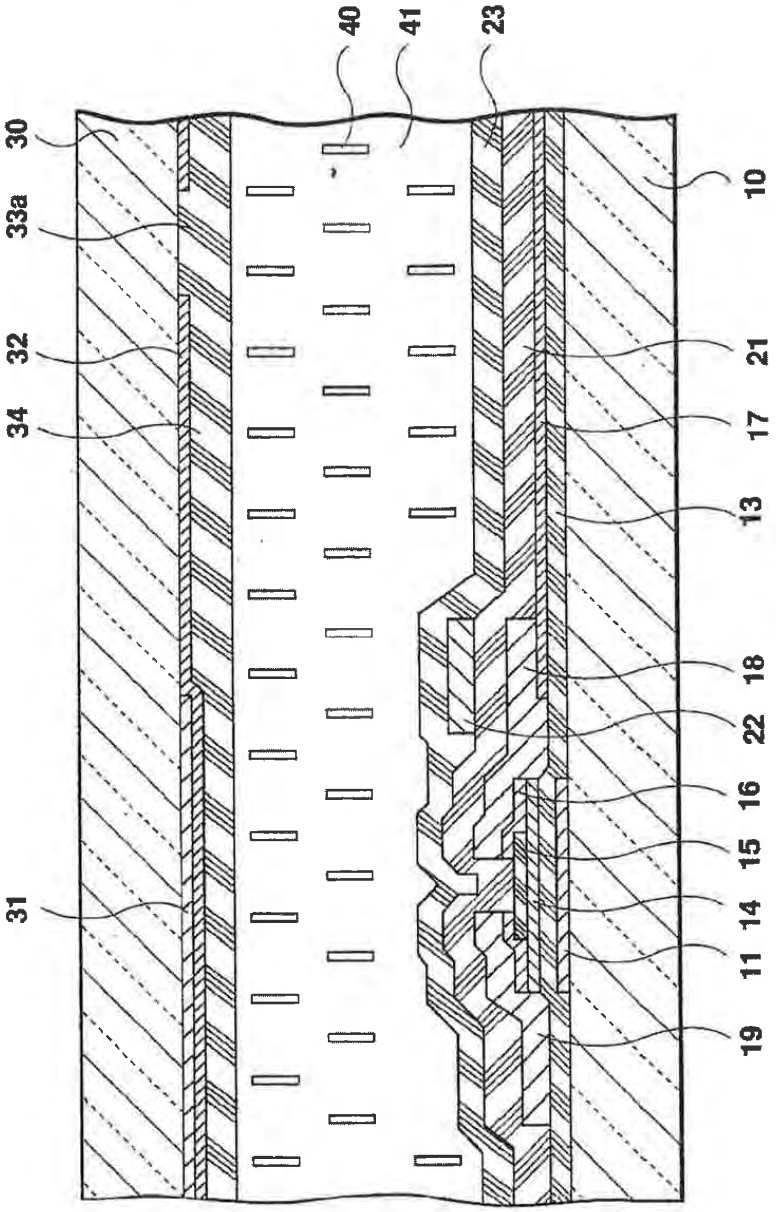


Fig. 4

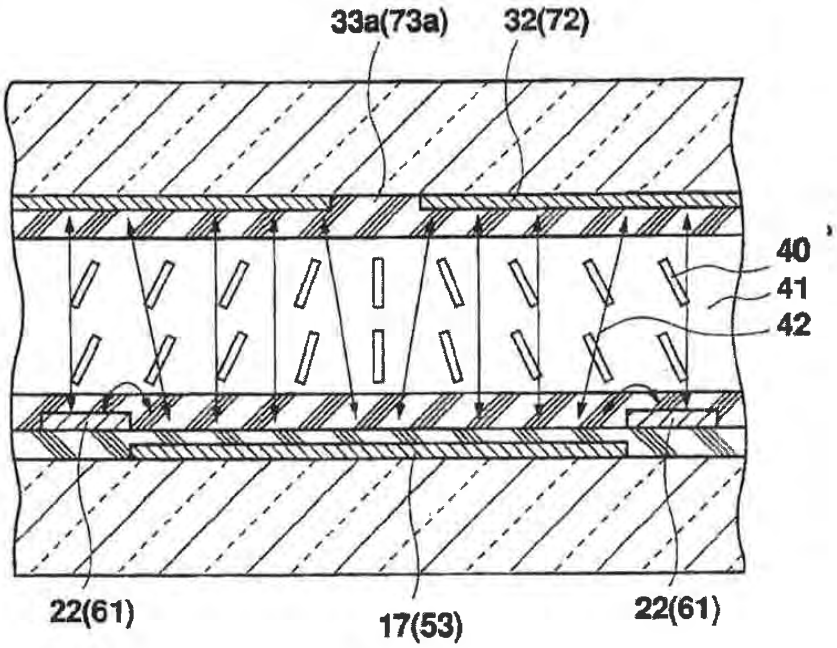


Fig. 5

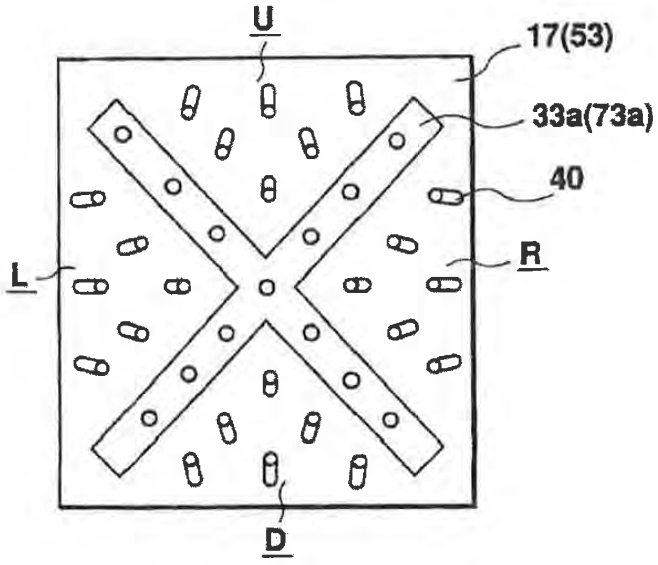


Fig. 6

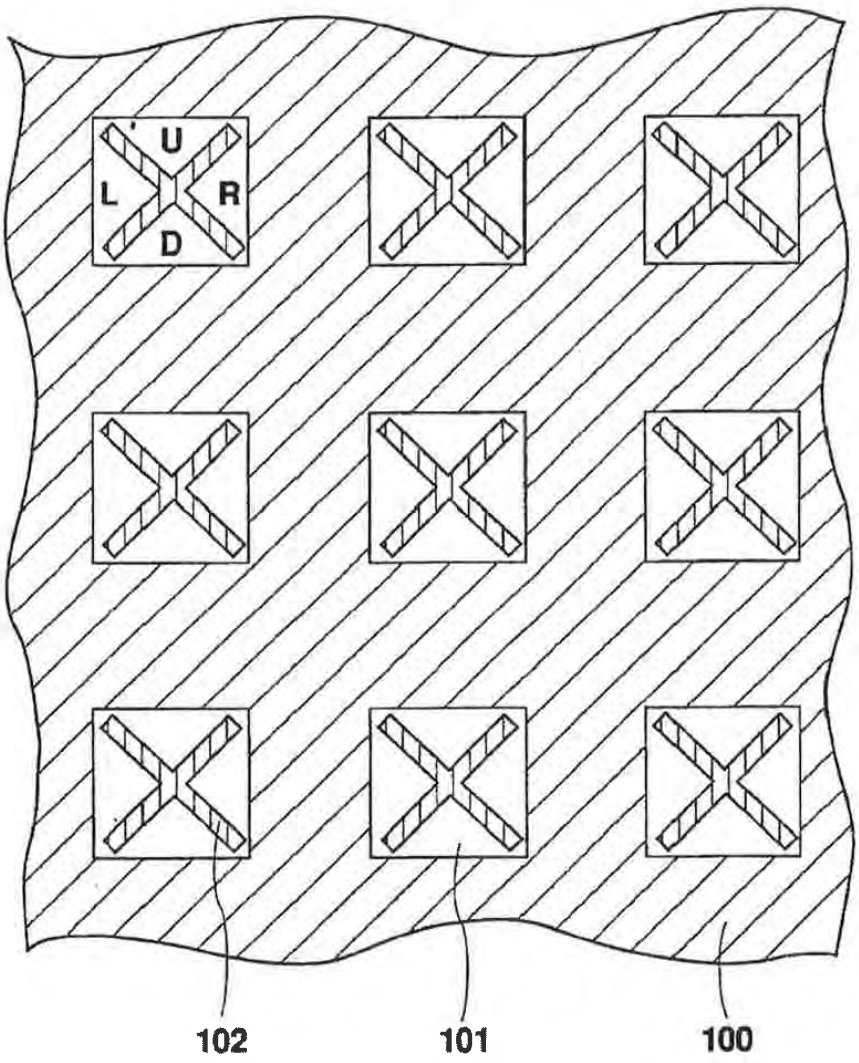


Fig. 7

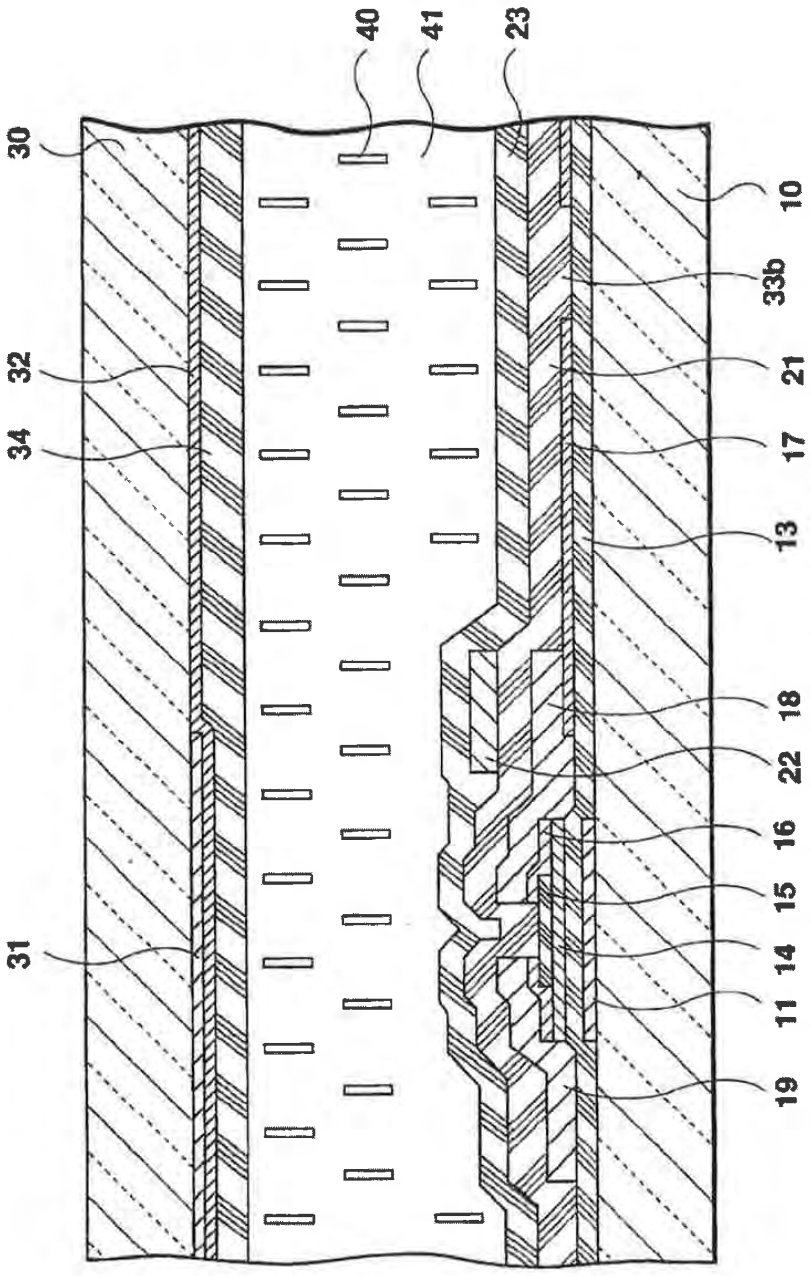


Fig. 8

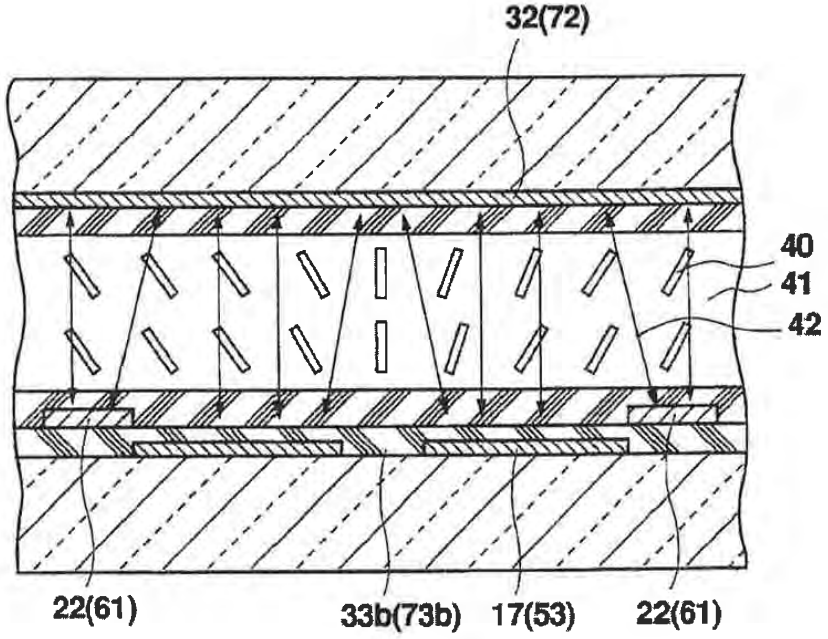


Fig. 9

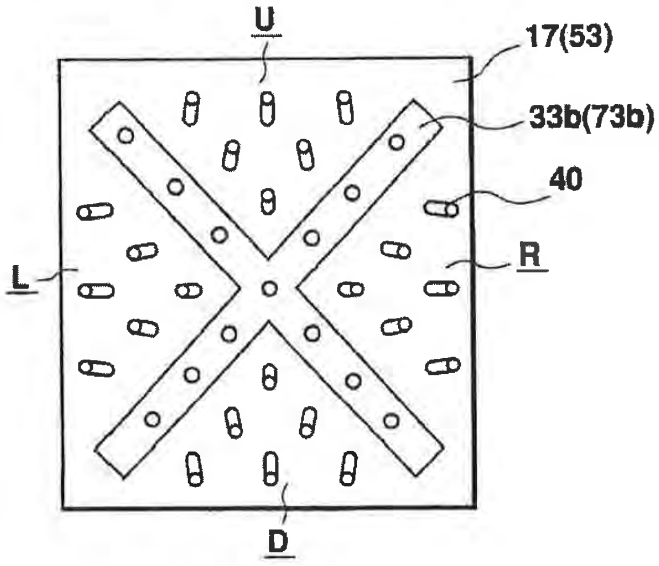


Fig. 10

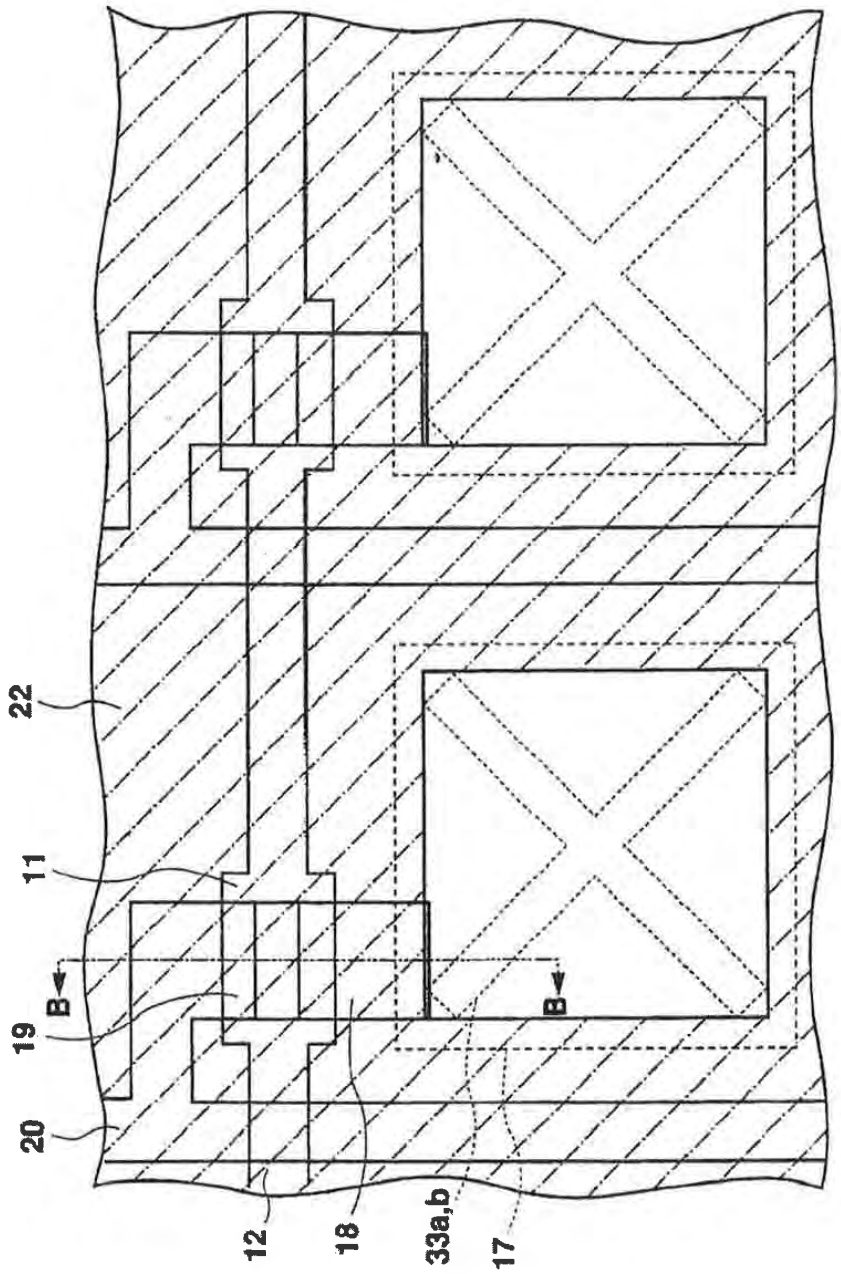


Fig. 11

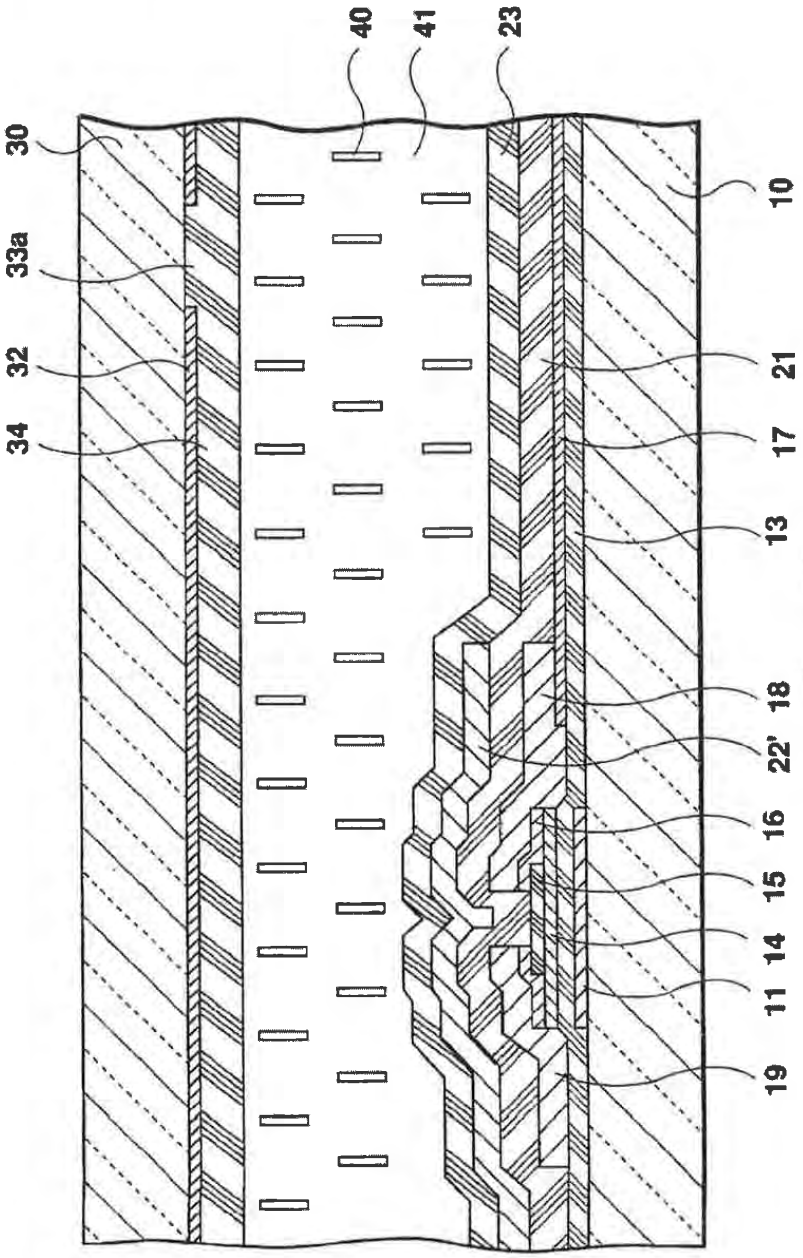


Fig. 12

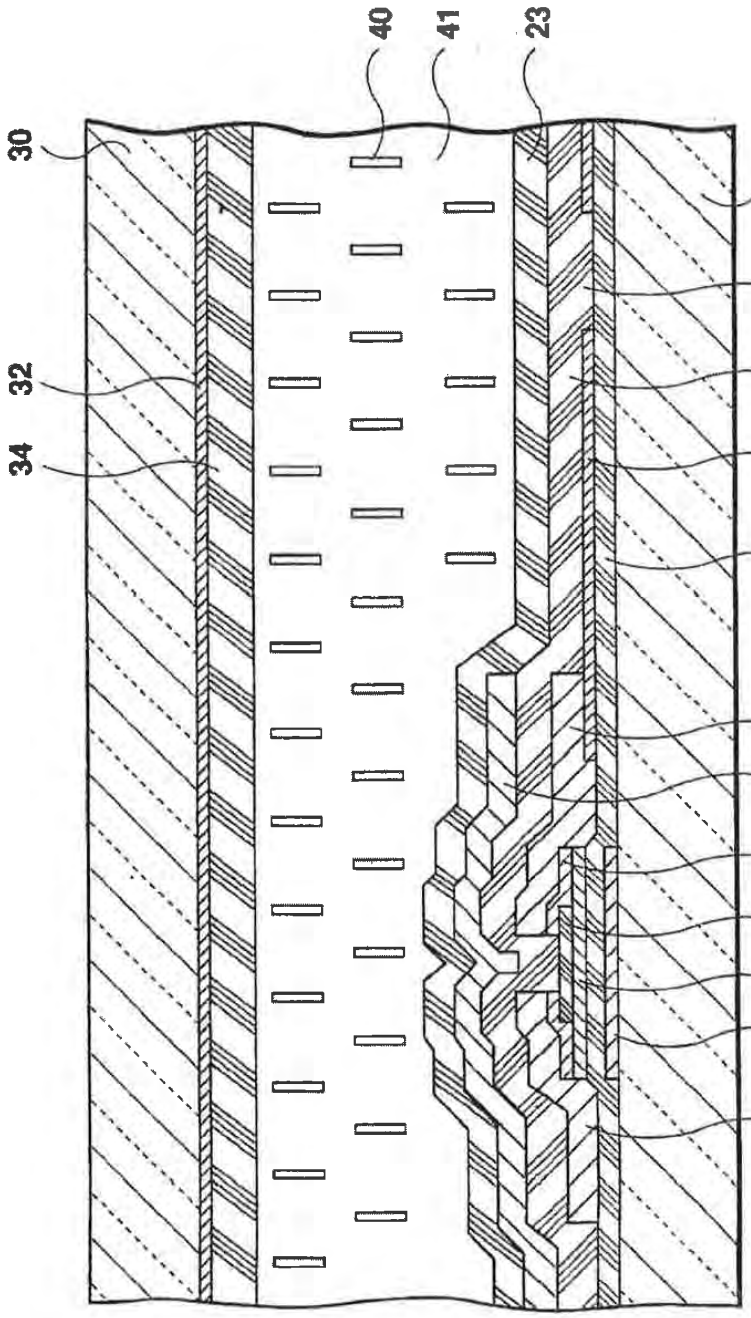


Fig. 13

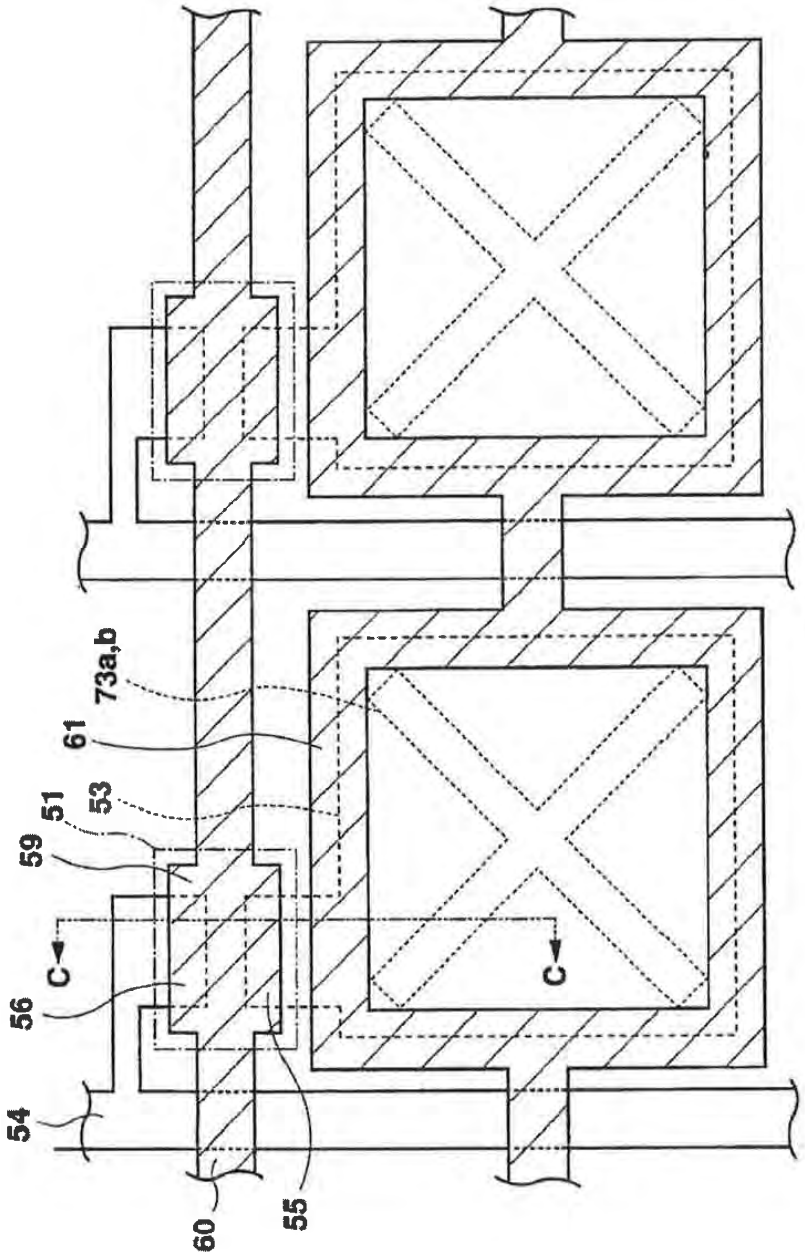


Fig. 14

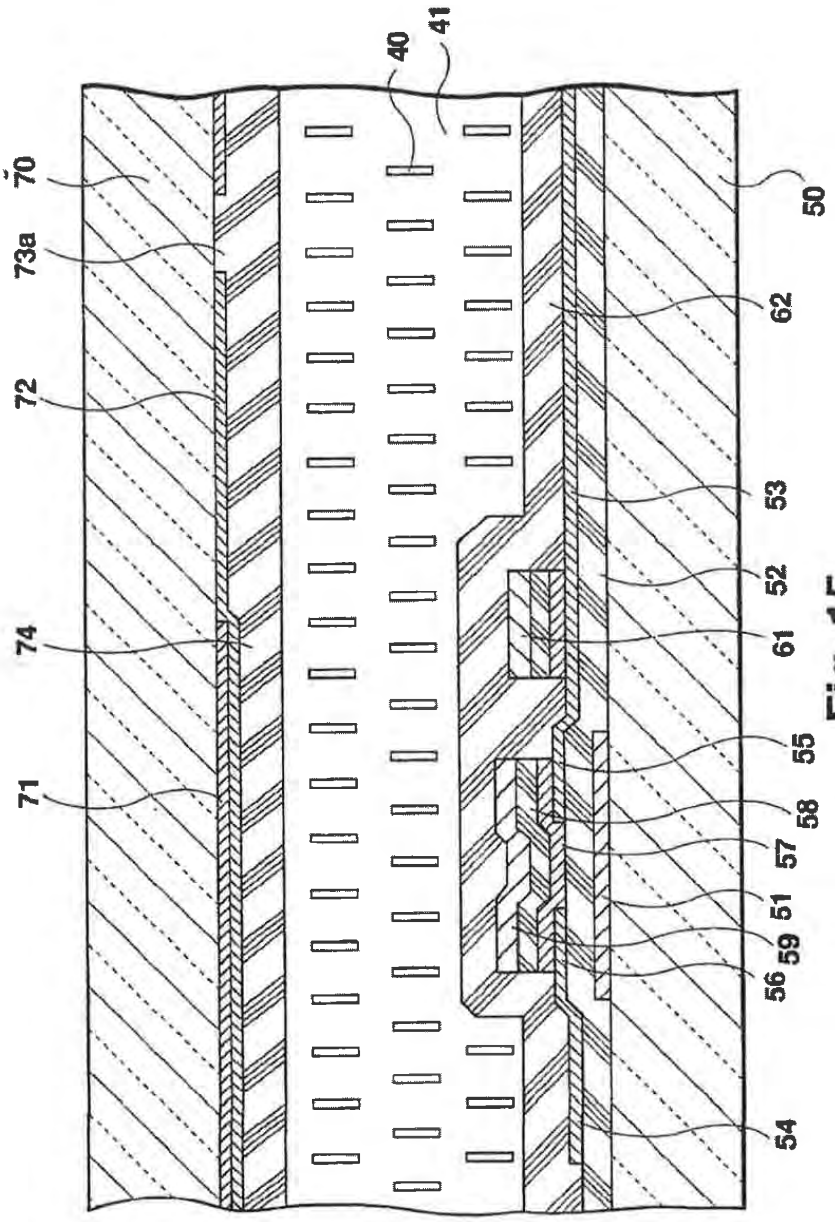


Fig. 15

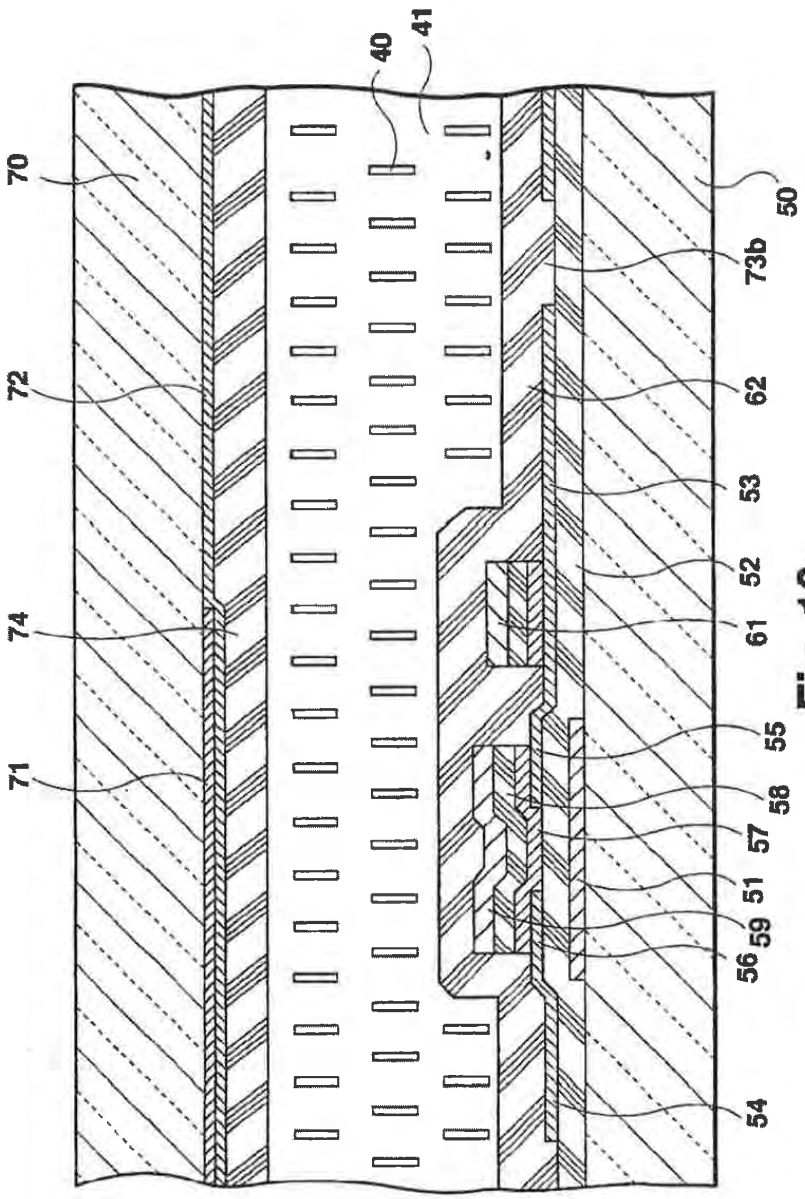


Fig. 16

LIQUID CRYSTAL DISPLAY HAVING ORIENTATION CONTROL ELECTRODES FOR CONTROLLING LIQUID CRYSTAL ORIENTATION

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to a liquid crystal display and more particularly to a liquid crystal display which provides a wide viewing angle and high display quality by controlling the orientation of liquid crystal directors.

2. Description of the Related Art

Liquid crystal displays have the advantages of their small size, slim form, and low power consumption. Therefore, they are becoming increasingly commercially practical for use in office automation machines, audio and visual machines, and the like. Particularly, the liquid crystal displays of the active matrix type using thin-film transistors (TFTs) as switching elements, which can display high-definition dynamic images, are used for television displays, etc.

To form the liquid crystal display, as shown in FIG. 1, a TFT substrate 2 comprising TFTs, display electrodes, etc., disposed like a matrix on a transparent substrate such as glass, and an opposed substrate 4 having common electrodes are affixed with a several μm thick liquid crystal layer 3 between, and both the substrates affixed to each other are sandwiched between two polarization plates 1 and 5 perpendicular to each other in a polarization axis direction.

The TFT substrate 2 has a structure in which TFTs are formed around the intersections of gate lines (scanning lines) and drain lines (data lines) and display electrodes located like a matrix are connected to the TFTs. The gate lines are scanned and selected in order, thereby turning on all TFTs on the same scanning line. Data signals synchronized with the turning on of the TFTs are supplied to the display electrodes on the drain lines. The common electrodes are also set to a predetermined potential in synchronization with gate line scanning, thereby applying a predetermined potential difference to display picture element capacitors formed by the common electrodes and opposite display electrodes for driving the liquid crystal.

Particularly, in the liquid crystal display using the ECB (electrically controlled birefringence) system, voltage is applied to display electrodes and common electrodes for controlling the orientation state of liquid crystal directors and a birefringence change is made in white light incident from a light source to provide an optical switch function. For example, a nematic crystal liquid having negative anisotropy of dielectric constant is used as the liquid crystal layer 3 and the initial orientation of liquid crystal directors is set to the direction vertical to the substrate face; the liquid crystal display of this type is called VAN (vertically aligned nematic) type.

In FIG. 1, white light incident from the TFT substrate 2 is passed through the first polarization plate 1 and results in linear polarization only. When no voltage is applied, the incident linear polarization is not subjected to birefringence in the liquid crystal layer 3, and thus is shut off by the second polarization plate 5 and black is displayed (normally black mode). When a predetermined voltage is applied to the liquid crystal layer 3, the orientation of the liquid crystal directors changes to the direction in which the orientation vector of the liquid crystal molecules having negative dielectric constant anisotropy approach a right angle with the electric field direction. Since a liquid crystal has anisotropy in refractive index, the linear polarization incident on the liquid crystal layer is subjected to birefringence and becomes elliptic polarization and light is transmitted through the second polarization plate 5. The transmitted light strength in the liquid crystal display depends on the voltage applied to the liquid crystal layer. Therefore, gradation display is enabled by adjusting the applied voltage for each picture element; light and dark (monochrome) display at the picture elements is visible as a predetermined display image on the entire display.

In the VAN type, macromolecular films of polyimide (S1Nx) are formed on the surfaces of both substrates 2 and 4 and rubbing treatment is applied to the films, thereby giving a predetermined pretilt angle to the initial vertical orientation of the liquid crystal directors for controlling the orientation of the liquid crystal directors. Further, for example, the opposed substrate 4 is formed with a color filter installed on an optical path and the color capability is combined with the optical shutter effect of ECB to provide color display.

FIG. 2 is a plan view showing a light transmission state when the conventional liquid crystal display using the ECB system shown in FIG. 1 is driven. Although not discussed in the description given so far, a shielding film made of metal, etc., is normally formed on the opposed substrate for shutting off transmission of light except for openings **201** corresponding to the picture elements arranged like a matrix. In the shield area **200**, light leakage between the picture elements is prevented and the shield area **200** is displayed in black, thereby improving display contrast. In each opening **201**, the transmission rate of light is controlled to provide the desired display; a black area called disclination **202** also occurs in the opening **201**. When a plurality of areas differ in orientation vector of liquid crystal, the orientation of liquid crystal directors is disarranged on boundaries between the areas, and the area indicating a transmission rate different from that in other areas is the disclination.

For liquid crystal directors in nematic phase, the orientation vector, when voltage is applied, is restricted only at an angle with the electric field direction and the azimuth with the electric field direction as an axis is released. That is, with the electric field effect only, an orientation vector oriented to a plurality of directions obtained by rotating with the electric field direction as the axis of symmetry is possible. On the other hand, the TFT substrate has electrode irregularities on the surface and surface orientation treatment is uneven. An electric field in a lateral direction exists due to the potential difference between the electrodes in a liquid crystal cell. Therefore, areas different in orientation vector of liquid crystal molecules occur in the cell. If an orientation vector error exists even partially, since liquid crystal has a continuum property, orientation vectors having an azimuth following the liquid crystal having the erroneous orientation vectors extend over a certain area. If such a phenomenon occurs at more than one place in the cell, more than one area has orientation vectors which are the same in angle with the electric field direction, but differ in azimuth. On the boundaries between the areas, the light transmission rate differs from that in other areas, causing disclination to occur. If disclination of different form for each picture element occurs frequently, the display screen will have a rough surface and the expected color display will not be provided.

If orientation vectors of liquid crystal molecules in each area become irregular in the display area, there is a chance that viewing angle dependency will arise.

On the other hand, in the VAN type, etc., due to static electricity occurring during rubbing treatment, TFT thresh-

old or mutual conductance shift results in electrostatic discharge damage, etc.

SUMMARY OF THE INVENTION

It is therefore an object of the invention to provide a solution to the above-mentioned problems.

To this end, according to the invention, there is provided a liquid crystal display comprising a first substrate and a second substrate. The first and second substrates are located facing each other with a liquid crystal layer therebetween. The display also includes a plurality of display electrodes located like a matrix and switching elements connected to the display electrodes. The display elements and the switching elements are formed on the liquid crystal layer side of the first substrate, and a common electrode is formed on the liquid crystal layer side of the second substrate, so that when a predetermined voltage is applied to the liquid crystal layer for display. The improvement is orientation control electrodes formed on the first substrate and which are electrically insulated from the display electrodes. Also, a potential different from that of the display electrode is applied to the orientation control electrode for controlling the orientation of the liquid crystal.

Thus, the orientation control electrodes to which a potential different from that of the display electrodes is applied are provided, so that the electric field in liquid crystal cells can be securely controlled according to the potential differences between the orientation control electrode and the common electrode and between the display electrode and the common electrode. It is also made possible to specify the azimuth of orientation vectors of liquid crystal molecules.

The electric field direction in the liquid crystal cell is inclined toward a predetermined direction from the normal direction of the substrate according to the effective potential difference between the display and orientation control electrodes. When a voltage is applied to the liquid crystal layer by both the electrodes, a predetermined angle occurs between the initial orientation direction of liquid crystal directors and the electric field direction. Thus, the liquid crystal directors incline in a direction to increase the angle of the electric field direction with the initial orientation direction in the shortest way. A determination is made to only one orientation vector of the liquid crystal molecules.

The orientation control electrodes may be formed in all areas except the formation area of the display electrodes or at least surrounding the periphery of the display electrodes.

If the orientation control electrode is located so as to surround the periphery of the display electrode, liquid crystal directors are subjected to equal orientation control on four sides of the display electrode. The orientation vectors of liquid crystal molecules incline at right angles to each side. Since the liquid crystal molecules have a continuum property, if the orientation state is controlled on each side of the display electrode, they are aligned to substantially equal orientation vectors to the center of the display electrode. Therefore, display quality can be improved.

If the orientation control electrodes are formed in all areas except the formation area of the display electrodes, light leakage in the non-display area can be prevented, eliminating the need for installing a shielding film on the opposed substrate side.

Further, if the orientation control electrodes are formed partially overlapping the display electrodes, light leakage in the non-display area can be securely prevented. Therefore, if a shielding film is formed on the opposed substrate side, an alignment margin can be set with the outer peripheral edge of the orientation control electrode as a reference, thereby reducing the margin to affix substrates for preventing the aperture ratio of the liquid crystal display from lowering.

An orientation control window containing no electrode may be formed in the picture element area of the common electrode or the display electrode. No electric field occurs in the window portion and liquid crystal directors are fixed to the initial orientation state. Therefore, the orientation control electrode and window enable the orientation vectors of the liquid crystal molecules to be fixed in one direction near the orientation control electrode and window. Because of the continuum property of liquid crystal, the orientation vectors of the liquid crystal molecules in the display electrode are aligned. Further, the orientation control window enables the boundaries between areas different in azimuth of orientation vectors in the display area to be fixed without variations from one picture element to another.

If the orientation control window is formed in the picture element area of the common electrode, the effective potential difference between the orientation control electrode and the common electrode is set smaller than that between the display electrode and the common electrode. On the other hand, if the orientation control window is formed in the picture element area of the display electrode, the effective potential difference between the orientation control electrode and the common electrode is set larger than that between the display electrode and the common electrode.

Near the edge of the orientation control window, an electric field occurs slantingly from the electrode existent area to the electrode nonexistent area in the liquid crystal layer. That is, the electric field occurring from the electrode opposed to the orientation control window avoids the orientation control window and moves to the electrode existent portion.

Therefore, the inclined direction of the electric field defined by the orientation control electrode and that defined by the orientation control window match in each zone of each picture element area, uniformly defining the orientation state of the liquid crystal molecules.

Particularly, if the orientation control window is formed like an X character, the orientation state of each picture element area is divided into four equal zones. Therefore, when an image is displayed, transmitted light in the four zones is composed, providing a liquid crystal display having low viewing angle dependency with four optimum viewing directions and a wide viewing angle.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings:

FIG. 1 is a structural drawing of a conventional liquid crystal display;

FIG. 2 is a plan view illustrating problems on the conventional liquid crystal display;

FIG. 3 is a plan view of a liquid crystal display according to a first or second embodiment of the invention;

FIG. 4 is a sectional view taken on line A—A in FIG. 3;

FIG. 5 is a sectional view illustrating the function and effect of the first embodiment;

FIG. 6 is a plan view illustrating the function and effect of the first embodiment;

FIG. 7 is a plan view illustrating the function and effect of the invention;

FIG. 8 is a sectional view taken on line A—A in FIG. 3;

FIG. 9 is a sectional view illustrating the function and effect of the second embodiment;

FIG. 10 is a plan view illustrating the function and effect of the second embodiment;

FIG. 11 is a plan view of a liquid crystal display according to third and fourth embodiments of the invention;

FIG. 12 is a sectional view taken on line B—B in FIG. 11;

FIG. 13 is a sectional view of a structure different from FIG. 12, taken on line B—B in FIG. 11;

FIG. 14 is a plan view of a liquid crystal display according to a fifth or sixth embodiment of the invention;

FIG. 15 is a sectional view taken on line C—C in FIG. 14; and

FIG. 16 is a sectional view taken on line C—C in FIG. 14.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to the accompanying drawings, there are shown preferred embodiments of the invention.

A first embodiment of the invention will be discussed. FIG. 3 is a plan view of a TFT substrate showing an electrode pattern of two picture elements. Gate lines 12 and drain lines 20 are crossed on the substrate. A display electrode 17 is located in the area surrounded by the gate lines 12 and the drain lines 20. A TFT is formed at the intersection of both the lines 12 and 20 or around the intersection, and a source electrode of the TFT 18 is connected to the display electrode 17. An orientation control electrode 22 is located so as to surround the periphery of the display electrode 17 and they are connected to each other in the row direction (the direction substantially parallel to the gate line). The X letter area indicated by the dotted line in FIG. 3 denotes an orientation control window 33*a* formed as an electrode nonexistent portion at a common electrode formed on an opposed substrate (not shown). The orientation control window 33*a* corresponds to the display electrode on the TFT substrate as a plane.

A more detailed description will be given in conjunction with FIG. 4, which is a sectional view taken on line A—A in FIG. 3. An about 1500Å thick gate electrode 11 and gate line 12 formed by sputtering and photoetching Cr, for example, are located on a transparent substrate 10 such as glass. SiNx is laminated by CVD (chemical vapor deposition) on almost the full face of the substrate so as to cover the gate electrode 11 and gate line 12 to form a gate insulation film 13, which is about 2000Å–4000Å thick. Following the gate insulation film 13, a-Si (amorphous silicon) 14, etching stopper 15, and N⁺a-Si 16 are laminated on the gate electrode 11 like an island by CVD film forming and photoetching, whereby channel and contact layers of the TFT are formed. On the other hand, in a different area on the gate insulation film 13 where the gate electrode 11 is not formed, an about 1000Å thick display electrode 17 is formed by sputtering and photoetching of ITO (indium tin oxide), transparent conductive material. The top layer is source drain wiring. A source electrode 18, drain electrode 19, and drain line 20 are formed by photoetching a pattern of Mo/Al laminated at a thickness of 1000Å/7000Å by sputtering, for example.

The following describe a general structure of the TFT substrate. In the present application, the full face is coated with an interlayer insulation film 21 such as SiNx, then an orientation control electrode 22 is disposed so as to surround the periphery of the display electrode 17. SiNx is laminated at a thickness of 0.5–1 μm by CVD, etc. The orientation control electrode 22 is formed on the interlayer insulation film 21 by laminating and patterning Al, Cr, Mo, etc., for example. As shown in FIG. 3, the orientation control electrode 22 is located so as to surround the periphery of the display electrode 17 and they are connected to each other with respect to the picture element on the same row (the same gate line).

Further, an orientation film 23 such as polyimide (S1Nx) is laminated on the full face for vertical orientation as a surface orientation treatment, whereby the initial orientation of liquid crystal directors 40 is defined in the normal direction of the substrate. Rubbing treatment of the orientation film 23 is not required.

In the invention, the TFT substrate is not limited to the structure mentioned here.

On the other hand, a shielding film 31 for opening each picture element portion and shutting off transmission of light through non-display portions is formed by Cr, etc., on a transparent substrate (opposed substrate) 30 facing the TFT substrate with a liquid crystal layer 41 therebetween. The full face of the shielding film 31 is coated with ITO for forming a common electrode 32. The display area of each picture element of the common electrode 32 is etched like an X letter as indicated by the dotted line in FIG. 3 for forming an orientation control window 33*a*, an electrode non-existent portion at the common electrode 32. Further, a vertical orientation film 34 as on the TFT substrate is formed on the full face of the substrate 30 on the common electrode 32 and the orientation control window 33*a* for completing the opposed substrate. The common electrode 32 is connected to the TFT substrate side by silver paste, etc., at four corners of the substrate and a signal is applied from an input terminal installed on the TFT substrate side. The orientation control electrode 22 connected for each row is also connected to the input terminal in common and the same signal as the common electrode is input.

FIG. 5 is a sectional view showing the operation in the cell when the liquid crystal display in the embodiment is driven. The orientation control electrode 22 is located on both sides of the display electrode 17. They face the common electrode 32 with the liquid crystal layer 41 therebetween. In the embodiment, the effective potential difference between the orientation control electrode 22 and the common electrode 32 is set smaller than that between the display electrode 17 and the common electrode 32. Therefore, in the periphery of the display area, an electric field 42 occurs from the display electrode 17 to the common electrode 32 in a slant direction from within the display area to the outside of the display area, thereby specifying the angle of the orientation vector of liquid crystal directors 40 with the electric field 42 and the azimuth with the electric field direction as an axis. That is, if the initial orientation vector is at some angle with the electric field direction, elasticity based on a continuum property of the liquid crystal causes the orientation vector to change in a direction to increase the angle in the shortest way when an electric field is applied, so that stable energy is provided. This effect is point symmetry in relation to four sides of the display electrode 17, as shown in FIG. 6. Since the orientation control window 33*a* in the common electrode 32 contains no electrode, a weak or no electric field occurs around the orientation control window 33*a* and the liquid crystal directors 40 are fixed to the initial orientation state.

Thus, for the liquid crystal directors 40, the orientation vector direction is specified as point symmetry in relation to

the four sides of the display area by the effect of the orientation control electrode **22** and the boundaries between areas different in orientation vector are fixed by the orientation control window **33***a*. Because of the continuum property of liquid crystals, orientation vectors can be restricted symmetrically at all picture elements and uniformly in their respective zones. The picture element display section is divided into four zones separated by the orientation control window **33***a*, U, D, L, and R. For example, in visual recognition from the upper direction of the screen, average transmitted light in zones U and D and composite light in zones L and R are recognized as transmitted light near the condition of visual recognition from the front. With respect to other directions, likewise, transmitted light equivalent to that on the front is recognized, reducing viewing angle dependency for providing a wide viewing angle.

FIG. **7** is a plan view showing a light transmission state when the liquid crystal display in the embodiment is driven. Openings **101** are arranged like a matrix in a black area **100** provided by the shielding film. Display is made as macroscopic composition of transmitted light corresponding to graduations controlled in the openings **101**. Each opening **101** provides a picture element shown in FIG. **6** and the boundaries **102** defined by the orientation control windows which have the same form in all openings **101** are represented in black, but variations from one picture element to another do not exist, so that the display is not adversely affected.

Thus, according to the invention, the viewing angle characteristic in horizontal and vertical directions is improved for enabling display at wide viewing angles and disclination variations from one picture element to another are suppressed for improving display quality. The function and effect described above are the same if the polarity of the applied voltage is inverted.

To drive the liquid crystal display in the embodiment, the orientation control electrode **22** is electrically connected to the common electrodes **32**, thereby eliminating the need for the driver circuit for the orientation control electrode **22**. The orientation control electrode **22** is set to the same potential as the common electrode **32**, thereby leveling the potential difference between both the electrodes **22** and **32**. Therefore, the potential difference between both the electrodes **22** and **32** becomes smaller than that between the display electrode **17** and the common electrode **32**, and electric field distribution in the cell becomes as shown in FIG. *5*.

If the orientation control electrode **22** is located near the display electrode **17**, the control function or effect of orientation vectors increases. Thus, the orientation control electrode **22** preferably abuts on the surround of the display electrode **17** as a plane or is partially superposed on the display electrode **17**.

Particularly in the invention, as shown in FIG. **3**, the orientation control electrode **22** is partially superimposed on the display electrode **17** for causing the superimposed portion to serve as substorage capacitance.

Since the structure shields transmitted light in the periphery of the display electrode **17**, the affixing margin between the substrates can be made small and the opening percentage of the shielding film **32** on the opposed substrate side can be improved. The margin can be set based on the outer periphery of the orientation control electrode **22** rather than the periphery of the display electrode **17**. Thus, the loss of the opening percentage caused by all margins can be reduced only to the alignment margin of the orientation control electrode **22** to the display electrode **17** on the TFT substrate side.

Next, a second embodiment of the invention will be discussed. The plane structure is the same as that in the first embodiment shown in FIG. **3**. The sectional structure taken on line A—A in FIG. **3** is shown in FIG. **8**. The second embodiment is characterized by the fact that the orientation control window **33***b* located in the common electrode **32** in the first embodiment is located in a display electrode **17** as indicated by reference numeral **33***b* in FIG. **8** at the corresponding position on a TFT substrate **10**. Further, the effective potential difference between an orientation control electrode **22** and a common electrode **32** is set larger than that between the display electrode **17** and the common electrode **32**. The orientation control window **33***b* is opened at the same time as formation of the display electrode **17** when ITO is patterned.

Thus, the potential difference between the orientation control electrode **22** and the common electrode **32** is larger than that between the display electrode **17** and the common electrode **32**, as indicated by arrows in FIG. **9**; so that in the periphery of the display area, an electric field **42** occurs from the common electrode **32** to the display electrode **17** in a slant direction from within the display area to the outside of the display area. On the other hand, no electric field exists around the orientation control window **33***b*. In this case, each liquid crystal director **40** has an orientation vector oriented in the direction opposite to that in FIG. **5** showing the first embodiment. Therefore, as shown in FIG. **10**, because of the continuum property of liquid crystal, the directions of the orientation vectors can be restricted as point symmetry in the display area, reducing viewing angle dependency and suppressing disclination variations from one picture element to another, as in the first embodiment.

Particularly in embodiments of the invention, the direction of the electric field **42** becomes slanted at the edge of the orientation control window **33**, as shown in FIGS. **5** and **9**. To locate the orientation control window **33***a* on the opposed substrate side in order to align electric fields **42** in the slant direction by the orientation control electrode **22**, the potential difference between the orientation control electrode **22** and the common electrode **32** is set smaller than that between the display electrode **17** and the common electrode **32**. On the other hand, to locate the orientation control window **33***b* on the TFT substrate side, the potential difference between the orientation control electrode **22** and the common electrode **32** is set larger than that between the display electrode **17** and the common electrode **32**.

The orientation control electrode **22** is placed above the layer forming the TFT in the first and second embodiments, but may be located on the same layer as the gate electrode **11** and the gate line **12**. This means that the orientation control electrode **22** can also be formed below the display electrode **17** on the plane electrode layout shown in FIG. **3**. In this case, when Cr is etched to form the gate electrode **11** and the gate line **12**, the orientation control electrode **22** can be formed at the same time, so that the manufacturing process is shortened.

The sectional structure of the TFT section is shown as in FIGS. **4** and **8** for the convenience of illustration; in fact, the liquid crystal layer **41** is 5–10 μm thick, while the TFT section film is 1–2 μm thick at most, and the picture element pitch is about 100–200 μm.

The main feature of embodiments of the invention lie in that the orientation control electrode **22** is disposed so as to surround the periphery of the display electrode **17**. Thus, macroscopically, whether the orientation control electrode **22** is formed above or below the display electrode **17** does

not introduce a serious problem. Either structure would produce the same effect as shown in FIGS. 5, 6, 9, and 10.

The basic function and effect of the third and fourth embodiments are the same as those of the first and second embodiments. FIG. 11 is a plan view common to the third and fourth embodiments. In the embodiments, an orientation control electrode 22' made of conductive material having a light non-transmission property such as Al, Cr, or Mo is located on a full face of a TFT substrate and the portion corresponding to a display area is opened by etching. That is, the orientation control electrode 22' is formed completely covering the top of the TFT, gate line 12, and drain line 20. Also, it is superposed partially on the periphery of a display electrode 17.

Sectional views taken on line B—B in FIG. 11 are shown in FIGS. 12 and 13. FIG. 12 shows the structure of the third embodiment, wherein an orientation control window 33*a* is located on the side of a common electrode 32 on an opposed substrate 30. FIG. 13 shows the structure of the fourth embodiment, wherein an orientation control window 33*b* is located on the side of a display electrode 17 on a TFT substrate 10. In the structures in FIGS. 12 and 13, the orientation control electrode 22' serves as a shielding film. Therefore, as seen in the figures, no shielding film is provided on the opposed substrate side. The structure with the shielding film located on the TFT substrate side can prevent a substrate affixing margin from reducing the effective display area and improve the aperture ratio compared with the structure with the shielding film located on the opposed substrate side.

Since the orientation control window is located on the common electrode side in the cell in FIG. 12, it is required that the effective potential difference between the orientation control electrode 22' and the common electrode 32 should be smaller than that between the display electrode 17 and the common electrode 32 as shown in FIG. 5. To meet this requirement, the orientation control electrode 22' needs to be connected to the common electrode 32 for setting to the same potential. At this time, the orientation control electrode 22' can also be actively superimposed on the display electrode 17 so that the superimposed portion is made to function as substorage capacitance at each picture element.

Next, a fifth embodiment of the invention will be discussed. FIG. 15 is a plan view showing an electrode pattern. Gate lines 60 and drain lines 54 are crossed. A display electrode 53 is located in the area surrounded by the gate lines 60 and the drain lines 54. A normal stagger type TFT is formed at the intersection of both the lines 54 and 60 or around the intersection, and a part of the display electrode 53 serves as a source electrode 56. An orientation control electrode 61 is located so as to surround the periphery of the display electrode 53 and the orientation control electrodes 61 on the same row are connected to each other in the row direction. The X letter area indicated by the dotted line in FIG. 14 is an area corresponding to a plane of an orientation control window 73*a* formed as an electrode nonexistent portion at a common electrode on an opposed substrate (not shown).

FIG. 15 is a sectional view taken on line C—C in FIG. 14. A shielding film 51 is formed by sputtering and then photoetching Cr, for example, on a transparent substrate 50 such as glass. SiNx or the like is laminated on the full face of the substrate so as to cover the shielding film 51 to form an interlayer insulation film 52. On the interlayer insulation film 52, the display electrode 53, a part of which serves as the source electrode 55, and the drain line 54, a part of which serves as a drain electrode 56, are formed by sputtering and photoetching of ITO.

A channel layer a-Si 57, a gate insulation film 58 SiNx, and a gate metal Al are laminated in order on source and drain lines (53, 54, 55, 56), and the laminate is etched with the same mask to form the gate line 60 and the orientation control electrode 61. In the area on the shielding film 51, a part of the gate line 60 is formed as a gate electrode 59 on the source and drain electrodes 55 and 56 to provide the normal stagger type TFT with the a-Si 57, gate insulation film 58, and gate electrode 59 laminated in order. Like the TFT, the orientation control electrode 22 has a 3-layer structure of a-Si, SiNx, and Al and is located so as to surround the periphery of the display electrode 53.

Further, a vertical orientation film 62 such as polyimide is formed on the full face to form a TFT substrate.

On the other hand, a shielding film 71 made of Cr is formed on a transparent substrate 70 made of glass and a common electrode 72 of ITO is formed on the full face covering the shielding film. The orientation control window 73*a* is opened by etching in the common electrode 72. Further, a vertical orientation film 74 is formed on the full face. The opposed substrate of such a structure is disposed facing the TFT substrate with a liquid crystal layer 41 therebetween. The common electrode 72 is connected to the TFT substrate side by silver paste, etc., at four corners of the liquid crystal cell.

In the structure in the embodiment, the potential difference between the orientation control electrode 61 and the common electrode 72 is set smaller than that between the display electrode 53 and the common electrode 72, as in the first embodiment, whereby the electric field distribution in the cell becomes as shown in FIG. 5 and the orientation of liquid crystal directors 40 becomes as shown in FIG. 6 as a plane. The function and effect related to the orientation of the liquid crystal directors are the same as those in the first embodiment and therefore will not be discussed again. The structure in the embodiment enables the TFT substrate to be manufactured with three masks, as seen in the description given above, thereby reducing manufacturing costs.

In the embodiment, the orientation control window located in the common electrode 72 in the fifth embodiment is located in a display electrode 53 on the corresponding TFT substrate, as indicated by reference numeral 73*b* in FIG. 16. Further, the potential difference between an orientation control electrode 61 and a common electrode 72 is set larger than that between the display electrode 53 and the common electrode 72. The orientation control window 73*b* is opened at the same time as formation of source and drain wiring (53, 54, 55, 56) when the ITO is patterned. Then, the electric field distribution in the cell becomes as shown in FIG. 9 and the orientation of liquid crystal directors 40 becomes as shown in FIG. 10 as a plane. The function and effect related to the orientation of the liquid crystal directors are the same as those in the second embodiment.

As seen in the description given above, the orientation vectors of the liquid crystal directors in each display picture element are symmetrically restricted by the orientation control electrode, and the boundaries between areas different in orientation vectors are fixed by the orientation control window. Therefore, viewing angle dependency is reduced and display at wide viewing angles is enabled. Also, occurrence of uniform disclination varying from one picture element to another can be prevented, removing a rough surface of the display screen and thus improving display quality.

Rubbing treatment of the orientation film is not required, reducing the manufacturing costs and eliminating static electricity occurring during rubbing for preventing the TFT from being electrostatically destroyed.

What is claimed is:

1. In a liquid crystal display comprising:

a first substrate;

a second substrate;

said first and second substrates being located facing each other with a liquid crystal layer therebetween;

a plurality of display electrodes disposed in a matrix;

switching elements connected to said display electrodes;

said display electrodes and said switching elements being formed on the liquid crystal layer side of said first substrate; and

a common electrode being formed on the liquid crystal layer side of said second substrate,

wherein a predetermined voltage is applied to said display electrodes to directly drive said liquid crystal layer for display,

the improvement comprising:

orientation control electrodes formed on said first substrate and electrically insulated from said display electrodes,

wherein a potential voltage independent from that of a display electrode potential is applied to said orientation control electrodes for controlling orientation of said liquid crystal layer.

2. The liquid crystal display as claimed in claim 1, wherein said switching elements are thin film transistors.

3. The liquid crystal display as claimed in claim 2, wherein each of said thin film transistors is a normal stagger type thin film transistor including a gate electrode formed via a semiconductor film and a gate insulation film above a source electrode and a drain electrode.

4. In a liquid crystal display comprising:

a first substrate;

a second substrate;

said first and second substrates being located facing each other with a liquid crystal layer therebetween;

a plurality of display electrodes disposed in a matrix;

switching elements connected to said display electrodes;

said display electrodes and said switching elements being formed on the liquid crystal layer side of said first substrate; and

a common electrode being formed on the liquid crystal layer side of said second substrate,

wherein a predetermined voltage is applied to said display electrodes to directly drive said liquid crystal layer for display,

the improvement comprising:

orientation control electrodes formed on said first substrate and electrically insulated from said display electrodes,

wherein a potential difference between said display electrode and said common electrode is applied to said orientation control electrode for controlling orientation of said liquid crystal layer, and wherein said orientation electrodes are formed in all areas except a formation area of said display electrodes or at least surrounding a periphery of said display electrodes.

5. The liquid crystal display as claimed in claim 4, wherein said orientation control electrodes are formed partially overlapping a peripheral edge of said display electrodes.

6. The liquid crystal display as claimed in claim 5, wherein said orientation control electrodes are electrically connected to said common electrode.

7. The liquid crystal display as claimed in claim 6, wherein said orientation control electrodes corresponding to picture elements on the same gate line are connected to each other.

8. The liquid crystal display as claimed in claim 7, wherein the overlapping portion of said orientation control electrode and said display electrode forms a substorage capacitance of each picture element, said substorage capacitance being electrically connected in parallel with a display capacitance of each picture element formed by said common electrode and said display electrode.

9. The liquid crystal display as claimed in claim 5, wherein the overlapping portion of said orientation control electrode and said display electrode forms a substorage capacitance for a picture element, said substorage capacitance being electrically connected in parallel with a display capacitance of each picture element formed by said common electrode and said display electrode.

10. The liquid crystal display as claimed in claim 4, wherein an orientation control window containing no electrode is formed in a picture element area of said common electrode.

11. The liquid crystal display as claimed in claim 10, wherein an effective potential difference between said orientation control electrode and said common electrode is smaller than that between said display electrode and said common electrode.

12. The liquid crystal display as claimed in claim 11, wherein said orientation control electrodes are electrically connected to said common electrode.

13. The liquid crystal display as claimed in claim 10, wherein said orientation control window is formed like an X character.

14. The liquid crystal display as claimed in claim 4, wherein an orientation control window containing no electrode is formed in a picture element area of each of said display electrodes.

15. The liquid crystal display as claimed in claim 14, wherein an effective potential difference between said orientation control electrode and said common electrode is larger than that between said display electrode and said common electrode.

16. The liquid crystal display as claimed in claim 14, wherein said orientation control window is formed like an X character.

17. In a liquid crystal display comprising:

a first substrate;

a second substrate;

said first and second substrates being located facing each other with a liquid crystal layer therebetween;

a plurality of display electrodes disposed in a matrix:

switching elements connected to said display electrodes;

said display electrodes and said switching elements being formed on the liquid crystal layer side of said first substrate; and

a common electrode being formed on the liquid crystal layer side of said second substrate,

wherein a predetermined voltage is applied to said display electrodes to directly drive said liquid crystal layer for display,

the improvement comprising:

orientation control electrodes formed on said first substrate and electrically insulated from said display electrodes,

wherein a potential difference between said display electrode and said common electrode is applied to said orientation control electrode for controlling orientation of said liquid crystal layer, wherein said switching elements are thin film transistors, wherein each of said thin film transistors is a normal stagger type thin film transistor including a gate electrode formed via a semiconductor film and a gate insulation film above a source electrode and a drain electrode and wherein an orientation control window containing no electrode is formed in a picture element area of said common electrode, and each of said orientation control electrodes is formed via the semiconductor film and the gate insulation film on said display electrode.

18. In a liquid crystal display comprising:

a first substrate:

a second substrate;

said first and second substrates being located facing each other with a liquid crystal layer therebetween;

a plurality of display electrodes disposed in a matrix;

switching elements connected to said display electrodes:

said display electrodes and said switching elements being formed on the liquid crystal layer side of said first substrate; and

a common electrode being formed on the liquid crystal layer side of said second substrate,

wherein a predetermined voltage is applied to said display electrodes to directly drive said liquid crystal layer for display,

the improvement comprising:

orientation control electrodes formed on said first substrate and electrically insulated from said display electrodes,

wherein a potential difference between said display electrode and said common electrode is applied to said orientation control electrode for controlling orientation of said liquid crystal layer, wherein said switching elements are thin film transistors, wherein each of said thin film transistors is a normal stagger type thin film transistor including a gate electrode formed via a semiconductor film and a gate insulation film above a source electrode and a drain electrode, and wherein an orientation control window containing no electrode is formed in a picture element area of each of said display electrodes, and each of said orientation control electrodes is formed via the semiconductor film and the gate insulation film on said display electrode.

19. A liquid crystal display comprising:

a first substrate;

a second substrate, said first and second substrates being located facing each other with a liquid crystal layer therebetween;

a plurality of display electrodes disposed in a matrix;

switching elements connected to said display electrodes, said display electrodes and said switching elements being formed on the liquid crystal layer side of said first substrate;

a common electrode formed on the liquid crystal layer side of said second substrate,

wherein a predetermined voltage is applied to said liquid crystal layer for display; and

orientation control electrodes formed on said first substrate and electrically insulated from said display electrodes, the orientation control electrodes surrounding an entire periphery of the display electrodes to maximize a display area of the liquid crystal layer,

wherein a potential independent from that of a display electrode potential is applied to said orientation control electrode for controlling orientation of the liquid crystal layer, and wherein the orientation of the crystal layer is controlled independently of a layer that has a rubbing direction for orientating the liquid crystal layer.

20. A liquid crystal display element comprising:

a first substrate;

a second substrate, the first and second substrates being located facing each other with a liquid crystal layer therebetween;

a display electrode;

a switching element connected to the display electrode, the display electrode and the switching elements being formed on the liquid crystal layer;

a common electrode also formed on the liquid crystal layer; and

an orientation control electrode formed on the first substrate and electrically insulated from the display electrode, the orientation control electrode surrounding an entire periphery of the display electrode to maximize a display area of the liquid crystal layer,

wherein a potential independent from a display electrode potential is applied to the orientation control electrode for controlling orientation of the liquid crystal layer, and

wherein the orientation of the crystal layer is controlled independent of a layer that has a rubbing direction for orientating the liquid crystal layer.

21. A liquid crystal display element comprising:

a first substrate;

a second substrate, the first and second substrates being located facing each other with a liquid crystal layer therebetween;

a display electrode;

a switching element connected to the display electrode, the display electrode and the switching elements being formed on the liquid crystal layer;

a common electrode also formed on the liquid crystal layer; and

an orientation control electrode formed on the first substrate and electrically insulated from the display electrode, the orientation control electrode surrounding an entire periphery of the display electrode to maximize a display area of the liquid crystal layer,

wherein a potential different from a display electrode potential is applied to the orientation control electrode for controlling orientation of the liquid crystal layer, and

wherein the orientation of the crystal layer is controlled independent of a layer that has a rubbing direction for orientating the liquid crystal layer, and wherein the orientation control electrode overlaps a portion of a peripheral edge of the display electrode.

22. A liquid crystal display element comprising:

a first substrate;

a second substrate, the first and second substrates being located facing each other with a liquid crystal layer therebetween;

a display electrode;

a switching element connected to the display electrode, the display electrode and the switching elements being formed on the liquid crystal layer;

a common electrode also formed on the liquid crystal layer; and

an orientation control electrode formed on the first substrate and electrically insulated from the display electrode, the orientation control electrode surrounding an entire periphery of the display electrode free of any overlap with the display electrode to maximize a display area of the liquid crystal layer,

wherein a potential different from a display electrode potential is applied to the orientation control electrode for controlling orientation of the liquid crystal layer.

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