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Paper 28
Entered: November 30, 2015

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD. (TSMC) and SAMSUNG ELECTRONICS CO., LTD,
Petitioner,

v.

DSS TECHNOLOGY MANAGEMENT, INC.,
Patent Owner.

Case IPR2014-01030[1]
Patent 5,652,084

Before ERICA A. FRANKLIN, JACQUELINE WRIGHT BONILLA, and KRISTINA M. KALAN, *Administrative Patent Judges*.

KALAN, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

[1] Case IPR2014-01493 has been joined with this proceeding.

I. INTRODUCTION

A. Background

Taiwan Semiconductor Manufacturing Company, Ltd. ("TSMC") filed a Petition to institute an *inter partes* review of claims 1–16 of U.S. Patent No. 5,652,084 (Ex. 1001, "the '084 patent"). Paper 1 ("Pet."). DSS Technology Management, Inc. ("Patent Owner") filed a Preliminary Response. Paper 6 ("Prelim. Resp."). On December 31, 2014, we instituted trial as to claims 1–12, 15, and 16 of the '084 patent. Paper 9 ("Dec.").

A different party, Samsung Electronics Co., Inc. ("Samsung"), filed a Petition for *inter partes* review of the '084 patent, which Petition was accorded a filing date of September 12, 2014. Case IPR2014-01493, Paper 1, Paper 4, *see also* Paper 7 (Corrected Petition for *Inter Partes* Review filed October 3, 2014). On January 29, 2015, Samsung also filed a Motion for Joinder to join the case with the previously instituted proceeding in *Taiwan Semiconductor Mfg. Co. v. DSS Tech. Mgmt., Inc.*, Case IPR2014-01030. Case IPR2014-01493, Paper 10. On February 24, 2015, we instituted trial in IPR2014-01493 and joined the case with Case IPR2014-01030. Case IPR2014-01493, Paper 12; Case IPR2014-01030, Paper 15.

During trial, Patent Owner filed a Patent Owner Response (Paper 18, "PO Resp."), which was accompanied by a Declaration from Dr. Chris A. Mack (Ex. 2007). TSMC and Samsung (collectively, "Petitioner") filed a Reply to the Patent Owner Response. Paper 22 ("Reply"). An oral hearing was held on August 12, 2015. A transcript of the consolidated hearing has been entered into the record. Paper 27 ("Tr.").

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73.

We determine that Petitioner has shown by a preponderance of the evidence that claims 1–12, 15, and 16 of the '084 patent are unpatentable.

B. Related Proceedings

The parties indicate that the '084 patent is involved in the following district court proceeding: *DSS Technology Mgmt., Inc. v. Taiwan Semiconductor Mfg. Co.*, 2-14-CV-00199 (E.D. Tex.) (the "related proceeding"). Pet. 1; Paper 4, Related Matters, 2.

C. The '084 Patent

The '084 patent, titled "Method for Reduced Pitch Lithography," issued on July 29, 1997. The '084 patent relates to a lithographic patterning process using multiple exposures to provide for relatively reduced pitch for features of a single patterned layer. Ex. 1001, Abstract.

Figure 1, reproduced below, illustrates an exemplary process:

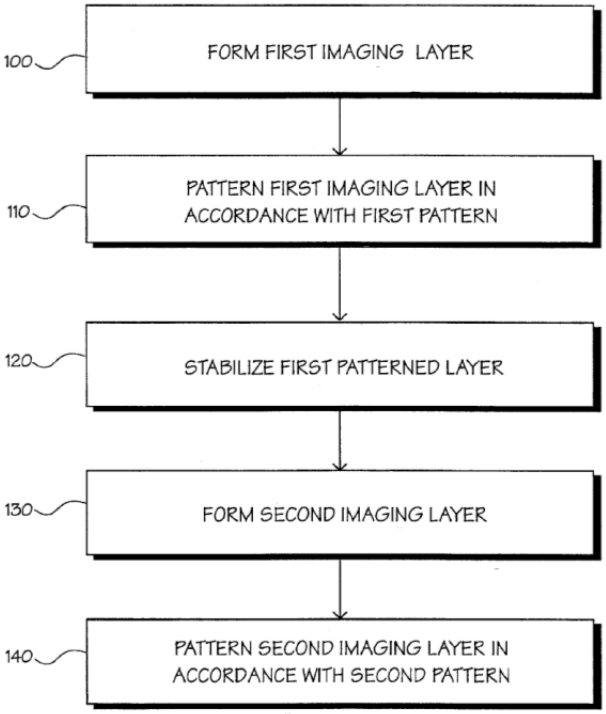
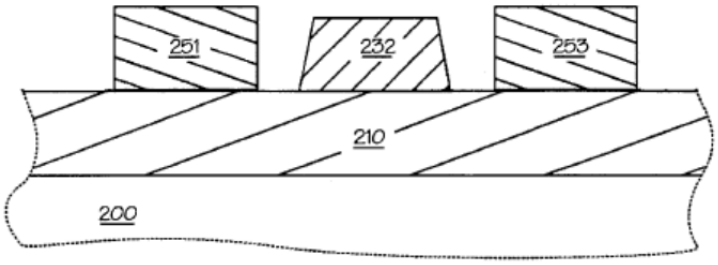


Figure 1 illustrates, in flow diagram form, one lithography method for semiconductor fabrication. *Id.* at 2:7–8.

Figure 5, reproduced below, illustrates a product of the method illustrated in Figure 1:



Specifically, Figure 5 shows a cross-sectional view of a semiconductor wafer as a result of the method of Figure 1. *Id.* at 2:20–22, 7:36–37. After completion of steps 110 and 120 of Figure 1, first patterned layer 232 is formed. *Id.* at 4:31–34. Following completion of steps 130 and 140 of Figure 1, second patterned layers 251 and 253 are formed. *Id.* at 6:51–53. As a result of the method of Figure 1, a single patterned layer is formed over layer 210 as illustrated in Figure 5. *Id.* at 7:36–37.

D. Illustrative Claims

Of the instituted claims, claims 1 and 15 are independent. As to the remaining instituted claims, claims 2–12 directly depend from claim 1, and claim 16 depends from claim 15.

Claim 1 of the ’084 patent is illustrative of the claims at issue:

> 1. A lithography method for semiconductor fabrication using a semiconductor wafer, comprising the steps of:
>
> (a) forming a first imaging layer over the semiconductor wafer;
>
> (b) patterning the first imaging layer in accordance with a first pattern to form a first patterned layer having a first feature;
>
> (c) stabilizing the first patterned layer;

(d) forming a second imaging layer over the first pattern layer; and

(e) patterning the second imaging layer in accordance with a second pattern to form a second patterned layer having a second feature distinct from the first feature, wherein the second patterned layer and the first patterned layer form a single patterned layer, and wherein the first and second features which are formed relatively closer to one another than is possible through a single exposure to radiation.

Ex. 1001, 13:6–24.

E. Prior Art Supporting Instituted Unpatentability Grounds

1. Japanese Patent App. No. H04-71222, published March 5, 1992 ("Jinbo") (Ex. 1011) (Ex. 1004).[2]

2. US Patent No. 4,931,351, issued June 5, 1990 ("McColgin") (Ex. 1006).

3. US Patent No. 4,548,688, issued October 22, 1985 ("Matthews") (Ex. 1007).

F. Instituted Unpatentability Grounds

We instituted an *inter partes* review of claims 1–12, 15, and 16 of the '084 patent on the following grounds. Dec. 19.

References	Basis	Claims Challenged
Jinbo	§ 102(b)	1–8, 12, 15, and 16
Jinbo and McColgin	§ 103(a)	9
Jinbo and Matthews	§ 103(a)	10 and 11

[2] Petitioner relies on a certified English translation of Jinbo submitted as Exhibit 1004 (in original and corrected versions). All references to Jinbo in this Decision refer to the corrected version of Exhibit 1004.

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