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United States Patent [19]

Hsue et al.

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[54] **PROCESS FOR CREATING HIGH DENSITY INTEGRATED CIRCUITS UTILIZING DOUBLE COATING PHOTORESIST MASK**

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[73] Assignee: **United Microelectronics Corporation**, Hsin-Chu, Taiwan

[21] Appl. No.: **746,147**

[22] Filed: **Nov. 6, 1996**

Related U.S. Application Data

[63] Continuation of Ser. No. 241,336, May 11, 1994, abandoned.

[51] **Int. Cl.**[6] **G03F 7/26**

[52] **U.S. Cl.** **430/312**; 430/313; 430/314; 430/328; 430/330; 430/394

[58] **Field of Search** 430/312, 313, 430/314, 328, 330, 394

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,591,547	5/1986	Brownell	430/312
4,704,347	11/1987	Vollenbroek et al.	430/312
4,906,552	3/1990	Ngo et al.	430/312
5,091,290	2/1992	Rolfson	430/327

Primary Examiner—Christopher G. Young
Attorney, Agent, or Firm—William H. Wright; Alan S. Raynes

[57] **ABSTRACT**

A new photolithographic process using the method of photoresist double coating to fabricate fine lines with narrow spacing is described. A layer to be etched is provided overlying a semiconductor substrate. The layer to be etched is coated with a first layer of photoresist and baked. The first photoresist layer is exposed to actinic light through openings in a mask and developed to produce the desired first pattern on the surface of the first photoresist wherein the openings have a minimum width of the resolution limit plus two times the misalignment tolerance of the photolithography process. The layer to be etched is coated with a second photoresist layer where the layer to be etched is exposed within the openings in the first photoresist layer. The second photoresist layer is exposed to actinic light through openings in a mask and developed to produce the desired second pattern on the surface of the second photoresist wherein the second pattern alternates with the first photoresist pattern and wherein the spacing between the first and second patterned photoresist coatings has a width equal to the misalignment tolerance. The misalignment tolerance is much smaller than the resolution limit so the line spacing achieved is narrower than the resolution limit of the photolithography process.

20 Claims, 3 Drawing Sheets

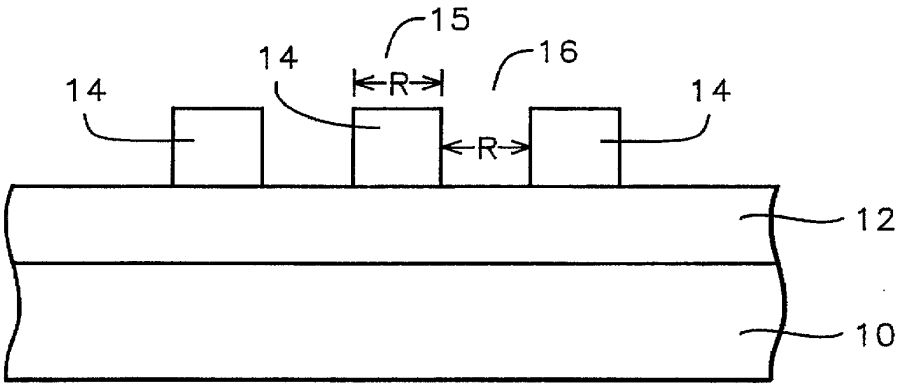

FIG. 1 Prior Art

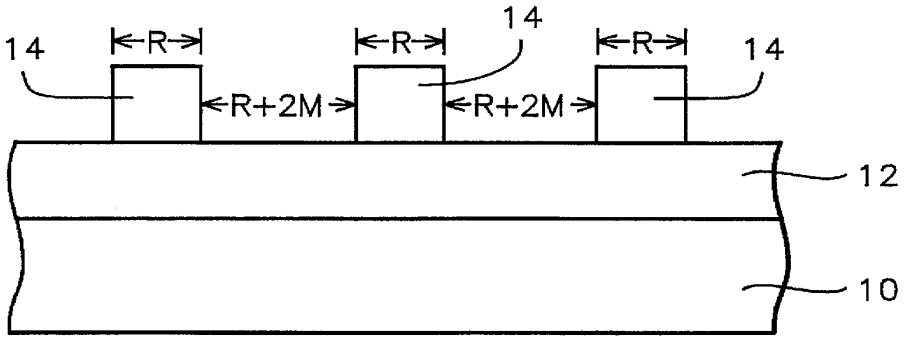

FIG. 2

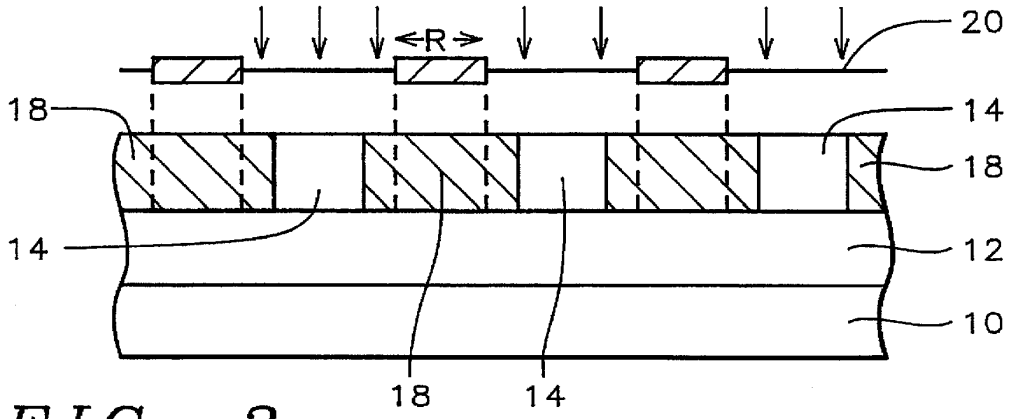

FIG. 3

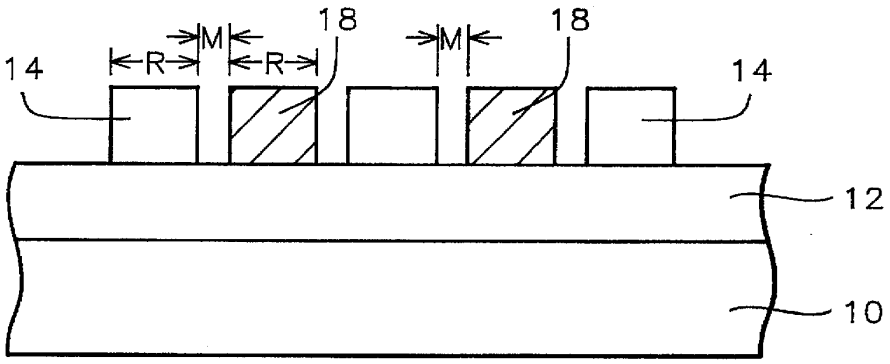

FIG. 4

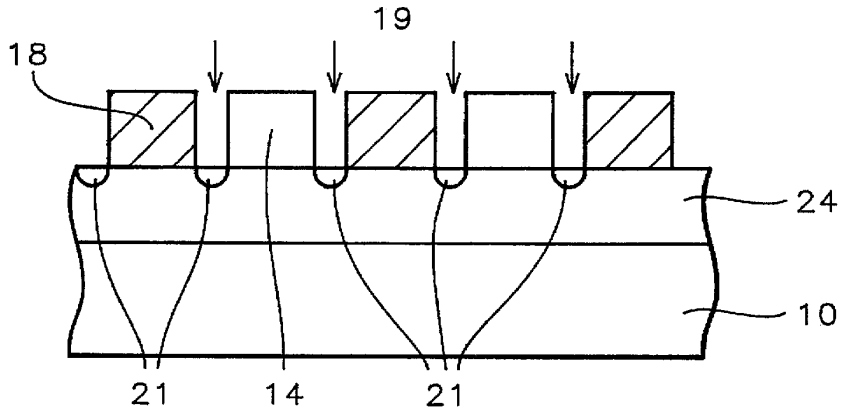

FIG. 5

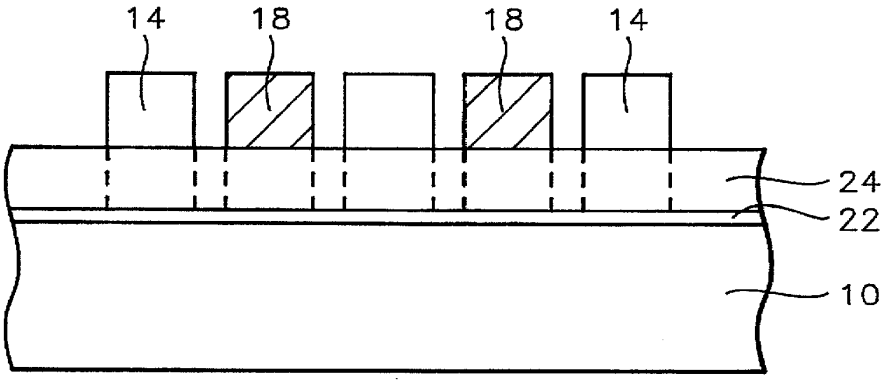

FIG. 6

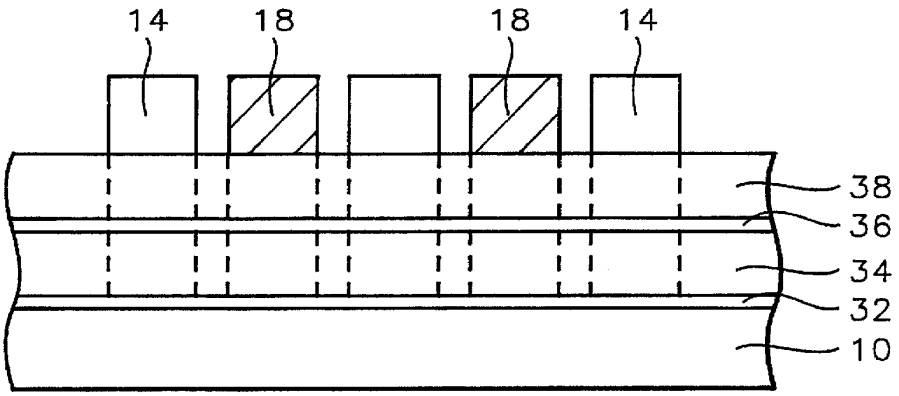

FIG. 7

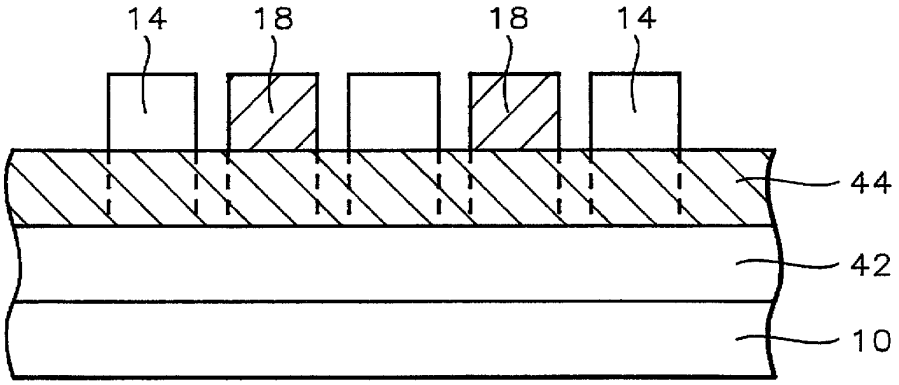

FIG. 8

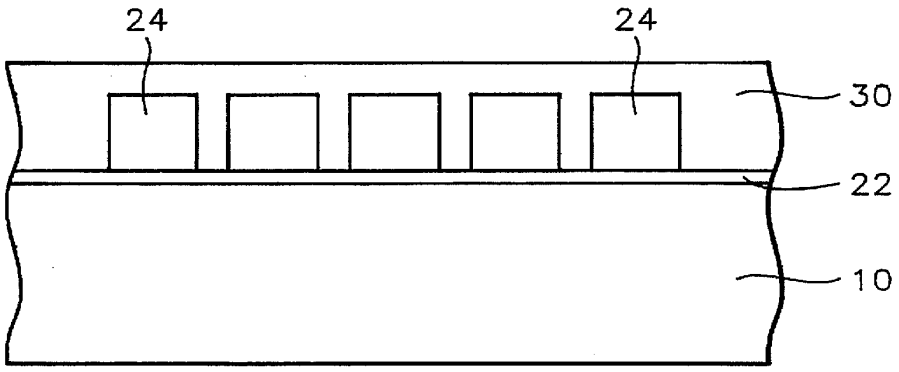

FIG. 9

PROCESS FOR CREATING HIGH DENSITY INTEGRATED CIRCUITS UTILIZING DOUBLE COATING PHOTORESIST MASK

This is a continuation of application Ser. No. 08/241,336 filed on May 11, 1994, now abandoned.

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The invention relates to the fabrication of integrated circuit devices, and more particularly, to a method of photoresist double coating to fabricate fine lines with narrower spacing than the resolution limit offered by the current best photolithography in the fabrication of integrated circuits.

(2) Description of the Prior Art

In the fabrication of integrated circuits, reductions in both the minimum line width and line spacing can lead to a denser circuit layout or smaller die size for the product. However, the minimum line width and line spacing on the wafer are limited conventionally by photolithography's resolution.

Referring to FIG. **1**, there is shown a portion of a partially completed integrated circuit. A layer **12** which is to be etched is deposited over silicon substrate **10**. Photoresist layer **14** coats the surface of the layer **12**. As shown in FIG. **1**, the photoresist layer **14** is patterned to create a photoresist mask. If the resolution of the photolithography process is R and the minimum misalignment tolerance between two layers is M, then the minimum pitch (line width (15)+line spacing (16)) is R+R=2R, by the conventional photolithographic process of the prior art.

U.S. Pat. No. 4,906,552 to Ngo et al describes a flood illumination patterning technique that achieves resolutions of 0.5 micrometers or less using a dual layer of photoresist. U.S. Pat. Nos. 5,091,290 to Rolfson, 4,704,347 to Vollenbroek et al, and 4,591,547 to Brownell all teach methods of dual layers of photoresist in which one layer of photoresist is at least partially over the other layer of photoresist.

SUMMARY OF THE INVENTION

A principal object of the present invention is to provide an effective and very manufacturable method of providing narrow line spacing of less than the resolution limit of the photolithography process.

In accordance with the object of this invention a new photolithographic process using the method of photoresist double coating to fabricate fine lines with narrow spacing is achieved. A layer to be etched is provided overlying a semiconductor substrate. The layer to be etched is coated with a first layer of photoresist and baked. The first photoresist layer is exposed to actinic light through openings in a mask and developed to produce the desired first pattern on the surface of the first photoresist wherein the openings have a minimum width of the resolution limit plus two times the misalignment tolerance of the photolithography process. The layer to be etched is coated with a second photoresist layer where the layer to be etched is exposed within the openings in the first photoresist layer. The second photoresist layer is exposed to actinic light through openings in a mask and developed to produce the desired second pattern on the surface of the second photoresist wherein the second pattern alternates with the first photoresist pattern and wherein the spacing between the first and second patterned photoresist coatings has a width equal to the misalignment tolerance. The misalignment tolerance is much smaller than the resolution limit so the line spacing achieved is narrower than the resolution limit of the photolithography process.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings forming a material part of this description, there is shown:

FIG. **1** schematically illustrates in cross-sectional representation a photolithographic process of the prior art.

FIGS. **2** through **4** schematically illustrate in cross-sectional representation a preferred embodiment of the present invention.

FIGS. **5** through **8** schematically illustrate in cross-sectional representation additional embodiments of the present invention.

FIG. **9** schematically illustrates in cross-sectional representation a completed integrated circuit for one embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now more particularly to FIGS. **2** through **4**, the photolithographic method of the present invention will be described. A layer **12** to be etched has been deposited over the surface of semiconductor substrate **10**. This layer can be a single layer or multi-layers and can be a polysilicon word line or metal line or various other structures in the fabrication of an integrated circuit. Specific examples will be discussed in the Examples section to follow. The process of the invention is independent of the material to be etched.

A first layer of photoresist **14** is coated over the surface of the layer **12**. A positive photoresist is used with a conventional thickness of between about 10,000 to 30,000 Angstroms. The photoresist layer **14** is exposed to actinic light through openings in a mask and developed to produce the desired pattern on the surface of the photoresist. The resulting resist mask layer **14** has openings of the size R+2M, where R is the line width and M is the misalignment tolerance.

The photoresist mask layer **14** is baked using an ultraviolet baking process at a temperature of between about 140° to 160° C. for between about 50 to 70 seconds. The ultraviolet baking process hardens the photoresist mask layer.

A second photoresist coating **18** is spun onto the wafer into the openings in the photoresist mask layer **14**. The photoresist layer **18** is exposed to actinic light through openings in a mask **20**, shown in FIG. **3**, and developed to produce the desired pattern on the surface of the photoresist. Since the first photoresist mask **14** has been hardened by the ultraviolet baking process, it will not be removed during developing and etching of the second photoresist layer **18**. The resulting resist mask layer is illustrated in FIG. **4**. The spacing between the lines will be M instead of R as in the prior art. Since M is much smaller than R, the line spacing has been reduced dramatically by using the double photoresist coating method of the invention. For example, for the 0.6 micrometer design rule, R=0.6 micrometers and M is approximately=0.2 micrometers. After the layer **12** has been etched, the photoresist mask layer **14**,**18** can be stripped using a wet or dry photoresist stripping process, such as sulfuric acid or other stripper chemicals for a wet strip, or oxygen plasma for a dry strip.

EXAMPLES

The following Examples are given to show the important features of the invention and to aid in the understanding thereof and variations may be made by one skilled in the art without departing from the spirit and scope of the invention.

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