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United States Patent [19]

Cleeves

[54] DISPOSABLE POST PROCESSING FOR SEMICONDUCTOR DEVICE FABRICATION

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- [73] Assignee: Cypress Semiconductor Corp., San Jose, Calif.
- [21] Appl. No.: 515,675
- [22] Filed: Aug. 17, 1995

Related U.S. Application Data

- [62] Division of Ser. No. 179,615, Jan. 10, 1994, abandoned.
- [51] Int. Cl.⁶ H01L 21/283
- [52] U.S. Cl. 437/195; 437/228; 430/313

[56] References Cited

U.S. PATENT DOCUMENTS

4,997,790	3/1991	Woo et al 437/195
5,063,169	11/1991	De Bruin et al 437/192
5,068,207	11/1991	Manocha et al 437/235
5,158,910	10/1992	
5,187,121	2/1993	Cote et al 437/195
5,219,787	6/1993	Carey et al 437/187
5,270,236	12/1993	Rosner 437/48
5,275,973	1/1994	Gelatos 437/195
5,283,208	2/1994	Lorsung et al 437/195
5,319,247	6/1994	Matsuura 257/760
5,352,630	10/1994	Kim et al 437/195
5,382,545	1/1995	Hong 437/195
5,461,004	10/1995	Kim 437/195

OTHER PUBLICATIONS

S. Wolf, "Silicon Processing for the VLSI Era" vol. II, pp. 161,238,429,432, Jun. 1990.

Fukase, et al, "A Margin-Free Contact Process Using An Al₂O₃ Etch-Stop Layer For Higher Density Devices," *IEDM*, Apr. 1992, pp. 837-840.

Ueno, et al, "A Quarter-Micron Planarized Interconnection Technology With Self-Aligned Plug," *IEDM*, Apr. 1992, pp. 305–308.

5,710,061

Jan. 20, 1998

Kusters, et al, "A High Density 4Mbit dRAM Process Using a Fully Overlapping Bitline Contact (FoBIC) Trench Cell," 1987 Symposium on VLSI Technology Digest of Technical Papers, May 18–21, 1987/Karuizawa, pp. 93–94.

Kakumu, et al, "PASPAC (Planarized A1/Silicide/Poly Si With Self Aligned Contact) With Low Contact Resistance and High Reliability in CMOS LSIs," 1987 Symposium on VLSI Technology Digest of Technical Papers, May 18–21, 1987/Karuizawa, pp. 77–78.

Kenny, et al, "A Buried-Plate Trench Cell for a 64-Mb DRAM," 1992 Symposium on VLSI Technology Digest of Technical Papers, Apr. 1992, pp. 14-15.

Subbanna, et al, "A Novel Borderless Contact/Interconnect Technology Using Aluminum Oxide Etch Stop for High Performance SRAM and Logic," Dec. 1993, pp. 441–444. Kusters, et al, "A Stacked Capacitor Cell with A Fully Self–Aligned Contact Process for High–Density Dynamic Random Access Memories," *Journal of the Electrochemical Society*, vol. 139, No. 8, Aug. 1992, pp. 2318–2321.

"Method for Forming Via Hole Formation," *IBM Technical Disclosure Bulletin*, vol. 34, No. 10A, Mar. 1992, pp. 219–220.

(List continued on next page.)

Primary Examiner-Charles L. Bowers, Jr.

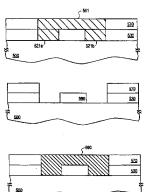
Assistant Examiner-Leon Radomsky

Attorney, Agent, or Firm-Blakely, Sokoloff, Taylor & Zafman LLP

ABSTRACT

A disposable post process allows openings to be created in a layer formed over a semiconductor wafer, for example to create self-aligned contacts. A layer of material is formed over a semiconductor wafer and subsequently patterned into posts which define the location and shape of openings to be formed in a subsequently formed planar layer. After the planar layer is formed to surround the posts, the posts are removed to create openings in the planar layer. These openings may then be used to form suitable contacts.

20 Claims, 8 Drawing Sheets



[57]

OTHER PUBLICATIONS

"Self-Aligned, Borderless Polysilicon Contacts Using Poly-silicon Pillars," *IBM Technical Disclosure Bulletin*, vol. 35, No. 2, Jul. 1992, pp. 480–483. Wolf, et al, "Silicon Processing for the VLSI Era, vol. I:

Process Technology," Lithography I: Optical Resist Materials and process Technology, 1986, pp. 453-454.

S. Wolf, "Silicon Processing for the VLSI Era, vol. 2: Process Integration," *Multilevel-Interconnect Tehnology for VLSI & ULSI*, 1992, pp. 222–237.

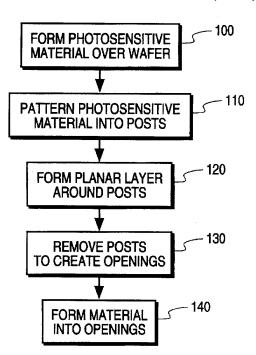


FIG. 1

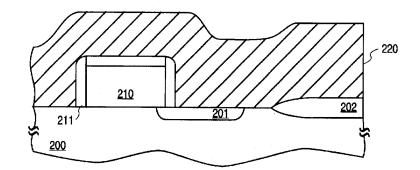
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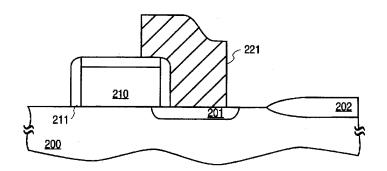


FIG. 2B

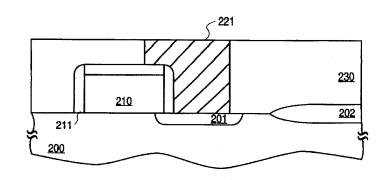


FIG. 2C

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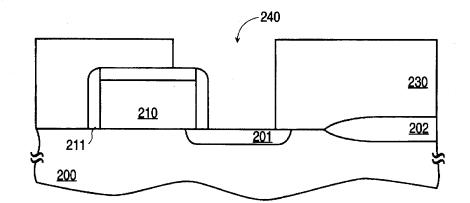


FIG. 2D

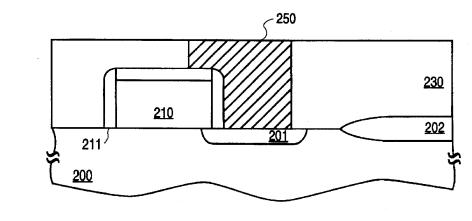


FIG. 2E

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