



US005652084A

United States Patent [19]
Cleeves

[11] Patent Number: 5,652,084
[45] Date of Patent: Jul. 29, 1997

- [54] **METHOD FOR REDUCED PITCH LITHOGRAPHY**
- [75] Inventor: **James M. Cleeves**, Redwood City, Calif.
- [73] Assignee: **Cypress Semiconductor Corporation**, Calif.
- [21] Appl. No.: **740,145**
- [22] Filed: **Oct. 22, 1996**

Related U.S. Application Data

- [63] Continuation of Ser. No. 361,595, Dec. 22, 1994, abandoned.
- [51] Int. Cl.⁶ **G03F 7/20**
- [52] U.S. Cl. **430/315; 430/313; 430/328; 430/330**
- [58] Field of Search **430/311, 313, 430/315, 324, 328, 330**

References Cited

U.S. PATENT DOCUMENTS

4,548,688	10/1985	Matthews	430/325
4,775,609	10/1988	McFarland	430/325
4,814,243	3/1989	Ziger	430/30
4,826,756	5/1989	Orvek	430/328
4,859,573	8/1989	Maheras et al.	430/326
4,904,866	2/1990	Collins	250/492.2
4,908,656	3/1990	Suwa et al.	355/53
4,931,351	6/1990	McColgin	430/323
4,985,374	1/1991	Tsuji et al.	430/229
5,158,910	10/1992	Cooper et al.	437/195
5,219,787	6/1993	Carey et al.	437/187
5,270,236	12/1993	Rosner	437/48
5,300,403	4/1994	Angelopolus	430/325
5,319,247	6/1994	Matsuura	257/760
5,320,932	6/1994	Haraguchi et al.	430/312
5,352,630	10/1994	Kim et al.	437/195

OTHER PUBLICATIONS

Fukase, et al, "A Margin-Free Contact Process Using An Al₂O₃ Etch-Stop Layer For High Density Devices", IEDM, Apr. 1992, pp. 837-840.

Ueno, et al., "A High Quarter-Micron Planarized Interconnection Technology with Self-Aligned Plug", IEDM, Apr. 1992, pp. 305-308.

Kusters, et al., "A High Density 4Mbit dRAM Process Using A Fully Overlapping Bitline Contact (FoBIC) Trench Cell", 1987 Symposium on VLSI Technology Digest of Technical Papers, May 18-21, 1987/Karuizawa, pp. 93-94.

Kakumu, et al., "PASPAC (Planarized Al/Silicide/Poly Si with Self Aligned Contact) with Low Contact Resistance and High Reliability in CMOS LSIs", 1987 Symposium on VLSI Technology Digest of Technical Papers, May 18-21, 1987/Karuizawa, pp. 77-78.

Kenny, et al., "A Buried-Plate Trench Cell for a 64-Mb DRAM", 1992 Symposium on VLSI Technology Digest of Technical Papers, Apr. 1992, pp. 14-15.

Subbanna, et al., "A Novel Borderless Contact/Interconnect Technology Using Aluminum Oxide Etch Stop for High Performance SRAM and Logic", Dec. 1993, pp. 441-444.

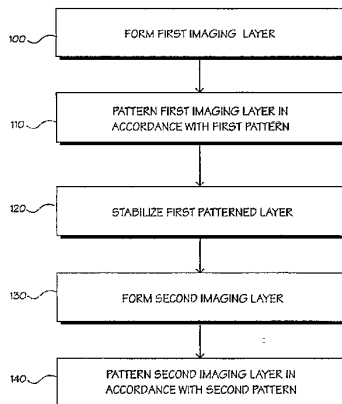
(List continued on next page.)

Primary Examiner—Kathleen Duda
Attorney, Agent, or Firm—Blakely, Sokoloff, Taylor & Zafman, LLP

[57] **ABSTRACT**

A lithographic patterning process uses multiple exposures to provide for relatively reduced pitch for features of a single patterned layer. A first imaging layer is exposed to radiation in accordance with a first pattern and developed. The resulting patterned layer is stabilized. A second imaging layer is subsequently formed to surround the first patterned layer, exposed to radiation in accordance with a second pattern, and developed to form a second patterned layer. As the first patterned layer has been stabilized, the first patterned layer remains with the second patterned layer to produce a single patterned layer. For another embodiment, a single imaging layer is patterned by exposure to radiation in accordance with two separate patterns. An exposed portion of the imaging layer is suitably stabilized to withstand subsequent lithographic process steps.

16 Claims, 10 Drawing Sheets



OTHER PUBLICATIONS

Kusters, et al., "A Stacked Capacitor Cell with a Fully Self-Aligned Contact Process for High-Density Dynamic Random Access Memories", *Journal of the Electrochemical Society*, vol. 139, No. 8, Aug. 1992, pp. 2318-2321.

"Method for Forming Via Hole Formation", *IBM Technical Disclosure Bulletin*, vol. 34, No. 10A, Mar. 1992, pp. 219-220.

"Self-Aligned, Borderless Polysilicon Contacts Using Polysilicon Pillars", *IBM Technical Disclosure Bulletin*, vol. 35, No. 2, Jul. 1992, pp. 480-483.

S. Wolf, Ph.D., et al., "Silicon Processing for the VLSI Era, vol. I: Process Technology", *Lithography I: Optical Resist Materials and Process Technology*, 1986, pp. 453-454.

S. Wolf, Ph.D., "Silicon Processing for the VLSI Era, vol. 2: Process Integration", *Multilevel-Interconnect Technology for VLSI & ULSI*, 1992, pp. 222-237.

"Method to Incorporate Three Sets of Pattern Information in Two Photomasking Steps", *IBM Technical Disclosure Bulletin*, vol. 32, No. 8A, pp. 218-219 (Jan. 1990).

"Dual-Image Resist for Single-Exposure Self-Aligned Processing," *IBM Technical Disclosure Bulletin*, vol. 33, No. 2, pp. 447-449 (Jul. 1990).

"Complementary Selective Writing by Direct-Write E-Beam/Optical Lithography Using Mixed Positive and Negative Resist," *IBM Technical Disclosure Bulletin*, vol. 33, No. 3A, pp. 62-63 (Aug. 1990).

"Sub-Micron Channel Length CMOS Technology," *IBM Technical Disclosure Bulletin*, vol. 33, No. 4, pp. 227-232 (Sep. 1990).

"Multilayer Circuit Fabrication Using Double Exposure of Positive Resist," *IBM Technical Disclosure Bulletin*, vol. 36, No. 10, pp. 423-424 (Oct. 1993).

Wolf, S., et al., *Silicon Processing for the VLSI Era, vol. 1: Process Technology*, Lattice Press, Sunset Beach, California, pp. 407-458 (1986).

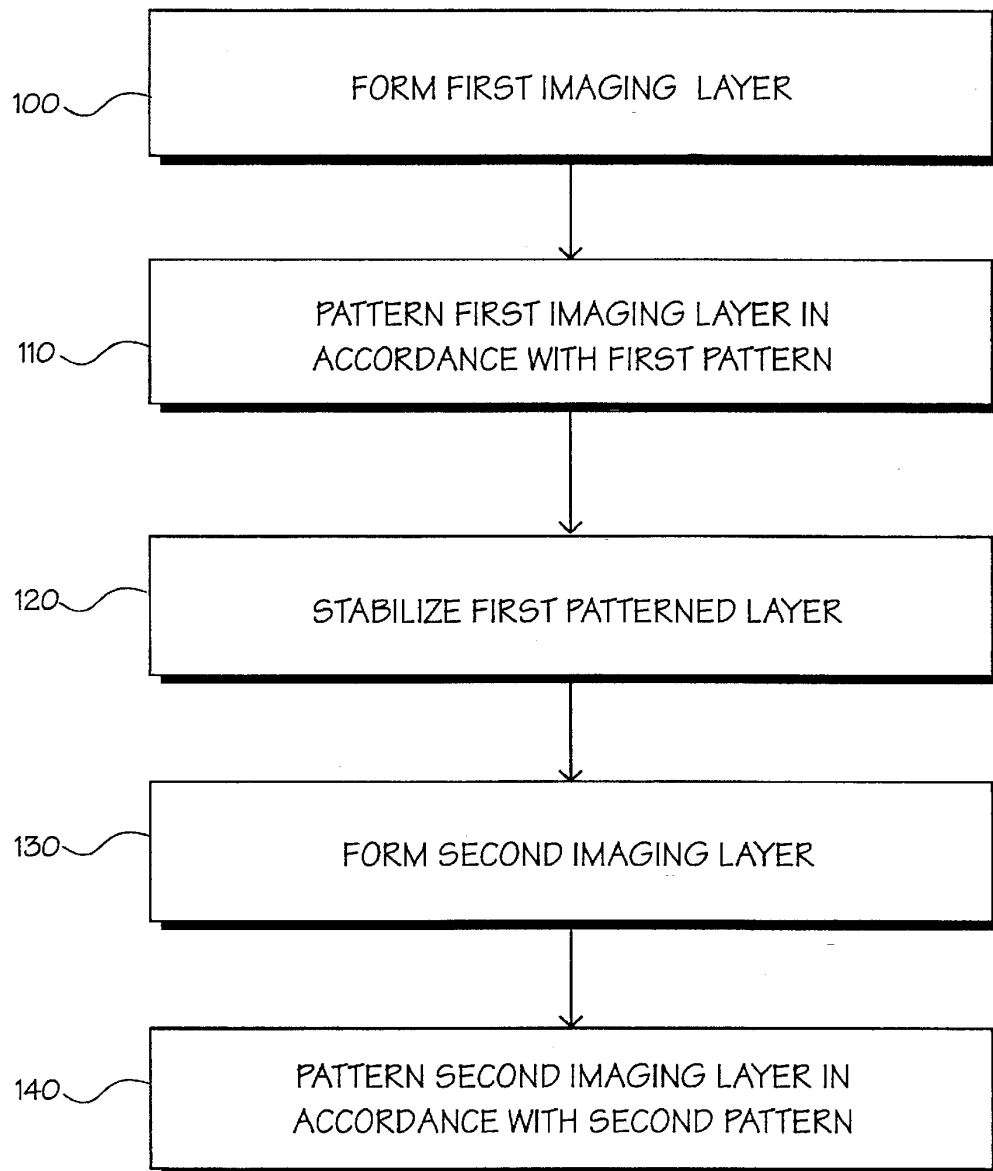


Fig.1

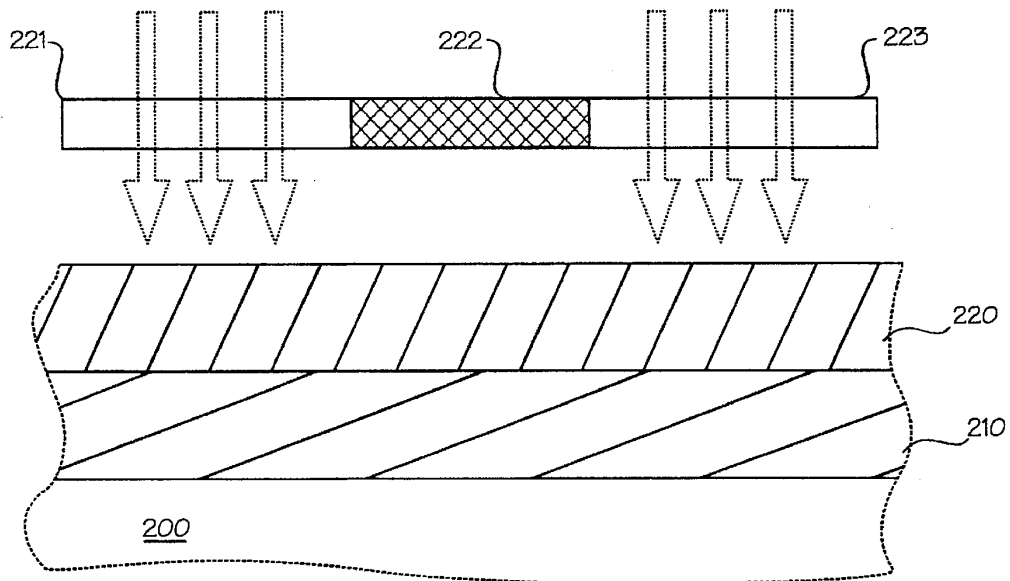


Fig.2

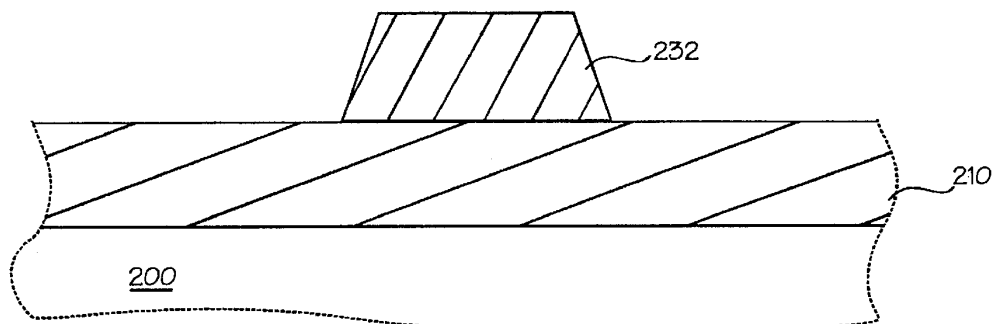


Fig.3

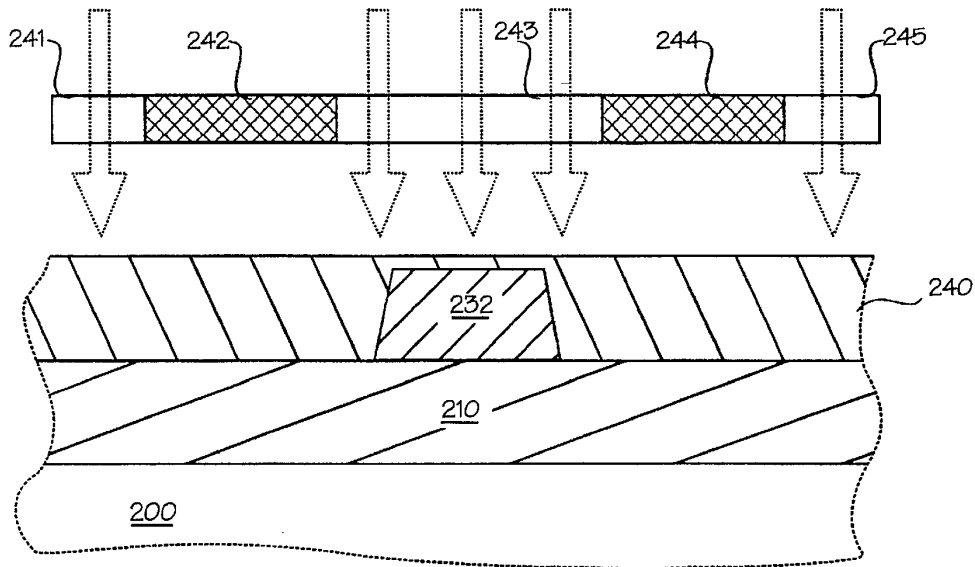


Fig.4

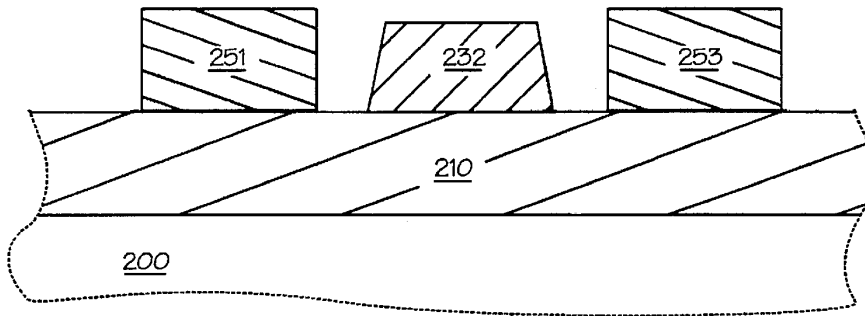


Fig.5

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts



Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research



With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips



Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS

Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS

Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS

Sync your system to PACER to automate legal marketing.