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(72) Inventeurs/Inventors:
ROW, EDWARD JOHN, US;
BOUCHER, LAURENCE B., US;
PITTS, WILLIAM M., US;
BLIGHTMAN, STEPHEN E., US

(73) Propriétaire/Owner:
AUSPEX SYSTEMS, INC., US

(74) Agent: GOWLING LAFLEUR HENDERSON LLP

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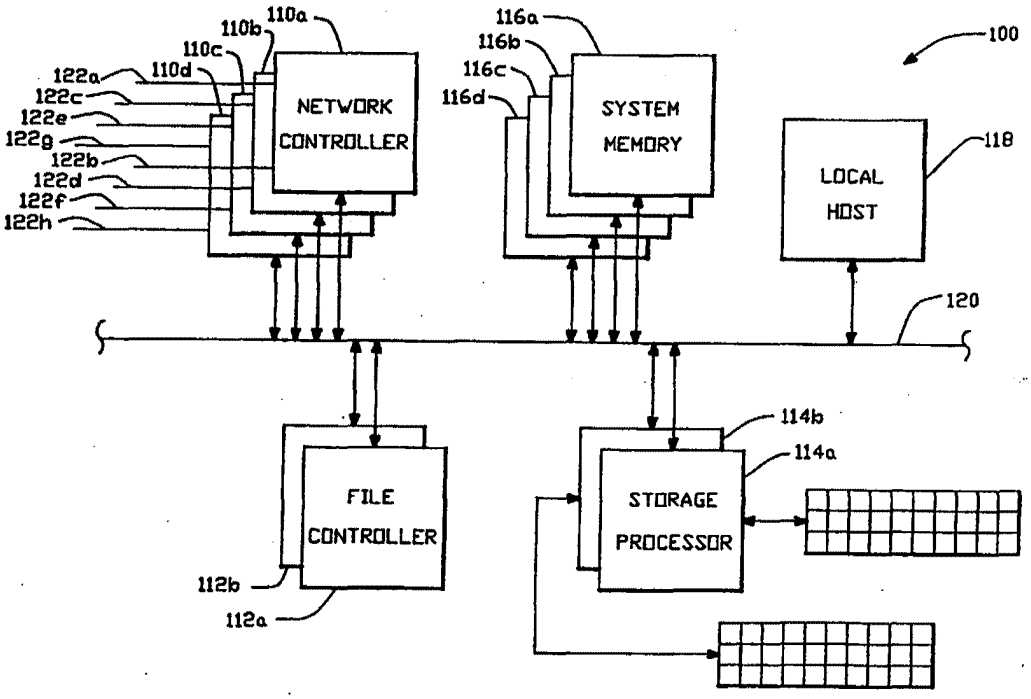

(57) Abrégé/Abstract:
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(71) Applicant: AUSPEX SYSTEMS, INC. [US/US]; 2952 Bunker Hill Lane, Santa Clara, CA 95054 (US).

(72) Inventors: ROW, Edward, John ; 468 Mountain Laurel Court, Moutain View, CA 94064 (US). BOUCHER, Laurence, B. ; 20605 Montalvo Heights Drive, Saratoga, CA 95070 (US). PITTS, William, M. ; 780 Mora Drive, Los Altos, CA 94022 (US). BLIGHTMAN, Stephen, E. ; 775 Salt Lake Drive, San Jose, CA 95133 (US).

(74) Agents: FLIESLER, Martin, C. et al.; Fliesler, Dubb, Meyer & Lovejoy, 4 Embarcadero Center, Suite 400, San Francisco, CA 94111 (US).

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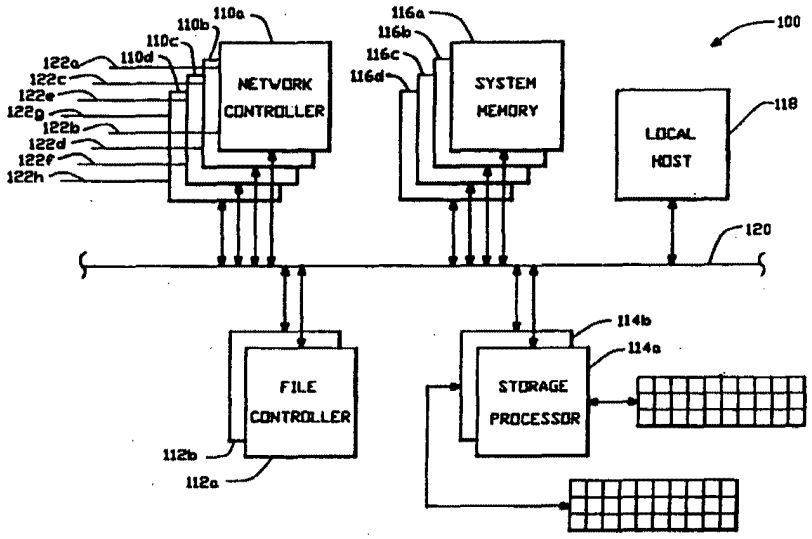

(57) Abstract

A file server architecture is disclosed, comprising as separate processors, a network controller unit (110), a file controller unit (112) and a storage processor unit (114). These units incorporate their own processors, and operate in parallel with a local Unix host processor (118). All networks are connected to the network controller unit (110), which performs all protocol processing up through the NFS layer. The virtual file system is implemented in the file controller unit (112) and the storage processor (114) provides high-speed multiplexed access to an array of mass storage devices. The file controller unit (112) controls file information caching through its own local cache buffer, and controls disk data caching through a large system memory which is accessible on a bus by any of the processors.

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PARALLEL I/O NETWORK FILE SERVER ARCHITECTURE

The present application is related to the following U.S. Patent Applications, all filed concurrently herewith:

1. MULTIPLE FACILITY OPERATING SYSTEM ARCHITECTURE, invented by David Hitz, Allan Schwartz, James Lau and Guy Harris;

2. ENHANCED VMEBUS PROTOCOL UTILIZING PSEUDOSYNCHRONOUS HANDSHAKING AND BLOCK MODE DATA TRANSFER, invented by Daryl Starr; and

3. BUS LOCKING FIFO MULTI-PROCESSOR COMMUNICATIONS SYSTEM UTILIZING PSEUDOSYNCHRONOUS HANDSHAKING AND BLOCK MODE DATA TRANSFER invented by Daryl D. Starr, William Pitts and Stephen Blightman.

The above applications are all assigned to the assignee of the present invention and are all expressly incorporated herein by reference.

BACKGROUND OF THE INVENTION

Field of the Invention

The invention relates to computer data networks, and more particularly, to network file server architectures for computer networks.

Description of the Related Art

Over the past ten years, remarkable increases in hardware price/performance ratios have caused a startling shift in both technical and office computing environments. Distributed workstation-server networks are displacing the once pervasive dumb terminal attached to mainframe or minicomputer. To date, however, network I/O limitations have constrained the potential performance available to workstation users. This situation has developed in part because dramatic jumps in microprocessor performance have exceeded increases in network I/O performance.

In a computer network, individual user workstations are referred to as clients, and shared resources for filing, printing, data storage and wide-area communications are referred to as servers. Clients and servers are all considered nodes of a network. Client nodes use standard communications protocols to exchange service requests and responses with server nodes.

Present-day network clients and servers usually run the DOS, MacIntosh OS, OS/2, or Unix operating systems. Local networks are usually Ethernet or Token Ring at the high end, Arcnet in the midrange, or LocalTalk or StarLAN at the low end. The client-server communication protocols are fairly strictly dictated by the operating system environment -- usually one of several proprietary schemes for PCs (NetWare, 3Plus, Vines, LANManager, LANServer); AppleTalk for MacIntoshes; and TCP/IP with NFS or RFS

for Unix. These protocols are all well-known in the industry.

Unix client nodes typically feature a 16- or 32-bit microprocessor with 1-8 MB of primary memory, a 640 x 1024 pixel display, and a built-in network interface. A 40-100 MB local disk is often optional. Low-end examples are 80286-based PCs or 68000-based MacIntosh I's; mid-range machines include 80386 PCs, MacIntosh II's, and 680X0-based Unix workstations; high-end machines include RISC-based DEC, HP, and Sun Unix workstations. Servers are typically nothing more than repackaged client nodes, configured in 19-inch racks rather than desk sideboxes. The extra space of a 19-inch rack is used for additional backplane slots, disk or tape drives, and power supplies.

Driven by RISC and CISC microprocessor developments, client workstation performance has increased by more than a factor of ten in the last few years. Concurrently, these extremely fast clients have also gained an appetite for data that remote servers are unable to satisfy. Because the I/O shortfall is most dramatic in the Unix environment, the description of the preferred embodiment of the present invention will focus on Unix file servers. The architectural principles that solve the Unix server I/O problem, however, extend easily to server performance bottlenecks in other operating system environments as well. Similarly, the description of the preferred embodiment will focus on Ethernet implementations, though the principles extend easily to other types of networks.

In most Unix environments, clients and servers exchange file data using the Network File System ("NFS"), a standard promulgated by Sun Microsystems and now widely adopted by the Unix community. NFS is defined in a document entitled, "NFS: Network File

System Protocol Specification," Request For Comments (RFC) 1094, by Sun Microsystems, Inc. (March 1989). This document is incorporated herein by reference in its entirety.

While simple and reliable, NFS is not optimal. Clients using NFS place considerable demands upon both networks and NFS servers supplying clients with NFS data. This demand is particularly acute for so-called diskless clients that have no local disks and therefore depend on a file server for application binaries and virtual memory paging as well as data. For these Unix client-server configurations, the ten-to-one increase in client power has not been matched by a ten-to-one increase in Ethernet capacity, in disk speed, or server disk-to-network I/O throughput.

The result is that the number of diskless clients that a single modern high-end server can adequately support has dropped to between 5-10, depending on client power and application workload. For clients containing small local disks for applications and paging, referred to as dataless clients, the client-to-server ratio is about twice this, or between 10-20.

Such low client/server ratios cause piecewise network configurations in which each local Ethernet contains isolated traffic for its own 5-10 (diskless) clients and dedicated server. For overall connectivity, these local networks are usually joined together with an Ethernet backbone or, in the future, with an FDDI backbone. These backbones are typically connected to the local networks either by IP routers or MAC-level bridges, coupling the local networks together directly, or by a second server functioning as a network interface, coupling servers for all the local networks together.

In addition to performance considerations, the low client-to-server ratio creates computing problems in several additional ways:

1. Sharing. Development groups of more than 5-10 people cannot share the same server, and thus cannot easily share files without file replication and manual, multi-server updates. Bridges or routers are a partial solution but inflict a performance penalty due to more network hops.

2. Administration. System administrators must maintain many limited-capacity servers rather than a few more substantial servers. This burden includes network administration, hardware maintenance, and user account administration.

3. File System Backup. System administrators or operators must conduct multiple file system backups, which can be onerously time consuming tasks. It is also expensive to duplicate backup peripherals on each server (or every few servers if slower network backup is used).

4. Price Per Seat. With only 5-10 clients per server, the cost of the server must be shared by only a small number of users. The real cost of an entry-level Unix workstation is therefore significantly greater, often as much as 140% greater, than the cost of the workstation alone.

The widening I/O gap, as well as administrative and economic considerations, demonstrates a need for higher-performance, larger-capacity Unix file servers. Conversion of a display-less workstation into a server may address disk capacity issues, but does nothing to address fundamental I/O limitations. As an NFS server, the one-time workstation must sustain 5-10 or more times the network, disk, backplane, and file system throughput than it was designed to support as a client. Adding larger disks, more network adaptors,

extra primary memory, or even a faster processor do not resolve basic architectural I/O constraints; I/O throughput does not increase sufficiently.

Other prior art computer architectures, while not specifically designed as file servers, may potentially be used as such. In one such well-known architecture, a CPU, a memory unit, and two I/O processors are connected to a single bus. One of the I/O processors operates a set of disk drives, and if the architecture is to be used as a server, the other I/O processor would be connected to a network. This architecture is not optimal as a file server, however, at least because the two I/O processors cannot handle network file requests without involving the CPU. All network file requests that are received by the network I/O processor are first transmitted to the CPU, which makes appropriate requests to the disk-I/O processor for satisfaction of the network request.

In another such computer architecture, a disk controller CPU manages access to disk drives, and several other CPUs, three for example, may be clustered around the disk controller CPU. Each of the other CPUs can be connected to its own network. The network CPUs are each connected to the disk controller CPU as well as to each other for interprocessor communication. One of the disadvantages of this computer architecture is that each CPU in the system runs its own complete operating system. Thus, network file server requests must be handled by an operating system which is also heavily loaded with facilities and processes for performing a large number of other, non file-server tasks. Additionally, the interprocessor communication is not optimized for file server type requests.

In yet another computer architecture, a plurality of CPUs, each having its own cache memory for data and

instruction storage, are connected to a common bus with a system memory and a disk controller. The disk controller and each of the CPUs have direct memory access to the system memory, and one or more of the CPUs can be connected to a network. This architecture is disadvantageous as a file server because, among other things, both file data and the instructions for the CPUs reside in the same system memory. There will be instances, therefore, in which the CPUs must stop running while they wait for large blocks of file data to be transferred between system memory and the network CPU. Additionally, as with both of the previously described computer architectures, the entire operating system runs on each of the CPUs, including the network CPU.

In yet another type of computer architecture, a large number of CPUs are connected together in a hypercube topology. One of more of these CPUs can be connected to networks, while another can be connected to disk drives. This architecture is also disadvantageous as a file server because, among other things, each processor runs the entire operating system. Interprocessor communication is also not optimal for file server applications.

SUMMARY OF THE INVENTION

The present invention involves a new, server-specific I/O architecture that is optimized for a Unix file server's most common actions -- file operations. Roughly stated, the invention involves a file server architecture comprising one or more network controllers, one or more file controllers, one or more storage processors, and a system or buffer memory, all connected over a message passing bus and operating in parallel with the Unix host processor. The network controllers each connect to one or more network, and

provide all protocol processing between the network layer data format and an internal file server format for communicating client requests to other processors in the server. Only those data packets which cannot be interpreted by the network controllers, for example client requests to run a client-defined program on the server, are transmitted to the Unix host for processing. Thus the network controllers, file controllers and storage processors contain only small parts of an overall operating system, and each is optimized for the particular type of work to which it is dedicated.

Client requests for file operations are transmitted to one of the file controllers which, independently of the Unix host, manages the virtual file system of a mass storage device which is coupled to the storage processors. The file controllers may also control data buffering between the storage processors and the network controllers, through the system memory. The file controllers preferably each include a local buffer memory for caching file control information, separate from the system memory for caching file data. Additionally, the network controllers, file processors and storage processors are all designed to avoid any instruction fetches from the system memory, instead keeping all instruction memory separate and local. This arrangement eliminates contention on the backplane between microprocessor instruction fetches and transmissions of message and file data.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described with respect to particular embodiments thereof, and reference will be made to the drawings, in which:

Fig. 1. is a block diagram of a prior art file server architecture;

Fig. 2 is a block diagram of a file server architecture according to the invention;

Fig. 3 is a block diagram of one of the network controllers shown in Fig. 2;

Fig. 4 is a block diagram of one of the file controllers shown in Fig. 2;

Fig. 5 is a block diagram of one of the storage processors shown in Fig. 2;

Fig. 6 is a block diagram of one of the system memory cards shown in Fig. 2;

Figs. 7A-C are a flowchart illustrating the operation of a fast transfer protocol BLOCK WRITE cycle; and

Figs. 8A-C are a flowchart illustrating the operation of a fast transfer protocol BLOCK READ cycle.

DETAILED DESCRIPTION

For comparison purposes and background, an illustrative prior-art file server architecture will first be described with respect to Fig. 1. Fig. 1 is an overall block diagram of a conventional prior-art Unix-based file server for Ethernet networks. It consists of a host CPU card 10 with a single microprocessor on board. The host CPU card 10 connects to an Ethernet #1 12, and it connects via a memory management unit (MMU) 11 to a large memory array 16. The host CPU card 10 also drives a keyboard, a video display, and two RS232 ports (not shown). It also connects via the MMU 11 and a standard 32-bit VME bus 20 to various peripheral devices, including an SMD disk controller 22 controlling one or two disk drives 24, a SCSI host adaptor 26 connected to a SCSI bus 28, a tape controller 30 connected to a quarter-inch tape drive 32, and possibly a network #2 controller 34 connected

to a second Ethernet 36. The SMD disk controller 22 can communicate with memory array 16 by direct memory access via bus 20 and MMU 11, with either the disk controller or the MMU acting as a bus master. This configuration is illustrative; many variations are available.

The system communicates over the Ethernets using industry standard TCP/IP and NFS protocol stacks. A description of protocol stacks in general can be found in Tanenbaum, "Computer Networks" (Second Edition, Prentice Hall: 1988). File server protocol stacks are described at pages 535-546. The Tanenbaum reference is incorporated herein by reference.

Basically, the following protocol layers are implemented in the apparatus of Fig. 1:

Network Layer. The network layer converts data packets between a formal specific to Ethernets and a format which is independent of the particular type of network used. the Ethernet-specific format which is used in the apparatus of Fig. 1 is described in Hornig, "A Standard For The Transmission of IP Datagrams Over Ethernet Networks," RFC 894 (April 1984), which is incorporated herein by reference.

The Internet Protocol (IP) Layer. This layer provides the functions necessary to deliver a package of bits (an internet datagram) from a source to a destination over an interconnected system of networks. For messages to be sent from the file server to a client, a higher level in the server calls the IP module, providing the internet address of the destination client and the message to transmit. The IP module performs any required fragmentation of the message to accommodate packet size limitations of any intervening gateway, adds internet headers to each fragment, and calls on the network layer to transmit the resulting internet datagrams. The internet header

includes a local network destination address (translated from the internet address) as well as other parameters.

For messages received by the IP layer from the network layer, the IP module determines from the internet address whether the datagram is to be forwarded to another host on another network, for example on a second Ethernet such as 36 in Fig. 1, or whether it is intended for the server itself. If it is intended for another host on the second network, the IP module determines a local net address for the destination and calls on the local network layer for that network to send the datagram. If the datagram is intended for an application program within the server, the IP layer strips off the header and passes the remaining portion of the message to the appropriate next higher layer. The internet protocol standard used in the illustrative apparatus of Fig. 1 is specified in Information Sciences Institute, "Internet Protocol, DARPA Internet Program Protocol Specification," RFC 791 (September 1981), which is incorporated herein by reference.

TCP/UDP Layer. This layer is a datagram service with more elaborate packaging and addressing options than the IP layer. For example, whereas an IP datagram can hold about 1,500 bytes and be addressed to hosts, UDP datagrams can hold about 64KB and be addressed to a particular port within a host. TCP and UDP are alternative protocols at this layer; applications requiring ordered reliable delivery of streams of data may use TCP, whereas applications (such as NFS) which do not require ordered and reliable delivery may use UDP.

The prior art file server of Fig. 1 uses both TCP and UDP. It uses UDP for file server-related services, and uses TCP for certain other services

which the server provides to network clients. The UDP is specified in Postel, "User Datagram Protocol," RFC 768 (August 28, 1980), which is incorporated herein by reference. TCP is specified in Postel, "Transmission Control Protocol," RFC 761 (January 1980) and RFC 793 (September 1981), which is also incorporated herein by reference.

XDR/RPC Layer. This layer provides functions callable from higher level programs to run a designated procedure on a remote machine. It also provides the decoding necessary to permit a client machine to execute a procedure on the server. For example, a caller process in a client node may send a call message to the server of Fig. 1. The call message includes a specification of the desired procedure, and its parameters. The message is passed up the stack to the RPC layer, which calls the appropriate procedure within the server. When the procedure is complete, a reply message is generated and RPC passes it back down the stack and over the network to the caller client. RPC is described in Sun Microsystems, Inc., "RPC: Remote Procedure Call Protocol Specification, Version 2," RFC 1057 (June 1988), which is incorporated herein by reference.

RPC uses the XDR external data representation standard to represent information passed to and from the underlying UDP layer. XDR is merely a data encoding standard, useful for transferring data between different computer architectures. Thus, on the network side of the XDR/RPC layer, information is machine-independent; on the host application side, it may not be. XDR is described in Sun Microsystems, Inc., "XDR: External Data Representation Standard," RFC 1014 (June 1987), which is incorporated herein by reference.

NFS Layer. The NFS ("network file system") layer is one of the programs available on the server which an RPC request can call. The combination of host address, program number, and procedure number in an RPC request can specify one remote NFS procedure to be called.

Remote procedure calls to NFS on the file server of Fig. 1 provide transparent, stateless, remote access to shared files on the disks 24. NFS assumes a file system that is hierarchical, with directories as all but the bottom level of files. Client hosts can call any of about 20 NFS procedures including such procedures as reading a specified number of bytes from a specified file; writing a specified number of bytes to a specified file; creating, renaming and removing specified files; parsing directory trees; creating and removing directories; and reading and setting file attributes. The location on disk to which and from which data is stored and retrieved is always specified in logical terms, such as by a file handle or Inode designation and a byte offset. The details of the actual data storage are hidden from the client. The NFS procedures, together with possible higher level modules such as Unix VFS and UFS, perform all conversion of logical data addresses to physical data addresses such as drive, head, track and sector identification. NFS is specified in Sun Microsystems, Inc., "NFS: Network File System Protocol Specification," RFC 1094 (March 1989), incorporated herein by reference.

With the possible exception of the network layer, all the protocol processing described above is done in software, by a single processor in the host CPU card 10. That is, when an Ethernet packet arrives on Ethernet 12, the host CPU 10 performs all the protocol processing in the NFS stack, as well as the protocol

processing for any other application which may be running on the host 10. NFS procedures are run on the host CPU 10, with access to memory 16 for both data and program code being provided via MMU 11. Logically specified data addresses are converted to a much more physically specified form and communicated to the SMD disk controller 22 or the SCSI bus 28, via the VME bus 20, and all disk caching is done by the host CPU 10 through the memory 16. The host CPU card 10 also runs procedures for performing various other functions of the file server, communicating with tape controller 30 via the VME bus 20. Among these are client-defined remote procedures requested by client workstations.

If the server serves a second Ethernet 36, packets from that Ethernet are transmitted to the host CPU 10 over the same VME bus 20 in the form of IP datagrams. Again, all protocol processing except for the network layer is performed by software processes running on the host CPU 10. In addition, the protocol processing for any message that is to be sent from the server out on either of the Ethernets 12 or 36 is also done by processes running on the host CPU 10.

It can be seen that the host CPU 10 performs an enormous amount of processing of data, especially if 5-10 clients on each of the two Ethernets are making file server requests and need to be sent responses on a frequent basis. The host CPU 10 runs a multitasking Unix operating system, so each incoming request need not wait for the previous request to be completely processed and returned before being processed. Multiple processes are activated on the host CPU 10 for performing different stages of the processing of different requests, so many requests may be in process at the same time. But there is only one CPU on the card 10, so the processing of these requests is not accomplished in a truly parallel manner. The

processes are instead merely time sliced. The CPU 10 therefore represents a major bottleneck in the processing of file server requests.

Another bottleneck occurs in MMU 11, which must transmit both instructions and data between the CPU card 10 and the memory 16. All data flowing between the disk drives and the network passes through this interface at least twice.

Yet another bottleneck can occur on the VME bus 20, which must transmit data among the SMD disk controller 22, the SCSI host adaptor 26, the host CPU card 10, and possibly the network #2 controller 24.

PREFERRED EMBODIMENT-OVERALL HARDWARE ARCHITECTURE

In Fig. 2 there is shown a block diagram of a network file server 100 according to the invention. It can include multiple network controller (NC) boards, one or more file controller (FC) boards, one or more storage processor (SP) boards, multiple system memory boards, and one or more host processors. The particular embodiment shown in Fig. 2 includes four network controller boards 110a-110d, two file controller boards 112a-112b, two storage processors 114a-114b, four system memory cards 116a-116d for a total of 192MB of memory, and one local host processor 118. The boards 110, 112, 114, 116 and 118 are connected together over a VME bus 120 on which an enhanced block transfer mode as described in the ENHANCED VMEBUS PROTOCOL application identified above may be used. Each of the four network controllers 110 shown in Fig. 2 can be connected to up to two Ethernets 122, for a total capacity of 8 Ethernets 122a-122h. Each of the storage processors 114 operates ten parallel SCSI busses, nine of which can each support up to three SCSI disk drives each. The tenth SCSI channel on each of the storage processors

114 is used for tape drives and other SCSI peripherals.

The host 118 is essentially a standard SunOs Unix processor, providing all the standard Sun Open Network Computing (ONC) services except NFS and IP routing. Importantly, all network requests to run a user-defined procedure are passed to the host for execution. Each of the NC boards 110, the FC boards 112 and the SP boards 114 includes its own independent 32-bit microprocessor. These boards essentially off-load from the host processor 118 virtually all of the NFS and disk processing. Since the vast majority of messages to and from clients over the Ethernets 122 involve NFS requests and responses, the processing of these requests in parallel by the NC, FC and SP processors, with minimal involvement by the local host 118, vastly improves file server performance. Unix is explicitly eliminated from virtually all network, file, and storage processing.

OVERALL SOFTWARE ORGANIZATION AND DATA FLOW

Prior to a detailed discussion of the hardware subsystems shown in Fig. 2, an overview of the software structure will now be undertaken. The software organization is described in more detail in the above-identified application entitled MULTIPLE FACILITY OPERATING SYSTEM ARCHITECTURE.

Most of the elements of the software are well known in the field and are found in most networked Unix systems, but there are two components which are not: Local NFS ("LNFS") and the messaging kernel ("MK") operating system kernel. These two components will be explained first.

The Messaging Kernel. The various processors in file server 100 communicate with each other through the use of a messaging kernel running on each of the

processors 110, 112, 114 and 118. These processors do not share any instruction memory, so task-level communication cannot occur via straightforward procedure calls as it does in conventional Unix. Instead, the messaging kernel passes messages over VME bus 120 to accomplish all necessary inter-processor communication. Message passing is preferred over remote procedure calls for reasons of simplicity and speed.

Messages passed by the messaging kernel have a fixed 128-byte length. Within a single processor, messages are sent by reference; between processors, they are copied by the messaging kernel and then delivered to the destination process by reference. The processors of Fig. 2 have special hardware, discussed below, that can expediently exchange and buffer inter-processor messaging kernel messages.

The LNFS Local NFS interface. The 22-function NFS standard was specifically designed for stateless operation using unreliable communication. This means that neither clients nor server can be sure if they hear each other when they talk (unreliability). In practice, an in an Ethernet environment, this works well.

Within the server 100, however, NFS level datagrams are also used for communication between processors, in particular between the network controllers 110 and the file controller 112, and between the host processor 118 and the file controller 112. For this internal communication to be both efficient and convenient, it is undesirable and impractical to have complete statelessness or unreliable communications. Consequently, a modified form of NFS, namely LNFS, is used for internal communication of NFS requests and responses. LNFS is used only within the file server 100; the external network protocol supported by the

server is precisely standard, licensed NFS. LNFS is described in more detail below.

The Network Controllers 110 each run an NFS server which, after all protocol processing is done up to the NFS layer, converts between external NFS requests and responses and internal LNFS requests and responses. For example, NFS requests arrive as RPC requests with XDR and enclosed in a UDP datagram. After protocol processing, the NFS server translates the NFS request into LNFS form and uses the messaging kernel to send the request to the file controller 112.

The file controller runs an LNFS server which handles LNFS requests both from network controllers and from the host 118. The LNFS server translates LNFS requests to a form appropriate for a file system server, also running on the file controller, which manages the system memory file data cache through a block I/O layer.

An overview of the software in each of the processors will now be set forth.

Network Controller 110

The optimized dataflow of the server 100 begins with the intelligent network controller 110. This processor receives Ethernet packets from client workstations. It quickly identifies NFS-destined packets and then performs full protocol processing on them to the NFS level, passing the resulting LNFS requests directly to the file controller 112. This protocol processing includes IP routing and reassembly, UDP demultiplexing, XDR decoding, and NFS request dispatching. The reverse steps are used to send an NFS reply back to a client. Importantly, these time-consuming activities are performed directly in the Network Controller 110, not in the host 118.

The server 100 uses conventional NFS ported from Sun Microsystems, Inc., Mountain View, CA, and is NFS protocol compatible.

Non-NFS network traffic is passed directly to its destination host processor 118.

The NCs 110 also perform their own IP routing. Each network controller 110 supports two fully parallel Ethernets. There are four network controllers in the embodiment of the server 100 shown in Fig. 2, so that server can support up to eight Ethernets. For the two Ethernets on the same network controller 110, IP routing occurs completely within the network controller and generates no backplane traffic. Thus attaching two mutually active Ethernets to the same controller not only minimizes their internet transit time, but also significantly reduces backplane contention on the VME bus 120. Routing table updates are distributed to the network controllers from the host processor 118, which runs either the gated or routed Unix demon.

While the network controller described here is designed for Ethernet LANs, it will be understood that the invention can be used just as readily with other network types, including FDDI.

File Controller 112

In addition to dedicating a separate processor for NFS protocol processing and IP routing, the server 100 also dedicates a separate processor, the intelligent file controller 112, to be responsible for all file system processing. It uses conventional Berkeley Unix 4.3 file system code and uses a binary-compatible data representation on disk. These two choices allow all standard file system utilities (particularly block-level tools) to run unchanged.

The file controller 112 runs the shared file system used by all NCs 110 and the host processor 118. Both the NCs and the host processor communicate with the file controller 112 using the LNFS interface. The NCs 110 use LNFS as described above, while the host processor 118 uses LNFS as a plug-in module to SunOs's standard Virtual File System ("VFS") interface.

When an NC receives an NFS read request from a client workstation, the resulting LNFS request passes to the FC 112. The FC 112 first searches the system memory 116 buffer cache for the requested data. If found, a reference to the buffer is returned to the NC 110. If not found, the LRU (least recently used) cache buffer in system memory 116 is freed and reassigned for the requested block. The FC then directs the SP 114 to read the block into the cache buffer from a disk drive array. When complete, the SP so notifies the FC, which in turn notifies the NC 100. The NC 110 then sends an NFS reply, with the data from the buffer, back to the NFS client workstation out on the network. Note that the SP 114 transfers the data into system memory 116, if necessary, and the NC 110 transferred the data from system memory 116 to the networks. The process takes place without any involvement of the host 118.

Storage Processor

The intelligent storage processor 114 manages all disk and tape storage operations. While autonomous, storage processors are primarily directed by the file controller 112 to move file data between system memory 116 and the disk subsystem. The exclusion of both the host 118 and the FC 112 from the actual data path helps to supply the performance needed to service many remote clients.

Additionally, coordinated by a Server Manager in the host 118, storage processor 114 can execute server backup by moving data between the disk subsystem and tape or other archival peripherals on the SCSI channels. Further, if directly accessed by host processor 118, SP 114 can provide a much higher performance conventional disk interface for Unix, virtual memory, and databases. In Unix nomenclature, the host processor 118 can mount boot, storage swap, and raw partitions via the storage processors 114.

Each storage processor 114 operates ten parallel, fully synchronous SCSI channels (busses) simultaneously. Nine of these channels support three arrays of nine SCSI disk drives each, each drive in an array being assigned to a different SCSI channel. The tenth SCSI channel hosts up to seven tape and other SCSI peripherals. In addition to performing reads and writes, SP 114 performs device-level optimizations such as disk seek queue sorting, directs device error recovery, and controls DMA transfers between the devices and system memory 116.

Host Processor 118

The local host 118 has three main purposes: to run Unix, to provide standard ONC network services for clients, and to run a Server Manager. Since Unix and ONC are ported from the standard SunOs Release 4 and ONC Services Release 2, the server 100 can provide identically compatible high-level ONC services such as the Yellow Pages, Lock Manager, DES Key Authenticator, Auto Mounter, and Port Mapper. Sun/2 Network disk booting and more general IP internet services such as Telnet, FTP, SMTP, SNMP, and reverse ARP are also supported. Finally, print spoolers and similar Unix demons operate transparently.

The host processor 118 runs the following software modules:

TCP and socket layers. The Transport Control Protocol ("TCP"), which is used for certain server functions other than NFS, provides reliable bytestream communication between two processors. Socket are used to establish TCP connections.

VFS interface. The Virtual File System ("VFS") interface is a standard SunOs file system interface. It paints a uniform file-system picture for both users and the non-file parts of the Unix operating system, hiding the details of the specific file system. Thus standard NFS, LNFS, and any local Unix file system can coexist harmoniously.

UFS interface. The Unix File System ("UFS") interface is the traditional and well-known Unix interface for communication with local-to-the-processor disk drives. In the server 100, it is used to occasionally mount storage processor volumes directly, without going through the file controller 112. Normally, the host 118 uses LNFS and goes through the file controller.

Device layer. The device layer is a standard software interface between the Unix device model and different physical device implementations. In the server 100, disk devices are not attached to host processors directly, so the disk driver in the host's device layer uses the messaging kernel to communicate with the storage processor 114.

Route and Port Mapper Demons. The Route and Port Mapper demons are Unix user-level background processes that maintain the Route and Port databases for packet routing. They are mostly inactive and not in any performance path.

Yellow Pages and Authentication Demon. The Yellow Pages and Authentication services are Sun-ONC standard

network services. Yellow Pages is a widely used multipurpose name-to-name directory lookup service. The Authentication service uses cryptographic keys to authenticate, or validate, requests to insure that requestors have the proper privileges for any actions or data they desire.

Server Manager. The Server Manager is an administrative application suite that controls configuration, logs error and performance reports, and provides a monitoring and tuning interface for the system administrator. These functions can be exercised from either system console connected to the host 118, or from a system administrator's workstation.

The host processor 118 is a conventional OEM Sun central processor card, Model 3E/120. It incorporates a Motorola 68020 microprocessor and 4MB of on-board memory. Other processors, such as a SPARC-based processor, are also possible.

The structure and operation of each of the hardware components of server 100 will now be described in detail.

NETWORK CONTROLLER HARDWARE ARCHITECTURE

Fig. 3 is a block diagram showing the data path and some control paths for an illustrative one of the network controllers 110a. It comprises a 20 MHz 68020 microprocessor 210 connected to a 32-bit microprocessor data bus 212. Also connected to the microprocessor data bus 212 is a 256K byte CPU memory 214. The low order 8 bits of the microprocessor data bus 212 are connected through a bidirectional buffer 216 to an 8-bit slow-speed data bus 218. On the slow-speed data bus 218 is a 128K byte EPROM 220, a 32 byte PROM 222, and a multi-function peripheral (MFP) 224. The EPROM 220 contains boot code for the network

controller 110a, while the PROM 222 stores various operating parameters such as the Ethernet addresses assigned to each of the two Ethernet interfaces on the board. Ethernet address information is read into the corresponding interface control block in the CPU memory 214 during initialization. The MFP 224 is a Motorola 68901, and performs various local functions such as timing, interrupts, and general purpose I/O. The MFP 224 also includes a UART for interfacing to an RS232 port 226. These functions are not critical to the invention and will not be further described herein.

The low order 16 bits of the microprocessor data bus 212 are also coupled through a bidirectional buffer 230 to a 16-bit LAN data bus 232. A LAN controller chip 234, such as the Am7990 LANCE Ethernet controller manufactured by Advanced Micro Devices, Inc. Sunnyvale, CA., interfaces the LAN data bus 232 with the first Ethernet 122a shown in Fig. 2. Control and data for the LAN controller 234 are stored in a 512K byte LAN memory 236, which is also connected to the LAN data bus 232. A specialized 16 to 32 bit FIFO chip 240, referred to herein as a parity FIFO chip and described below, is also connected to the LAN data bus 232. Also connected to the LAN data bus 232 is a LAN DMA controller 242, which controls movements of packets of data between the LAN memory 236 and the FIFO chip 240. The LAN DMA controller 242 may be a Motorola M68440 DMA controller using channel zero only.

The second Ethernet 122b shown in Fig. 2 connects to a second LAN data bus 252 on the network controller card 110a shown in Fig. 3. The LAN data bus 252 connects to the low order 16 bits of the microprocessor data bus 212 via a bidirectional buffer 250, and has similar components to those appearing on

the LAN data bus 232. In particular, a LAN controller 254 interfaces the LAN data bus 252 with the Ethernet 122b, using LAN memory 256 for data and control, and a LAN DMA controller 262 controls DMA transfer of data between the LAN memory 256 and the 16-bit wide data port A of the parity FIFO 260.

The low order 16 bits of microprocessor data bus 212 are also connected directly to another parity FIFO 270, and also to a control port of a VME/FIFO DMA controller 272. The FIFO 270 is used for passing messages between the CPU memory 214 and one of the remote boards 110, 112, 114, 116 or 118 (Fig. 2) in a manner described below. The VME/FIFO DMA controller 272, which supports three round-robin non-prioritized channels for copying data, controls all data transfers between one of the remote boards and any of the FIFOs 240, 260 or 270, as well as between the FIFOs 240 and 260.

32-bit data bus 274, which is connected to the 32-bit port B of each of the FIFOs 240, 260 and 270, is the data bus over which these transfers take place. Data bus 274 communicates with a local 32-bit bus 276 via a bidirectional pipelining latch 278, which is also controlled by VME/FIFO DMA controller 727, which in turn communicates with the VME bus 120 via a bidirectional buffer 280.

The local data bus 276 is also connected to a set of control registers 282, which are directly addressable across the VME bus 120. The registers 282 are used mostly for system initialization and diagnostics.

The local data bus 276 is also coupled to the microprocessor data bus 212 via a bidirectional buffer 284. When the NC 110a operates in slave mode, the CPU memory 214 is directly addressable from VME bus 120. One of the remote boards can copy data directly from

the CPU memory 214 via the bidirectional buffer 284. LAN memories 236 and 256 are not directly addressed over VME bus 120.

The parity FIFOs 240, 260 and 270 each consist of an ASIC, the functions and operation of which are described in the Appendix. The FIFOs 240 and 260 are configured for packet data transfer and the FIFO 270 is configured for massage passing. Referring to the Appendix, the FIFOs 240 and 260 are programmed with the following bit settings in the Data Transfer Configuration Register:

Bit	Definition	Setting
0	WD Mode	N/A
1	Parity Chip	N/A
2	Parity Correct Mode	N/A
3	8/16 bits CPU & PortA interface	16 bits(1)
4	Invert Port A address 0	no (0)
5	Invert Port A address 1	yes (1)
6	Checksum Carry Wrap	yes (1)
7	Reset	no (0)

The Data Transfer Control Register is programmed as follows:

Bit	Definition	Setting
0	Enable PortA Req/Ack	yes (1)
1	Enable PortB Req/Ack	yes (1)
2	Data Transfer Direction	(as desired)
3	CPU parity enable	no (0)
4	PortA parity enable	no (0)
5	PortB parity enable	no (0)
6	Checksum Enable	yes (1)
7	PortA Master	yes (1)

Unlike the configuration used on FIFOs 240 and 260, the microprocessor 210 is responsible for loading and unloading Port A directly. The microprocessor 210 reads an entire 32-bit word from port A with a single instruction using two port A access cycles. Port A

data transfer is disabled by unsetting bits 0 (Enable PortA Req/Ack) and 7 (PortA Master) of the Data Transfer Control Register.

The remainder of the control settings in FIFO 270 are the same as those in FIFOs 240 and 260 described above.

The NC 110a also includes a command FIFO 290. The command FIFO 290 includes an input port coupled to the local data bus 276, and which is directly addressable across the VME bus 120, and includes an output port connected to the microprocessor data bus 212. As explained in more detail below, when one of the remote boards issues a command or response to the NC 110a, it does so by directly writing a 1-word (32-bit) message descriptor into NC 110a's command FIFO 290. Command FIFO 290 generates a "FIFO not empty" status to the microprocessor 210, which then reads the message descriptor off the top of FIFO 290 and processes it. If the message is a command, then it includes a VME address at which the message is located (presumably an address in a shared memory similar to 214 on one of the remote boards). The microprocessor 210 then programs the FIFO 270 and the VME/FIFO DMA controller 272 to copy the message from the remote location into the CPU memory 214.

Command FIFO 290 is a conventional two-port FIFO, except that additional circuitry is included for generating a Bus Error signal on VME bus 120 if an attempt is made to write to the data input port while the FIFO is full. Command FIFO 290 has space for 256 entries.

A noteworthy feature of the architecture of NC 110a is that the LAN buses 232 and 252 are independent of the microprocessor data bus 212. Data packets being routed to or from an Ethernet are stored in LAN memory 236 on the LAN data bus 232 (or 256 on the LAN data

bus 252), and not in the CPU memory 214. Data transfer between the LAN memories 236 and 256 and the Ethernets 122a and 122b, are controlled by LAN controllers 234 and 254, respectively, while most data transfer between LAN memory 236 or 256 and a remote port on the VME bus 120 are controlled by LAN DMA controllers 242 and 262, FIFOs 240 and 260, and VME/FIFO DMA controller 272. An exception to this rule occurs when the size of the data transfer is small, e.g., less than 64 bytes, in which case microprocessor 210 copies it directly without using DMA. The microprocessor 210 is not involved in larger transfers except in initiating them and in receiving notification when they are complete.

The CPU memory 214 contains mostly instructions for microprocessor 210, messages being transmitted to or from a remote board via FIFO 270, and various data blocks for controlling the FIFOs, the DMA controllers and the LAN controllers. The microprocessor 210 accesses the data packets in the LAN memories 236 and 256 by directly addressing them through the bidirectional buffers 230 and 250, respectively, for protocol processing. The local high-speed static RAM in CPU memory 214 can therefore provide zero wait state memory access for microprocessor 210 independent of network traffic. This is in sharp contrast to the prior art architecture shown in Fig. 1, in which all data and data packets, as well as microprocessor instructions for host CPU card 10, reside in the memory 16 and must communicate with the host CPU card 10 via the MMU 11.

While the LAN data buses 232 and 252 are shown as separate buses in Fig. 3, it will be understood that they may instead be implemented as a single combined bus.

NETWORK CONTROLLER OPERATION

In operation, when one of the LAN controllers (such as 234) receives a packet of information over its Ethernet 122a, it reads in the entire packet and stores it in corresponding LAN memory 236. The LAN controller 234 then issues an interrupt to microprocessor 210 via MFP 224, and the microprocessor 210 examines the status register on LAN controller 234 (via bidirectional buffer 230) to determine that the event causing the interrupt was a "receive packet completed." In order to avoid a potential lockout of the second Ethernet 122b caused by the prioritized interrupt handling characteristic of MFP 224, the microprocessor 210 does not at this time immediately process the received packet; instead, such processing is scheduled for a polling function.

When the polling function reaches the processing of the received packet, control over the packet is passed to a software link level receive module. The link level receive module then decodes the packet according to either of two different frame formats: standard Ethernet format or SNAP (IEEE 802 LCC) format. An entry in the header in the packet specifies which frame format was used. The link level driver then determines which of three types of messages is contained in the received packet: (1) IP, (2) ARP packets which can be handled by a local ARP module, or (3) ARP packets and other packet types which must be forwarded to the local host 118 (Fig. 2) for processing. If the packet is an ARP packet which can be handled by the NC 110a, such as a request for the address of server 100, then the microprocessor 210 assembles a response packet in LAN memory 236 and, in a conventional manner, causes LAN controller 234 to transmit that packet back over Ethernet 122a. It is noteworthy that the data manipulation for

accomplishing this task is performed almost completely in LAN memory 236, directly addressed by microprocessor 210 as controlled by instructions in CPU memory 214. The function is accomplished also without generating any traffic on the VME backplane 120 at all, and without disturbing the local host 118.

If the received packet is either an ARP packet which cannot be processed completely in the NC 110a, or is another type of packet which requires delivery to the local host 118 (such as a client request for the server 100 to execute a client-defined procedure), then the microprocessor 210 programs LAN DMA controller 242 to load the packet from LAN memory 236 into FIFO 240, programs FIFO 240 with the direction of data transfer, and programs DMA controller 272 to read the packet out of FIFO 240 and across the VME bus 120 into system memory 116. In particular, the microprocessor 210 first programs the LAN DMA controller 242 with the starting address and length of the packet in LAN memory 236, and programs the controller to begin transferring data from the LAN memory 236 to port A of parity FIFO 240 as soon as the FIFO is ready to receive data. Second, microprocessor 210 programs the VME/FIFO DMA controller 272 with the destination address in system memory 116 and the length of the data packet, and instructs the controller to begin transferring data from port B of the FIFO 260 onto VME bus 120. Finally, the microprocessor 210 programs FIFO 240 with the direction of the transfer to take place. The transfer then proceeds entirely under the control of DMA controllers 242 and 272, without any further involvement by microprocessor 210.

The microprocessor 210 then sends a message to host 118 that a packet is available at a specified system memory address. The microprocessor 210 sends such a

message by writing a message descriptor to a software-emulated command FIFO on the host, which copies the message from CPU memory 214 on the NC via buffer 284 and into the host's local memory, in ordinary VME block transfer mode. The host then copies the packet from system memory 116 into the host's own local memory using ordinary VME transfers.

If the packet received by NC 110a from the network is an IP packet, then the microprocessor 210 determines whether it is (1) an IP packet for the server 100 which is not an NFS packet; (2) an IP packet to be routed to a different network; or (3) an NFS packet. If it is an IP packet for the server 100, but not an NFS packet, then the microprocessor 210 causes the packet to be transmitted from the LAN memory 236 to the host 118 in the same manner described above with respect to certain ARP packets.

If the IP packet is not intended for the server 100, but rather is to be routed to a client on a different network, then the packet is copied into the LAN memory associated with the Ethernet to which the destination client is connected. If the destination client is on the Ethernet 122b, which is on the same NC board as the source Ethernet 122a, then the microprocessor 210 causes the packet to be copied from LAN memory 236 into LAN 256 and then causes LAN controller 254 to transmit it over Ethernet 122b. (Of course, if the two LAN data buses 232 and 252 are combined, then copying would be unnecessary; the microprocessor 210 would simply cause the LAN controller 254 to read the packet out of the same locations in LAN memory to which the packet was written by LAN controller 234.)

The copying of a packet from LAN memory 236 to LAN memory 256 takes place similarly to the copying described above from LAN memory to system memory. For

transfer sizes of 64 bytes or more, the microprocessor 210 first programs the LAN DMA controller 242 with the starting address and length of the packet in LAN memory 236, and programs the controller to begin transferring data from the LAN memory 236 into port A of parity FIFO 240 as soon as the FIFO is ready to receive data. Second, microprocessor 210 programs the LAN DMA controller 262 with a destination address in LAN memory 256 and the length of the data packet, and instructs that controller to transfer data from parity FIFO 260 into the LAN memory 256. Third, microprocessor 210 programs the VME/FIFO DMA controller 272 to clock words of data out of port B of the FIFO 240, over the data bus 274, and into port B of FIFO 260. Finally, the microprocessor 210 programs the two FIFOs 240 and 260 with the direction of the transfer to take place. The transfer then proceeds entirely under the control of DMA controllers 242, 262 and 272, without any further involvement by the microprocessor 210. Like the copying from LAN memory to system memory, if the transfer size is smaller than 64 bytes, the microprocessor 210 performs the transfer directly, without DMA.

When each of the LAN DMA controllers 242 and 262 complete their work, they so notify microprocessor 210 by a respective interrupt provided through MFP 224. When the microprocessor 210 has received both interrupts, it programs LAN controller 254 to transmit the packet on the Ethernet 122b in a conventional manner.

Thus, IP routing between the two Ethernets in a single network controller 110 takes place over data bus 274, generating no traffic over VME bus 120. Nor is the host processor 118 disturbed for such routing, in contrast to the prior art architecture of Fig. 1. Moreover, all but the shortest copying work is

performed by controllers outside microprocessor 210, requiring the involvement of the microprocessor 210, and bus traffic on microprocessor data bus 212, only for the supervisory functions of programming the DMA controllers and the parity FIFOs and instructing them to begin. The VME/FIFO DMA controller 272 is programmed by loading control registers via microprocessor data bus 212; the LAN DMA controllers 242 and 262 are programmed by loading control registers on the respective controllers via the microprocessor data bus 212, respective bidirectional buffers 230 and 250, and respective LAN data buses 232 and 252, and the parity FIFOs 240 and 260 are programmed as set forth in the Appendix.

If the destination workstation of the IP packet to be routed is on an Ethernet connected to a different one of the network controllers 110, then the packet is copied into the appropriate LAN memory on the NC 110 to which that Ethernet is connected. Such copying is accomplished by first copying the packet into system memory 116, in the manner described above with respect to certain ARP packets, and then notifying the destination NC that a packet is available. When an NC is so notified, it programs its own parity FIFO and DMA controllers to copy the packet from system memory 116 into the appropriate LAN memory. It is noteworthy that though this type of IP routing does create VME bus traffic, it still does not involve the host CPU 118.

If the IP packet received over the Ethernet 122a and now stored in LAN memory 236 is an NFS packet intended for the server 100, then the microprocessor 210 performs all necessary protocol preprocessing to extract the NFS message and convert it to the local NFS (LNFS) format. This may well involve the logical concatenation of data extracted from a large number of

individual IP packets stored in LAN memory 236, resulting in a linked list, in CPU memory 214, pointing to the different blocks of data in LAN memory 236 in the correct sequence.

The exact details of the LNFS format are not important for an understanding of the invention, except to note that it includes commands to maintain a directory of files which are stored on the disks attached to the storage processors 114, commands for reading and writing data to and from a file on the disks, and various configuration management and diagnostics control messages. The directory maintenance commands which are supported by LNFS include the following messages based on conventional NFS: get attributes of a file (GETATTR); set attributes of a file (SETATTR); look up a file (LOOKUP); created a file (CREATE); remove a file (REMOVE); rename a file (RENAME); created a new linked file (LINK); create a symlink (SYMLINK); remove a directory (RMDIR); and return file system statistics (STATFS). The data transfer commands supported by LNFS include read from a file (READ); write to a file (WRITE); read from a directory (READDIR); and read a link (READLINK). LNFS also supports a buffer release command (RELEASE), for notifying the file controller that an NC is finished using a specified buffer in system memory. It also supports a VOP-derived access command, for determining whether a given type access is legal for specified credential on a specified file.

If the LNFS request includes the writing of file data from the LAN memory 236 to disk, the NC 110a first requests a buffer in system memory 116 to be allocated by the appropriate FC 112. When a pointer to the buffer is returned, microprocessor 210 programs LAN DMA controller 242, parity FIFO 240 and VME/FIFO DMA controller 272 to transmit the entire block of

file data to system memory 116. The only difference between this transfer and the transfer described above for transmitting IP packets and ARP packets to system memory 116 is that these data blocks will typically have portions scattered throughout LAN memory 236. The microprocessor 210 accommodates that situation by programming LAN DMA controller 242 successively for each portion of the data, in accordance with the linked list, after receiving notification that the previous portion is complete. The microprocessor 210 can program the parity FIFO 240 and the VME/FIFO DMA controller 272 once for the entire message, as long as the entire data block is to be placed contiguously in system memory 116. If it is not, then the microprocessor 210 can program the DMA controller 272 for successive blocks in the same manner LAN DMA controller 242.

If the network controller 110a receives a message from another processor in server 100, usually from file controller 112, that file data is available in system memory 116 for transmission on one of the Ethernets, for example Ethernet 122a, then the network controller 110a copies the file data into LAN memory 236 in a manner similar to the copying of file data in the opposite direction. In particular, the microprocessor 210 first programs VME/FIFO DMA controller 272 with the starting address and length of the data in system memory 116, and programs the controller to begin transferring data over the VME bus 120 into port B of parity FIFO 240 as soon as the FIFO is ready to receive data. The microprocessor 210 then programs the LAN DMA controller 242 with a destination address in LAN memory 236 and then length of the file data, and instructs that controller to transfer data from the parity FIFO 240 into the LAN memory 236. Third, microprocessor 210 programs the parity FIFO 240

with the direction of the transfer to take place. The transfer then proceeds entirely under the control of DMA controllers 242 and 272, without any further involvement by the microprocessor 210. Again, if the file data is scattered in multiple blocks in system memory 116, the microprocessor 210 programs the VME/FIFO DMA controller 272 with a linked list of the blocks to transfer in the proper order.

When each of the DMA controllers 242 and 272 complete their work, they so notify microprocessor 210 through MFP 224. The microprocessor 210 then performs all necessary protocol processing on the LNFS message in LAN memory 236 in order to prepare the message for transmission over the Ethernet 122a in the form of Ethernet IP packets. As set forth above, this protocol processing is performed entirely in network controller 110a, without any involvement of the local host 118.

It should be noted that the parity FIFOs are designed to move multiples of 128-byte blocks most efficiently. The data transfer size through port B is always 32-bits wide, and the VME address corresponding to the 32-bit data must be quad-byte aligned. The data transfer size for port A can be either 8 or 16 bits. For bus utilization reasons, it is set to 16 bits when the corresponding local start address is double-byte aligned, and is set at 8 bits otherwise. The TCP/IP checksum is always computed in the 16 bit mode. Therefore, the checksum word requires byte swapping if the local start address is not double-byte aligned.

Accordingly, for transfer from port B to port A of any of the FIFOs 240, 260 or 270, the microprocessor 210 programs the VME/FIFO DMA controller to pad the transfer count to the next 128-byte boundary. The extra 32-bit word transfers do not involve the VME

bus, and only the desired number of 32-bit words will be unloaded from port A.

For transfers from port A to port B of the parity FIFO 270, the microprocessor 210 loads port A word-by-word and forces a FIFO full indication when it is finished. The FIFO full indication enables unloading from port B. The same procedure also takes place for transfers from port A to port B of either of the parity FIFOs 240 or 260, since transfers of fewer than 128 bytes are performed under local microprocessor control rather than under the control of LAN DMA controller 242 or 262. For all of the FIFOs, the VME/FIFO DMA controller is programmed to unload only the desired number of 32-bit words.

FILE CONTROLLER HARDWARE ARCHITECTURE

The file controllers (FC) 112 may each be a standard off-the-shelf microprocessor board, such as one manufactured by Motorola Inc. Preferably, however, a more specialized board is used such as that shown in block diagram form in Fig. 4.

Fig. 4 shows one of the FCs 112a, and it will be understood that the other FC can be identical. In many aspects it is simply a scaled-down version of the NC 110a shown in Fig. 3, and in some respects it is scaled up. Like the NC 110a, FC 112a comprises a 20MHz 68020 microprocessor 310 connected to a 32-bit microprocessor data bus 312. Also connected to the microprocessor data bus 312 is a 256K byte shared CPU memory 314. The low order 8 bits of the microprocessor data bus 312 are connected through a bidirectional buffer 316 to an 8-bit slow-speed data bus 318. On slow-speed data bus 318 are a 128K byte PROM 320, and a multifunction peripheral (MFP) 324. The functions of the PROM 320 and MFP 324 are the same as those described above with respect to EPROM 220 and

MFP 224 on NC 110a. FC 112a does not include PROM like the PROM 222 on NC 110a, but does include a parallel port 392. The parallel port 392 is mainly for testing and diagnostics.

Like the NC 110a, the FC 112a is connected to the VME bus 120 via a bidirectional buffer 380 and a 32-bit local data bus 376. A set of control registers 382 are connected to the local data bus 376, and directly addressable across the VME bus 120. The local data bus 376 is also coupled to the microprocessor data bus 312 via a bidirectional buffer 384. This permits the direct addressability of CPU memory 314 from VME bus 120.

FC 112a also includes a command FIFO 390, which includes an input port coupled to the local data bus 376 and which is directly addressable across the VME bus 120. The command FIFO 390 also includes an output port connected to the microprocessor data bus 312. The structure, operation and purpose of command FIFO 390 are the same as those described above with respect to command FIFO 290 on NC 110a.

The FC 112a omits the LAN data buses 323 and 352 which are present in NC 110a, but instead includes a 4 megabyte 32-bit wide FC memory 396 coupled to the microprocessor data bus 312 via a bidirectional buffer 394. As will be seen, FC memory 396 is used as a cache memory for file control information, separate from the file data information cached in system memory 116.

The file controller embodiment shown in Fig. 4 does not include any DMA controllers, and hence cannot act as a master for transmitting or receiving data in any block transfer mode, over the VME bus 120. Block transfers do occur with the CPU memory 314 and the FC memory 396, however, with the FC 112a acting as an VME bus slave. In such transfers, the remote master

addresses the CPU memory 314 or the FC memory 396 directly over the VME bus 120 through the bidirectional buffers 384 and, if appropriate, 394.

FILE CONTROLLER OPERATION

The purpose of the FC 112a is basically to provide virtual file system services in response to requests provided in LNFS format by remote processors on the VME bus 120. Most requests will come from a network controller 110, but requests may also come from the local host 118.

The file related commands supported by LNFS are identified above. They are all specified to the FC 112a in terms of logically identified disk data blocks. For example, the LNFS command for reading data from a file includes a specification of the file from which to read (file system ID (FSID) and file ID (inode)), a byte offset, and a count of the number of bytes to read. The FC 112a converts that identification into physical form, namely disk and sector numbers, in order to satisfy the command.

The FC 112a runs a conventional Fast File System (FFS or UFS), which is based on the Berkeley 4.3 VAX release. This code performs the conversion and also performs all disk data caching and control data caching. However, as previously mentioned, control data caching is performed using the FC memory 396 on FC 112a, whereas disk data caching is performed using the system memory 116 (Fig. 2). Caching this file control information within the FC 112a avoids the VME bus congestion and speed degradation which would result if file control information was cached in system memory 116. The memory on the FC 112a is directly accessed over the VME bus 120 for three main purposes. First, and by far the most frequent, are accesses to FC memory 396 by an SP 114 to read or

write cached file control information. These are accesses requested by FC 112a to write locally modified file control structures through to disk, or to read file control structures from disk. Second, the FC's CPU memory 314 is accessed directly by other processors for message transmissions from the FC 112a to such other processors. For example, if a data block in system memory is to be transferred to an SP 114 for writing to disk, the FC 112a first assembles a message in its local memory 314 requesting such a transfer. The FC 112a then notifies the SP 114, which copies the message directly from the CPU memory 314 and executes the requested transfer.

A third type of direct access to the FC's local memory occurs when an LNFS client reads directory entries. When FC 112a receives an LNFS request to read directory entries, the FC 112a formats the requested directory entries in FC memory 396 and notifies the requestor of their location. The requestor then directly accesses FC memory 396 to read the entries.

The version of the UFS code on FC 112a includes some modifications in order to separate the two caches. In particular, two sets of buffer headers are maintained, one for the FC memory 396 and one for the system memory 116. Additionally, a second set of the system buffer routines (GETBLK(), BRELSE(), BREAD(), BWRITE(), and BREADA()) exist, one for buffer accesses to FC Mem 396 and one for buffer accesses to system memory 116. The UFS code is further modified to call the appropriate buffer routines for FC memory 396 for accesses to file control information, and to call the appropriate buffer routines for the system memory 116 for the caching of disk data. A description of UFS may be found in chapters 2, 6, 7 and 8 of "Kernel Structure and Flow," by Rieken and Webb of .sh

consulting (Santa Clara, California: 1988), incorporated herein by reference.

When a read command is sent to the FC by a requestor such as a network controller, the FC first converts the file, offset and count information into disk and sector information. It then locks the system memory buffers which contain that information, instructing the storage processor 114 to read them from disk if necessary. When the buffer is ready, the FC returns a message to the requestor containing both the attributes of the designated file and an array of buffer descriptors that identify the locations in system memory 116 holding the data.

After the requestor has read the data out of the buffers, it sends a release request back to the FC. The release request is the same message that was returned by the FC in response to the read request; the FC 112a uses the information contained therein to determine which buffers to free.

A write command is processed by FC 112a similarly to the read command, but the caller is expected to write to (instead of read from) the locations in system memory 116 identified by the buffer descriptors returned by the FC 112a. Since FC 112a employs write-through caching, when it receives the release command from the requestor, it instructs storage processor 114 to copy the data from system memory 116 onto the appropriate disk sectors before freeing the system memory buffers for possible reallocation.

The READDIR transaction is similar to read and write, but the request is satisfied by the FC 112a directly out of its own FC memory 396 after formatting the requested directory information specifically for this purpose. The FC 112a causes the storage processor read the requested directory information from disk if it is not already locally cached. Also,

the specified offset is a "magic cookie" instead of a byte offset, identifying directory entries instead of an absolute byte offset into the file. No file attributes are returned.

The READLINK transaction also returns no file attributes, and since links are always read in their entirety, it does not require any offset or count.

For all of the disk data caching performed through system memory 116, the FC 112a acts as a central authority for dynamically allocating, deallocating and keeping track of buffers. If there are two or more FCs 112, each has exclusive control over its own assigned portion of system memory 116. In all of these transactions, the requested buffers are locked during the period between the initial request and the release request. This prevents corruption of the data by other clients.

Also in the situation where there are two or more FCs, each file system on the disks is assigned to a particular one of the FCs! FC #0 runs a process called FC_VICE_PRESIDENT, which maintains a list of which file systems are assigned to which FC. When a client processor (for example an NC 110) is about to make an LNFS request designating a particular file system, it first sends the fsid in a message to the FC_VICE_PRESIDENT asking which FC controls the specified file system. The FC_VICE_PRESIDENT responds, and the client processor sends the LNFS request to the designated FC. The client processor also maintains its own list of fsid/FC pairs as it discovers them, so as to minimize the number of such requests to the FC_VICE_PRESIDENT.

STORAGE PROCESSOR HARDWARE ARCHITECTURE

In the file server 100, each of the storage processors 114 can interface the VME bus 120 with up

to 10 different SCSI buses. Additionally, it can do so at the full usage rate of an enhanced block transfer protocol of 55MB per second.

Fig. 5 is a block diagram of one of the SPs 114a. SP 114b is identical. SP 114a comprises a microprocessor 510, which may be a Motorola 68020 microprocessor operating at 20MHz. The microprocessor 510 is coupled over a 32-bit microprocessor data bus 512 with CPU memory 514, which may include up to 1MB of static RAM. The microprocessor 510 accesses instructions, data and status on its own private bus 512, with no contention from any other source. The microprocessor 510 is the only master of bus 512.

The low order 16 bits of the microprocessor data bus 512 interface with a control bus 516 via a bidirectional buffer 518. The low order 8 bits of the control bus 516 interface with a slow speed bus 520 via another bidirectional buffer 522. The slow speed bus 520 connects to an MFP 524, similar to the MFP 224 in NC 110a (Fig. 3), and with a PROM 526, similar to PROM 220 on NC 110a. The PROM 526 comprises 128K bytes of EPROM which contains the functional code for SP 114a. Due to the width and speed of the EPROM 526, the functional code is copied to CPU memory 514 upon reset for faster execution.

MFP 524, like the MFP 224 on NC 110a, comprises a Motorola 68901 multifunction peripheral device. It provides the functions of a vectored interrupt controller, individually programmable I/O pins, four timers and a UART. The UART functions provide serial communications across an RS 232 bus (not shown in Fig. 5) for debug monitors and diagnostics. Two of the four timing functions may be used as general-purpose timers by the microprocessor 510, either independently or in cascaded fashion. A third timer function provides the refresh clock for a DMA controller

described below, and the fourth timer generates the UART clock. Additional information on the MFP 524 can be found in "MC 68901 Multi-Function Peripheral Specification," by Motorola, Inc., which is incorporated herein by reference. The eight general-purpose I/O bits provided by MFP 524 are configured according to the following table:

Bit	Direction	Definition
7	input	Power Failure is Imminent - This functions as an early warning.
6	input	SCSI Attention - A composite of the SCSI. Attentions from all 10 SCSI channels.
5	input	Channel Operation Done - A composite of the channel done bits from all 13 channels of the DMA controller, described below.
4	output	DMA Controller Enable. Enables the DMA Controller to run.
3	input	VMEbus Interrupt Done - Indicates the completion of a VMEbus Interrupt.
2	input	Command Available - Indicates that the SP'S Command Fifo, described below, contains one or more command pointers.
1	output	External Interrupts Disable. Disables externally generated interrupts to the microprocessor 510.
0	output	Command Fifo Enable. Enables operation of the SP'S Command Fifo. Clears the Command Fifo when reset.

Commands are provided to the SP 114a from the VME bus 120 via a bidirectional buffer 530, a local data bus 532, and a command FIFO 534. The command FIFO 534 is similar to the command FIFOs 290 and 390 on NC 110a and FC 112a, respectively, and has a depth of 256 32-bit entries. The command FIFO 534 is a write-only register as seen on the VME bus 120, and as a read-only register as seen by microprocessor 510. If the

FIFO is full at the beginning of a write from the VME bus, a VME bus error is generated. Pointers are removed from the command FIFO 534 in the order received, and only by the microprocessor 510. Command available status is provided through I/O bit 4 of the MFP 524, and as a long as one or more command pointers are still within the command FIFO 534, the command available status remains asserted.

As previously mentioned, the SP 114a supports up to 10 SCSI buses or channels 540a-540j. In the typical configuration, buses 540a-540i support up to 3 SCSI disk drives each, and channel 540j supports other SCSI peripherals such as tape drives, optical disks, and so on. Physically, the SP 114a connects to each of the SCSI buses with an ultra-miniature D sub connector and round shielded cables. Six 50-pin cables provide 300 conductors which carry 18 signals per bus and 12 grounds. The cables attach at the front panel of the SP 114a and to a commutator board at the disk drive array. Standard 50-pin cables connect each SCSI device to the commutator board. Termination resistors are installed on the SP 114a.

The SP 114a supports synchronous parallel data transfers up to 5MB per second on each of the SCSI buses 540, arbitration, and disconnect/reconnect services. Each SCSI bus 540 is connected to a respective SCSI adaptor 542, which in the present embodiment is an AIC 6250 controller IC manufactured by Adaptec Inc., Milpitas, California, operating in the non-multiplexed address bus mode. The AIC 6250 is described in detail in "AIC-6250 Functional Specification," by Adaptec Inc., which is incorporated herein by reference. The SCSI adaptors 542 each provide the necessary hardware interface and low-level electrical protocol to implement its respective SCSI channel.

The 8-bit data port of each of the SCSI adaptors 542 is connected to port A of a respective one of a set of ten parity FIFOs 544a-544j. The FIFOs 544 are the same as FIFOs 240, 260 and 270 on NC 110a, and are connected and configured to provide parity covered data transfers between the 8-bit data port of the respective SCSI adaptors 542 and a 36-bit (32-bit plus 4 bits of parity) common data bus 550. The FIFOs 544 provide handshake, status, word assembly/disassembly and speed matching FIFO buffering for this purpose. The FIFOs 544 also generate and check parity for the 32-bit bus, and for RAID 5 implementations they accumulate and check redundant data and accumulate recovered data.

All of the SCSI adaptors 542 reside at a single location of the address space of the microprocessor 510, as do all of the parity FIFOs 544. The microprocessor 510 selects individual controllers and FIFOs for access in pairs, by first programming a pair select register (not shown) to point to the desired pair and then reading from or writing to the control register address of the desired chip in the pair. The microprocessor 510 communicates with the control registers on the SCSI adaptors 542 via the control bus 516 and an additional bidirectional buffer 546, and communicates with the control registers on FIFOs 544 via the control bus 516 and a bidirectional buffer 552. Both the SCSI adaptors 542 and FIFOs 544 employ 8-bit control registers, and register addressing of the FIFOs 544 is arranged such that such registers alias in consecutive byte locations. This allows the microprocessor 510 to write to the registers as a single 32-bit register, thereby reducing instruction overhead.

The parity FIFOs 544 are each configured in their Adaptec 6250 mode. Referring to the Appendix, the

FIFOs 544 are programmed with the following bit settings in the Data Transfer Configuration Register:

Bit	Definition	Setting
0	WD Mode	(0)
1	Parity Chip	(1)
2	Parity Correct Mode	(0)
3	8/16 bits CPU & PortA interface	(0)
4	Invert Port A address 0	(1)
5	Invert Port A address 1	(1)
6	Checksum Carry Wrap	(0)
7	Reset	(0)

The Data Transfer Control Register is programmed as follows:

Bit	Definition	Setting
0	Enable PortA Req/Ack	(1)
1	Enable PortB Req/Ack	(1)
2	Data Transfer Direction	as desired
3	CPU parity enable	(0)
4	PortA parity enable	(1)
5	PortB parity enable	(1)
6	Checksum Enable	(0)
7	PortA Master	(0)

In addition, bit 4 of the RAM Access Control Register (Long Burst) is programmed for 8-byte bursts.

SCSI adaptors 542 each generate a respective interrupt signal, the status of which are provided to microprocessor 510 as 10 bits of a 16-bit SCSI interrupt register 556. The SCSI interrupt register 556 is connected to the control bus 516. Additionally, a composite SCSI interrupt is provided through the MFP 524 whenever any one of the SCSI adaptors 542 needs servicing.

An additional parity FIFO 554 is also provided in the SP 114a, for message passing. Again referring to the Appendix, the parity FIFO 554 is programmed with

the following bit settings in the Data Transfer Configuration Register:

Bit	Definition	Setting
0	WD Mode	(0)
1	Parity Chip	(1)
2	Parity Correct Mode	(0)
3	8/16 bits CPU & PortA interface	(1)
4	Invert Port A address 0	(1)
5	Invert Port A address 1	(1)
6	Checksum Carry Wrap	(0)
7	Reset	(0)

The Data Transfer Control Register is programmed as follows:

Bit	Definition	Setting
0	Enable PortA Req/Ack	(0)
1	Enable PortB Req/Ack	(1)
2	Data Transfer Direction	as desired
3	CPU parity enable	(0)
4	PortA parity enable	(0)
5	PortB parity enable	(1)
6	Checksum Enable	(0)
7	PortA Master	(0)

In addition, bit 4 of the RAM Access Control Register (Long Burst) is programmed for 8-byte bursts.

Port A of FIFO 554 is connected to the 16-bit control bus 516, and port B is connected to the common data bus 550. FIFO 554 provides one means by which the microprocessor 510 can communicate directly with the VME bus 120, as is described in more detail below.

The microprocessor 510 manages data movement using a set of 15 channels, each of which has an unique status which indicates its current state. Channels are implemented using a channel enable register 560 and a channel status register 562, both connected to the control bus 516. The channel enable register 560

is a 16-bit write-only register, whereas the channel status register 562 is a 16-bit read-only register. The two registers reside at the same address to microprocessor 510. The microprocessor 510 enables a particular channel by setting its respective bit in channel enable register 560, and recognizes completion of the specified operation by testing for a "done" bit in the channel status register 562. The microprocessor 510 then resets the enable bit, which causes the respective "done" bit in the channel status register 562 to be cleared.

The channels are defined as follows:

CHANNEL	FUNCTION
0:9	These channels control data movement to and from the respective FIFOs 544 via the common data bus 550. When a FIFO is enabled and a request is received from it, the channel becomes ready. Once the channel has been serviced a status of done is generated.
11:10	These channels control data movement between a local data buffer 564, described below, and the VME bus 120. When enabled the channel becomes ready. Once the channel has been serviced a status of done is generated.
12	When enabled, this channel causes the DRAM in local data buffer 564 to be refreshed based on a clock which is generated by the MFP 524. The refresh consists of a burst of 16 rows. This channel does not generate a status of done.
13	The microprocessor's communication FIFO 554 is serviced by this channel. When enable is set and the FIFO 554 asserts a request then the channel becomes ready. This channel generates a status of done.
14	Low latency writes from microprocessor 510 onto the VME bus 120 are controlled by this channel. When this channel is enabled data is moved from a special 32 bit register, described below, onto the VME bus 120. This channel generates a done status.

15 This is a null channel for which neither a ready status nor done status is generated.

Channels are prioritized to allow servicing of the more critical requests first. Channel priority is assigned in a descending order starting at channel 14. That is, in the event that all channels are requesting service, channel 14 will be the first one served.

The common data bus 550 is coupled via a bidirectional register 570 to a 36-bit junction bus 572. A second bidirectional register 574 connects the junction bus 572 with the local data bus 532. Local data buffer 564, which comprises 1MB of DRAM, with parity, is coupled bidirectionally to the junction bus 572. It is organized to provide 256K 32-bit words with byte parity. The SP 114a operates the DRAMs in page mode to support a very high data rate, which requires bursting of data instead of random single-word accesses. It will be seen that the local data buffer 564 is used to implement a RAID (redundant array of inexpensive disks) algorithm, and is not used for direct reading and writing between the VME bus 120 and a peripheral on one of the SCSI buses 540.

A read-only register 576, containing all zeros, is also connected to the junction bus 572. This register is used mostly for diagnostics, initialization, and clearing of large blocks of data in system memory 116.

The movement of data between the FIFOs 544 and 554, the local data buffer 564, and a remote entity such as the system memory 116 on the VME bus 120, is all controlled by a VME/FIFO DMA controller 580. The VME/FIFO DMA controller 580 is similar to the VME/FIFO DMA controller 272 on network controller 110a (Fig. 3), and is described in the Appendix. Briefly, it includes a bit slice engine 582 and a dual-port static RAM 584. One port of the dual-port static RAM 584 communicates over the 32-bit microprocessor data bus

512 with microprocessor 510, and the other port communicates over a separate 16-bit bus with the bit slice engine 582. The microprocessor 510 places command parameters in the dual-port RAM 584, and uses the channel enables 560 to signal the VME/FIFO DMA controller 580 to proceed with the command. The VME/FIFO DMA controller is responsible for scanning the channel status and servicing requests, and returning ending status in the dual-port RAM 584. The dual-port RAM 584 is organized as 1K x 32 bits at the 32-bit port and as 2K x 16 bits at the 16-bit port. An example showing the method by which the microprocessor 510 controls the VME/FIFO DMA controller 580 is as follows. First, the microprocessor 510 writes into the dual-port RAM 584 the desired command and associated parameters for the desired channel. For example, the command might be, "copy a block of data from FIFO 544h out into a block of system memory 116 beginning at a specified VME address." Second, the microprocessor sets the channel enable bit in channel enable register 560 for the desired channel.

At the time the channel enable bit is set, the appropriate FIFO may not yet be ready to send data. Only when the VME/FIFO DMA controller 580 does receive a "ready" status from the channel, will the controller 580 execute the command. In the meantime, the DMA controller 580 is free to execute commands and move data to or from other channels.

When the DMA controller 580 does receive a status of "ready" from the specified channel, the controller fetches the channel command and parameters from the dual-ported RAM 584 and executes. When the command is complete, for example all the requested data has been copied, the DMA controller writes status back into the dual-port RAM 584 and asserts "done" for the channel in channel status register 562. The microprocessor

510 is then interrupted, at which time it reads channel status register 562 to determine which channel interrupted. The microprocessor 510 then clears the channel enable for the appropriate channel and checks the ending channel status in the dual-port RAM 584.

In this way a high-speed data transfer can take place under the control of DMA controller 580, fully in parallel with other activities being performed by microprocessor 510. The data transfer takes place over busses different from microprocessor data bus 512, thereby avoiding any interference with microprocessor instruction fetches.

The SP 114a also includes a high-speed register 590, which is coupled between the microprocessor data bus 512 and the local data bus 532. The high-speed register 590 is used to write a single 32-bit word to an VME bus target with a minimum of overhead. The register is write only as viewed from the microprocessor 510. In order to write a word onto the VME bus 120, the microprocessor 510 first writes the word into the register 590, and the desired VME target address into dual-port RAM 584. When the microprocessor 510 enables the appropriate channel in channel enable register 560, the DMA controller 580 transfers the data from the register 590 into the VME bus address specified in the dual-port RAM 584. The DMA controller 580 then writes the ending status to the dual-port RAM and sets the channel "done" bit in channel status register 562.

This procedure is very efficient for transfer of a single word of data, but becomes inefficient for large blocks of data. Transfers of greater than one word of data, typically for message passing, are usually performed using the FIFO 554.

The SP 114a also includes a series of registers 592, similar to the registers 282 on NC 110a (Fig. 3)

and the registers 382 on FC 112a (Fig. 4). The details of these registers are not important for an understanding of the present invention.

STORAGE PROCESSOR OPERATION

The 30 SCSI disk drives supported by each of the SPs 114 are visible to a client processor, for example one of the file controllers 112, either as three large, logical disks or as 30 independent SCSI drives, depending on configuration. When the drives are visible as three logical disks, the SP uses RAID 5 design algorithms to distribute data for each logical drive on nine physical drives to minimize disk arm contention. The tenth drive is left as a spare. The RAID 5 algorithm (redundant array of inexpensive drives, revision 5) is described in "A Case For a Redundant Arrays of Inexpensive Disks (RAID)", by Patterson et al., published at ACM SIGMOD Conference, Chicago, Ill., June 1-3, 1988, incorporated herein by reference.

In the RAID 5 design, disk data are divided into stripes. Data stripes are recorded sequentially on eight different disk drives. A ninth parity stripe, the exclusive-or of eight data stripes, is recorded on a ninth drive. If a stripe size is set to 8K bytes, a read of 8K of data involves only one drive. A write of 8K of data involves two drives: a data drive and a parity drive. Since a write requires the reading back of old data to generate a new parity stripe, writes are also referred to as modify writes. The SP 114a supports nine small reads to nine SCSI drives concurrently. When stripe size is set to 8K, a read of 64K of data starts all eight SCSI drives, with each drive reading one 8K stripe worth of data. The parallel operation is transparent to the caller client.

The parity stripes are rotated among the nine drives in order to avoid drive contention during write operations. The parity stripe is used to improve availability of data. When one drive is down, the SP 114a can reconstruct the missing data from a parity stripe. In such case, the SP 114a is running in error recovery mode. When a bad drive is repaired, the SP 114a can be instructed to restore data on the repaired drive while the system is on-line.

When the SP 114a is used to attach thirty independent SCSI drives, no parity stripe is created and the client addresses each drive directly.

The SP 114a processes multiple messages (transactions, commands) at one time, up to 200 messages per second. The SP 114a does not initiate any messages after initial system configuration. The following SP 114a operations are defined:

01 No Op
02 Send Configuration Data
03 Receive Configuration Data
05 Read and Write Sectors
06 Read and Write Cache Pages
07 IOCTL Operation
08 Dump SP 114a Local Data Buffer
09 Start/Stop A SCSI Drive
0C Inquiry
0E Read Message Log Buffer
0F Set SP 114a Interrupt

The above transactions are described in detail in the above-identified application entitled MULTIPLE FACILITY OPERATING SYSTEM ARCHITECTURE. For and understanding of the invention, it will be useful to describe the function and operation of only two of these commands: read and write sectors, and read and write cache pages.

Read and Write Sectors

This command, issued usually by an FC 112, causes the SP 114a to transfer data between a specified block of system memory and a specified series of contiguous sectors on the SCSI disks. As previously described in connection with the file controller 112, the particular sectors are identified in physical terms. In particular, the particular disk sectors are identified by SCSI channel number (0-9), SCSI ID on that channel number (0-2), starting sector address on the specified drive, and a count of the number of sectors to read or write. The SCSI channel number is zero if the SP 114a is operating under RAID 5.

The SP 114a can execute up to 30 messages on the 30 SCSI drives simultaneously. Unlike most of the commands to an SP 114, which are processed by microprocessor 510 as soon as they appear on the command FIFO 534, read and write sectors commands (as well as read and write cache memory commands) are first sorted and queued. Hence, they are not served in the order of arrival.

When a disk access command arrives, the microprocessor 510 determines which disk drive is targeted and inserts the message in a queue for that disk drive sorted by the target sector address. The microprocessor 510 executes commands on all the queues simultaneously, in the order present in the queue for each disk drive. In order to minimize disk arm movements, the microprocessor 510 moves back and forth among queue entries in an elevator fashion.

If no error conditions are detected from the SCSI disk drives, the command is completed normally. When a data check error condition occurs and the SP 114a is configured for RAID 5, recovery actions using redundant data begin automatically. When a drive is down while the SP 114a is configured for RAID 5,

recovery actions similar to data check recovery take place.

Read/Write Cache Pages

This command is similar to read and write sectors, except that multiple VME addresses are provided for transferring disk data to and from system memory 116. Each VME address points to a cache page in system memory 116, the size of which is also specified in the command. When transferring data from a disk to system memory 116, data are scattered to different cache pages; when writing data to a disk, data are gathered from different cache pages in system memory 116. Hence, this operation is referred to as a scatter-gather function.

The target sectors on the SCSI disks are specified in the command in physical terms, in the same manner that they are specified for the read and write sectors command. Termination of the command with or without error conditions is the same as for the read and write sectors command.

The dual-port RAM 584 in the DMA controller 580 maintains a separate set of commands for each channel controlled by the bit slice engine 582. As each channel completes its previous operation, the microprocessor 510 writes a new DMA operation into the dual-port RAM 584 for that channel in order to satisfy the next operation on a disk elevator queue.

The commands written to the DMA controller 580 include an operation code and a code indicating whether the operation is to be performed in non-block mode, in standard VME block mode, or in enhanced block mode. The operation codes supported by DMA controller 580 are as follows:

OP CODE	OPERATION	
0	NO-OP	
1	ZEROES -> BUFFER	Move zeros from zeros register 576 to local data buffer 564.
2	ZEROES -> FIFO	Move zeros from zeros register 576 to the currently selected FIFO on common data bus 550.
3	ZEROES -> VMEbus	Move zeros from zeros register 576 out onto the VME bus 120. Used for initializing cache buffers in system memory 116.
4	VMEbus -> BUFFER	Move data from the VME bus 120 to the local data buffer 564. This operation is used during a write, to move target data intended for a down drive into the buffer for participation in redundancy generation. Used only for RAID 5 application.
5	VMEbus -> FIFO	New data to be written from VME bus onto a drive. Since RAID 5 requires redundancy data to be generated from data that is buffered in local data buffer 564, this operation will be used only if the SP 114a is not configured for RAID 5.
6	VMEbus -> BUFFER & FIFO	Target data is moved from VME bus 120 to a SCSI

			device and is also captured in the local data buffer 564 for participation in redundancy generation. Used only if SP 114a is configured for RAID 5 operation.
	7	BUFFER -> VMEbus	This operation is not used.
	8	BUFFER -> FIFO	Participating data is transferred to create redundant data or recovered data on a disk drive. Used only in RAID 5 applications.
	9	FIFO -> VMEbus	This operation is used to move target data directly from a disk drive onto the VME bus 120.
	A	FIFO -> BUFFER	Used to move participating data for recovery and modify operations. Used only in RAID 5 applications.
	B	FIFO -> VMEbus & BUFFER	This operation is used to save target data for participation in data recovery. Used only in RAID 5 applications.

SYSTEM MEMORY

Fig. 6 provides a simplified block diagram of the preferred architecture of one of the system memory cards 116a. Each of the other system memory cards are the same. Each memory card 116 operates as a slave on the enhanced VME bus 120 and therefore requires no on-board CPU. Rather, a timing control block 610 is sufficient to provide the necessary slave control operations. In particular, the timing control block

610, in response to control signals from the control portion of the enhanced VME bus 120, enables a 32-bit wide buffer 612 for an appropriate direction transfer of 32-bit data between the enhanced VME bus 120 and a multiplexer unit 614. The multiplexer 614 provides a multiplexing and demultiplexing function, depending on data transfer direction, for a six megabit by seventy-two bit word memory array 620. An error correction code (ECC) generation and testing unit 622 is also connected to the multiplexer 614 to generate or verify, again depending on transfer direction, eight bits of ECC data. The status of ECC verification is provided back to the timing control block 610.

ENHANCED VME BUS PROTOCOL

VME bus 120 is physically the same as an ordinary VME bus, but each of the NCs and SPs include additional circuitry and firmware for transmitting data using an enhanced VME block transfer protocol. The enhanced protocol is described in detail in the above-identified application entitled ENHANCED VMEBUS PROTOCOL UTILIZING PSEUDOSYNCHRONOUS HANDSHAKING AND BLOCK MODE DATA TRANSFER, and summarized in the Appendix hereto. Typically transfers of LNFS file data between NCs and system memory, or between SPs and system memory, and transfers of packets being routed from one NC to another through system memory, are the only types of transfers that use the enhanced protocol in server 100. All other data transfers on VME bus 120 use either conventional VME block transfer protocols or ordinary non-block transfer protocols.

MESSAGE PASSING

As is evident from the above description, the different processors in the server 100 communicate with each other via certain types of messages. In

software, these messages are all handled by the messaging kernel, described in detail in the MULTIPLE FACILITY OPERATING SYSTEM ARCHITECTURE application cited above. In hardware, they are implemented as follows.

Each of the NCs 110, each of the FCs 112, and each of the SPs 114 includes a command or communication FIFO such as 290 on NC 110a. The host 118 also includes a command FIFO, but since the host is an unmodified purchased processor board, the FIFO is emulated in software. The write port of the command FIFO in each of the processors is directly addressable from any of the other processors over VME bus 120.

Similarly, each of the processors except SPs 114 also includes shared memory such as CPU memory 214 on NC 110a. This shared memory is also directly addressable by any of the other processors in the server 100.

If one processor, for example network controller 110a, is to send a message or command to a second processor, for example file controller 112a, then it does so as follows. First, it forms the message in its own shared memory (e.g., in CPU memory 214 on NC 110a). Second, the microprocessor in the sending processor directly writes a message descriptor into the command FIFO in the receiving processor. For a command being sent from network controller 110a to file controller 112a, the microprocessor 210 would perform the write via buffer 284 on NC 110a, VME bus 120, and buffer 384 on file controller 112a.

The command descriptor is a single 32-bit word containing in its high order 30 bits a VME address indicating the start of a quad-aligned message in the sender's shared memory. The low order two bits indicate the message type as follows:

Type	Description
0	Pointer to a new message being sent
1	Pointer to a reply message
2	Pointer to message to be forwarded
3	Pointer to message to be freed; also message acknowledgment

All messages are 128-bytes long.

When the receiving processor reaches the command descriptor on its command FIFO, it directly accesses the sender's shared memory and copies it into the receiver's own local memory. For a command issued from network controller 110a to file controller 112a, this would be an ordinary VME block or non-block mode transfer from NC CPU memory 214, via buffer 284, VME bus 120 and buffer 384, into FC CPU memory 314. The FC microprocessor 310 directly accesses NC CPU memory 214 for this purpose over the VME bus 120.

When the receiving processor has received the command and has completed its work, it sends a reply message back to the sending processor. The reply message may be no more than the original command message unaltered, or it may be a modified version of that message or a completely new message. If the reply message is not identical to the original command message, then the receiving processor directly accesses the original sender's shared memory to modify the original command message or overwrite it completely. For replies from the FC 112a to the NC 110a, this involves an ordinary VME block or non-block mode transfer from the FC 112a, via buffer 384, VME bus 120, buffer 284 and into NC CPU memory 214. Again, the FC microprocessor 310 directly accesses NC CPU memory 214 for this purpose over the VME bus 120.

Whether or not the original command message has been changed, the receiving processor then writes a reply message descriptor directly into the original sender's command FIFO. The reply message descriptor

contains the same VME address as the original command message descriptor, and the low order two bits of the word are modified to indicate that this is a reply message. For replies from the FC 112a to the NC 110a, the message descriptor write is accomplished by microprocessor 310 directly accessing command FIFO 290 via buffer 384, VME bus 120 and buffer 280 on the NC. Once this is done, the receiving processor can free the buffer in its local memory containing the copy of the command message.

When the original sending processor reaches the reply message descriptor on its command FIFO, it wakes up the process that originally sent the message and permits it to continue. After examining the reply message, the original sending processor can free the original command message buffer in its own local shared memory.

As mentioned above, network controller 110a uses the buffer 284 data path in order to write message descriptors onto the VME bus 120, and uses VME/FIFO DMA controller 272 together with parity FIFO 270 in order to copy messages from the VME bus 120 into CPU memory 214. Other processors read from CPU memory 214 using the buffer 284 data path.

File controller 112a writes message descriptors onto the VME bus 120 using the buffer 384 data path, and copies messages from other processors' shared memory via the same data path. Both take place under the control of microprocessor 310. Other processors copy messages from CPU memory 314 also via the buffer 384 data path.

Storage processor 114a writes message descriptors onto the VME bus using high-speed register 590 in the manner described above, and copies messages from other processors using DMA controller 580 and FIFO 554. The SP 114a has no shared memory, however, so it uses a

buffer in system memory 116 to emulate that function. That is, before it writes a message descriptor into another processor's command FIFO, the SP 114a first copies the message into its own previously allocated buffer in system memory 116 using DMA controller 580 and FIFO 554. The VME address included in the message descriptor then reflects the VME address of the message in system memory 116.

In the host 118, the command FIFO and shared memory are both emulated in software.

The invention has been described with respect to particular embodiments thereof, and it will be understood that numerous modifications and variations are possible within the scope of the invention.

APPENDIX A

VME/FIFO DMA Controller

In storage processor 114a, DMA controller 580 manages the data path under the direction of the microprocessor 510. The DMA controller 580 is a microcoded 16-bit bit-slice implementation executing pipelined instructions at a rate of one each 62.5ns. It is responsible for scanning the channel status 562 and servicing request with parameters stored in the dual-ported ram 584 by the microprocessor 510. Ending status is returned in the ram 584 and interrupts are generated for the microprocessor 510.

Control Store. The control store contains the microcoded instructions which control the DMA controller 580. The control store consists of 6 1K x 8 proms configured to yield a 1K x 48 bit microword. Locations within the control store are addressed by the sequencer and data is presented at the input of the pipeline registers.

Sequencer. The sequencer controls program flow by generating control store addresses based upon pipeline data and various status bits. The control store address consists of 10 bits. Bits 8:0 of the control store address derive from a multiplexer having as its inputs either an ALU output or the output of an incrementer. The incrementer can be preloaded with pipeline register bits 8:0, or it can be incremented as a result of a test condition. The 1K address range is divided into two pages by a latched flag such that the microprogram can execute from either page. Branches, however remain within the selected page. Conditional sequencing is performed by having the test condition increment the pipeline provided address. A false condition allows execution from the pipeline address while a true condition causes execution from

the address + 1. The alu output is selected as an address source in order to directly vector to a routine or in order to return to a calling routine. Note that when calling a subroutine the calling routine must reside within the same page as the subroutine or the wrong page will be selected on the return.

ALU. The alu comprises a single IDT49C402A integrated circuit. It is 16 bits in width and most closely resembles four 2901s with 64 registers. The alu is used primarily for incrementing, decrementing, addition and bit manipulation. All necessary control signals originate in the control store. The IDT HIGH PERFORMANCE CMOS 1988 DATA BOOK, incorporated by reference herein, contains additional information about the alu.

Microword. The 48 bit microword comprises several fields which control various functions of the DMA controller 580. The format of the microword is defined below along with mnemonics and a description of each function.

AI<8:0>	47:39	(Alu Instruction bits 8:0) The AI bits provide the instruction for the 49C402A alu. Refer to the IDT data book for a complete definition of the alu instructions. Note that the I9 signal input of the 49C402A is always low.
CIN	38	(Carry INput) This bit forces the carry input to the alu.
RA<5:0>	37:32	(Register A address bits 5:0) These bits select one of 64 registers as the "A" operand for the alu. These bits also provide literal bits 15:10 for the alu bus.
RB<5:0>	31:26	(Register B address bits 5:0) These bits select one of 64 registers as the "B" operand for the alu. These bits also provide literal bits 9:4 for the alu bus.

LFD 25 (Latched Flag Data) When set this bit causes the selected latched flag to be set. When reset this bit causes the selected latched flag to be cleared. This bits also functions as literal bit 3 for the alu bus.

LFS<2:0> 24:22 (Latched Flag Select bits 2:0) The meaning of these bits is dependent upon the selected source for the alu bus. In the event that the literal field is selected as the bus source then LFS<2:0> function as literal bits <2:0> otherwise the bits are used to select one of the latched flags.

LFS<2:0>	SELECTED FLAG
0	This value selects a null flag.
1	When set this bit enables the buffer clock. When reset this bit disables the buffer clock.
2	When this bit is cleared VME bus transfers, buffer operations and RAS are all disabled.
3	NOT USED
4	When set this bit enables VME bus transfers.
5	When set this bit enables buffer operations.
6	When set this bit asserts the row address strobe to the dram buffer.
7	When set this bit selects page 0 of the control store.

SRC<1,0> 20,21 (alu bus SouRCe select bits 1,0) These bits select the data source to be enabled onto the alu bus.

SRC<1.0>	Selected Source
0	alu
1	dual ported ram
2	literal
3	reserved-not defined

PF<2:0> 19:17 (Pulsed Flag select bits 2:0) These bits select a flag/signal to be pulsed.

PF<2:0>	Flag
0	null
1	SGL_CLK generates a single transition of buffer clock.
2	SET_VB forces vme and buffer enable to be set.
3	CL_PERR clears buffer parity error status.
4	SET_DN set channel done status for the currently selected channel.
5	INC_ADR increment dual ported ram address.
6:7	RESERVED - NOT DEFINED

DEST<3:0> 16:13 (DESTination select bits 3:0) These bits select one of 10 destinations to be loaded from the alu bus.

DEST<3:0>	Destination
0	null
1	WR_RAM causes the data on the alu bus to be written to the dual ported ram. D<15:0> -> ram<15:0>
2	WR_BADD

loads the data from the alu bus into the dram address counters.

D<14:7> -> mux addr<8:0>

3 WR_VADL
loads the data from the alu bus into the least significant 2 bytes of the VME address register.
D<15:2> -> VME addr<15:2>
D1 -> ENB_tional registers
D<15:2> -> VME addr<15:2>
D1 -> ENB_ENH
D0 -> ENB_BLK

4 WR_VADH
loads the most significant 2 bytes of the VME address register.
D<15:0> -> VME addr<31:16>

5 WR_RADD
loads the dual ported ram address counters.
D<10:0> -> ram addr <10:0>

6 WR_WCNT
loads the word counters.
D15 -> count enable*
D<14:8> -> count <6:0>

7 WR_CO
loads the co-channel select register.
D<7:4> -> CO<3:0>

8 WR_NXT
loads the next-channel select register.
D<3:0> -> NEXT<3:0>

9 WR_CUR
loads the current-channel select register.
D<3:0> -> CURR <3:0>

10:14 RESERVED - NOT DEFINED

15 JUMP
causes the control store sequencer to select the alu data bus.
D<8:0> -> CS_A<8:0>

SUBSTITUTE SHEET

TEST<3:0> 12:9 (TEST condition select bits 3:0) Select one of 16 inputs to the test multiplexor to be used as the carry input to the incrementer.

TEST<3:0>	Condition	
0	FALSE	-always false
1	TRUE	-always true
2	ALU_COUT	-carry output of alu
3	ALU_EQ	-equals output of alu
4	ALU_OVR	-alu overflow
5	ALU_NEG	-alu negative
6	XFR_DONE	-transfer complete
7	PAR_ERR	-buffer parity error
8	TIMOUT	-bus operation timeout
9	ANY_ERR	-any error status
14:10	RESERVED	-NOT DEFINED
15	CH_RDY	-next channel ready

NEXT_A<8:0> 8:0 (NEXT Address bits 8:0) Selects an instructions from the current page of the control store for execution.

Dual Ported Ram. The dual ported ram is the medium by which command, parameters and status are communicated between the DMA controller 580 and the microprocessor 510. The ram is organized as 1K x 32 at the master port and as 2K x 16 at the DMA port. The ram may be both written and read at either port.

The ram is addressed by the DMA controller 580 by loading an 11 bit address into the address counters. Data is then read into bidirectional registers and the address counter is incremented to allow read of the next location.

Writing the ram is accomplished by loading data from the processor into the registers after loading the ram address. Successive writes may be performed on every other processor cycle.

The ram contains current block pointers, ending status, high speed bus address and parameter blocks. The following is the format of the ram:

OFFSET	31	0
0	CURR POINTER 0	STATUS 0
4	INITIAL POINTER 0	
.	.	
.	.	
58	CURR POINTER B	STATUS B
5C	INITIAL POINTER B	
60	not used	not used
64	not used	not used
68	CURR POINTER D	STATUS D
6C	INITIAL POINTER D	
70	not used	STATUS E
74	HIGH SPEED BUS ADDRESS 31:2	0 0
78	PARAMETER BLOCK 0	
.	.	
.	.	
??	PARAMETER BLOCK n	

The Initial Pointer is a 32 bit value which points the first command block of a chain. The current pointer is a sixteen bit value used by the DMA controller 580 to point to the current command block. The current command block pointer should be initialized to 0x0000 by the microprocessor 510 before enabling the channel. Upon detecting a value of 0x0000

in the current block pointer the DMA controller 580 will copy the lower 16 bits from the initial pointer to the current pointer. Once the DMA controller 580 has completed the specified operations for the parameter block the current pointer will be updated to point to the next block. In the event that no further parameter blocks are available the pointer will be set to 0x0000.

The status byte indicates the ending status for the last channel operation performed. The following status bytes are defined:

STATUS	MEANING
0	NO ERRORS
1	ILLEGAL OP CODE
2	BUS OPERATION TIMEOUT
3	BUS OPERATION ERROR
4	DATA PATH PARITY ERROR

The format of the parameter block is:

OFFSET	31	0
0	FORWARD LINK	
4	NOT USED	WORD COUNT
8	VME ADDRESS 31:2, ENH, BLK	
C	TERM 0 | OP 0	BUF ADDR 0
	.	
	.	
	.	
C+(4Xn)	TERM n | OP n	BUF ADDR n

FORWARD LINK - The forward link points to the first word of the next parameter block for execution. It allows several parameter blocks to be initialized and chained to create a sequence of operations for execution. The forward pointer has the following format:

A31:A2,0,0

The format dictates that the parameter block must start on a quad byte boundary. A pointer of 0x00000000 is a special case which indicates no forward link exists.

WORD COUNT - The word count specifies the number of quad byte words that are to be transferred to or from each buffer address or to/from the VME address. A word count of 64K words may be specified by initializing the word count with the value of 0. The word count has the following format:

|D15|D14|D13|D12|D11|D10|D9|D8|D7|D6|D5|D4|D3|D2|D1|D0|

The word count is updated by the DMA controller 580 at the completion of a transfer to/from the last specified buffer address. Word count is not updated after transferring to/from each buffer address and is therefore not an accurate indicator of the total data moved to/from the buffer. Word count represents the amount of data transferred to the VME bus or one of the FIFOs 544 or 554.

VME ADDRESS - The VME address specifies the starting address for data transfers. Thirty bits allows the address to start at any quad byte boundary.

ENH - This bit when set selects the enhanced block transfer protocol described in the above-cited ENHANCED VMEBUS PROTOCOL UTILIZING PSEUDOSYNCHRONOUS HANDSHAKING AND BLOCK MODE DATA TRANSFER application, to be used during the VME bus transfer. Enhanced protocol will be disabled automatically when performing any transfer to or from 24 bit or 16 bit address space, when the starting address is not 8 byte aligned or when the word count is not even.

BLK - This bit when set selects the conventional VME block mode protocol to be used during the VME bus transfer. Block mode will be disabled automatically

when performing any transfer to or from 16 bit address space.

BUF ADDR - The buffer address specifies the starting buffer address for the adjacent operation. Only 16 bits are available for a 1M byte buffer and as a result the starting address always falls on a 16 byte boundary. The programmer must ensure that the starting address is on a modulo 128 byte boundary. The buffer address is updated by the DMA controller 580 after completion of each data burst.

|A19|A18|A17|A16|A15|A14|A13|A12|A11|A10|A9|A8|A7|A6|A5|A4|

TERM - The last buffer address and operation within a parameter block is identified by the terminal bit. The DMA controller 580 continues to fetch buffer addresses and operations to perform until this bit is encountered. Once the last operation within the parameter block is executed the word counter is updated and if not equal to zero the series of operations is repeated. Once the word counter reaches zero the forward link pointer is used to access the next parameter block.

|0|0|0|0|0|0|0|0|T|

OP - Operations are specified by the op code. The op code byte has the following format:

|0|0|0|0|OP3|OP2|OP1|OP0|

The op codes are listed below ("FIFO" refers to any of the FIFOs 544 or 554):

2066443

OP CODE	OPERATION
0	NO-OP
1	ZEROES -> BUFFER
2	ZEROES -> FIFO
3	ZEROES -> VMEbus
4	VMEbus -> BUFFER
5	VMEbus -> FIFO
6	VMEbus -> BUFFER & FIFO
7	BUFFER -> VMEbus
8	BUFFER -> FIFO
9	FIFO -> VMEbus
A	FIFO -> BUFFER
B	FIFO -> VMEbus & BUFFER
C	RESERVED
D	RESERVED
E	RESERVED
F	RESERVED

APPENDIX B

Enhanced VME Block Transfer Protocol

The enhanced VME block transfer protocol is a VMEbus compatible pseudo-synchronous fast transfer handshake protocol for use on a VME backplane bus having a master functional module and a slave functional module logically interconnected by a data transfer bus. The data transfer bus includes a data strobe signal line and a data transfer acknowledge signal line. To accomplish the handshake, the master transmits a data strobe signal of a given duration on the data strobe line. The master then awaits the reception of a data transfer acknowledge signal from the slave module on the data transfer acknowledge signal line. The slave then responds by transmitting data transfer acknowledge signal of a given duration on the data transfer acknowledge signal line.

Consistent with the pseudo-synchronous nature of the handshake protocol, the data to be transferred is referenced to only one signal depending upon whether the transfer operation is a READ or WRITE operation.

In transferring data from the master functional unit to the slave, the master broadcasts the data to be transferred. The master asserts a data strobe signal and the slave, in response to the data strobe signal, captures the data broadcast by the master. Similarly, in transferring data from the slave to the master, the slave broadcasts the data to be transferred to the master unit. The slave then asserts a data transfer acknowledge signal and the master, in response to the data transfer acknowledge signal, captures the data broadcast by the slave.

The fast transfer protocol, while not essential to the present invention, facilitates the rapid transfer of large amounts of data across a VME backplane bus by substantially increasing the data transfer rate.

These data rates are achieved by using a handshake wherein the data strobe and data transfer acknowledge signals are functionally decoupled and by specifying high current drivers for all data and control lines.

The enhanced pseudo-synchronous method of data transfer (hereinafter referred to as "fast transfer mode") is implemented so as to comply and be compatible with the IEEE VME backplane bus standard. The protocol utilizes user-defined address modifiers, defined in the VMEbus standard, to indicate use of the fast transfer mode. Conventional VMEbus functional units, capable only of implementing standard VMEbus protocols, will ignore transfers made using the fast transfer mode and, as a result, are fully compatible with functional units capable of implementing the fast transfer mode.

The fast transfer mode reduces the number of bus propagations required to accomplish a handshake from four propagations, as required under conventional VMEbus protocols, to only two bus propagations. Likewise, the number of bus propagations required to effect a BLOCK READ or BLOCK WRITE data transfer is reduced. Consequently, by reducing the propagations across the VMEbus to accomplish handshaking and data transfer functions, the transfer rate is materially increased.

The enhanced protocol is described in detail in the above-cited ENHANCED VMEBUS PROTOCOL application, and will only be summarized here. Familiarity with the conventional VME bus standards is assumed.

In the fast transfer mode handshake protocol, only two bus propagations are used to accomplish a handshake, rather than four as required by the conventional protocol. At the initiation of a data transfer cycle, the master will assert and deassert DS0* in the form of a pulse of a given duration. The

deassertion of DS0* is accomplished without regard as to whether a response has been received from the slave. The master then waits for an acknowledgement from the slave. Subsequent pulsing of DS0* cannot occur until a responsive DTACK* signal is received from the slave. Upon receiving the slave's assertion of DTACK*, the master can then immediately reassert data strobe, if so desired. The fast transfer mode protocol does not require the master to wait for the deassertion of DTACK* by the slave as a condition precedent to subsequent assertions of DS0*. In the fast transfer mode, only the leading edge (i.e., the assertion) of a signal is significant. Thus, the deassertion of either DS0* or DTACK* is completely irrelevant for completion of a handshake. The fast transfer protocol does not employ the DS1* line for data strobe purposes at all.

The fast transfer mode protocol may be characterized as pseudo-synchronous as it includes both synchronous and asynchronous aspects. The fast transfer mode protocol is synchronous in character due to the fact that DS0* is asserted and deasserted without regard to a response from the slave. The asynchronous aspect of the fast transfer mode protocol is attributable to the fact that the master may not subsequently assert DS0* until a response to the prior strobe is received from the slave. Consequently, because the protocol includes both synchronous and asynchronous components, it is most accurately classified as "pseudo-synchronous."

The transfer of data during a BLOCK WRITE cycle in the fast transfer protocol is referenced only to DS0*. The master first broadcasts valid data to the slave, and then asserts DS0 to the slave. The slave is given a predetermined period of time after the assertion of DS0* in which to capture the data. Hence, slave

modules must be prepared to capture data at any time, as DTACK* is not referenced during the transfer cycle.

Similarly, the transfer of data during a BLOCK READ cycle in the fast transfer protocol is referenced only to DTACK*. The master first asserts DS0*. The slave then broadcasts data to the master and then asserts DTACK*. The master is given a predetermined period of time after the assertion of DTACK in which to capture the data. Hence, master modules must be prepared to capture data at any time as DS0 is not referenced during the transfer cycle.

Fig. 7, parts A through C, is a flowchart illustrating the operations involved in accomplishing the fast transfer protocol BLOCK WRITE cycle. To initiate a BLOCK WRITE cycle, the master broadcasts the memory address of the data to be transferred and the address modifier across the DTB bus. The master also drives interrupt acknowledge signal (IACK*) high and the LWORD* signal low 701. A special address modifier, for example "1F," broadcast by the master indicates to the slave module that the fast transfer protocol will be used to accomplish the BLOCK WRITE.

The starting memory address of the data to be transferred should reside on a 64-bit boundary and the size of block of data to be transferred should be a multiple of 64 bits. In order to remain in compliance with the VMEbus standard, the block must not cross a 256 byte boundary without performing a new address cycle.

The slave modules connected to the DTB receive the address and the address modifier broadcast by the master across the bus and receive LWORD* low and IACK* high 703. Shortly after broadcasting the address and address modifier 701, the master drives the AS* signal low 705. The slave modules receive the AS* low signal 707. Each slave individually determines whether it

will participate in the data transfer by determining whether the broadcasted address is valid for the slave in question 709. If the address is not valid, the data transfer does not involve that particular slave and it ignores the remainder of the data transfer cycle.

The master drives WRITE* low to indicate that the transfer cycle about to occur is a WRITE operation 711. The slave receives the WRITE* low signal 713 and, knowing that the data transfer operation is a WRITE operation, awaits receipt of a high to low transition on the DS0* signal line 715. The master will wait until both DTACK* and BERR* are high 718, which indicates that the previous slave is no longer driving the DTB.

The master proceeds to place the first segment of the data to be transferred on data lines D00 through D31, 719. After placing data on D00 through D31, the master drives DS0* low 721 and, after a predetermined interval, drives DS0* high 723.

In response to the transition of DS0* from high to low, respectively 721 and 723, the slave latches the data being transmitted by the master over data lines D00 through D31, 725. The master places the next segment of the data to be transferred on data lines D00 through D31, 727, and awaits receipt of a DTACK* signal in the form of a high to low transition signal, 729 in Fig. 7B.

Referring to Fig. 7B, the slave then drives DTACK* low, 731, and, after a predetermined period of time, drives DTACK high, 733. The data latched by the slave, 725, is written to a device, which has been selected to store the data 735. The slave also increments the device address 735. The slave then waits for another transition of DS0* from high to low 737.

To commence the transfer of the next segment of the block of data to be transferred, the master drives DS0* low 739 and, after a predetermined period of time, drives DS0* high 741. In response to the transition of DS0* from high to low, respectively 739 and 741, the slave latches the data being broadcast by the master over data lines D00 through D31, 743. The master places the next segment of the data to be transferred on data lines D00 through D31, 745, and awaits receipt of a DTACK* signal in the form of a high to low transition, 747.

The slave then drives DTACK* low, 749, and, after a predetermined period of time, drives DTACK* high, 751. The data latched by the slave, 743, is written to the device selected to store the data and the device address is incremented 753. The slave waits for another transition of DS0* from high to low 737.

The transfer of data will continue in the above-described manner until all of the data has been transferred from the master to the slave. After all of the data has been transferred, the master will release the address lines, address modifier lines, data lines, IACK* line, LWORD* line and DS0* line, 755. The master will then wait for receipt of a DTACK* high to low transition 757. The slave will drive DTACK* low, 759 and, after a predetermined period of time, drive DTACK* high 761. In response to the receipt of the DTACK* high to low transition, the master will drive AS* high 763 and then release the AS* line 765.

Fig. 8, parts A through C, is a flowchart illustrating the operations involved in accomplishing the fast transfer protocol BLOCK READ cycle. To initiate a BLOCK READ cycle, the master broadcasts the memory address of the data to be transferred and the address modifier across the DTB bus 801. The master

drives the LWORD* signal low and the IACK* signal high 801. As noted previously, a special address modifier indicates to the slave module that the fast transfer protocol will be used to accomplish the BLOCK READ.

The slave modules connected to the DTB receive the address and the address modifier broadcast by the master across the bus and receive LWORD* low and IACK* high 803. Shortly after broadcasting the address and address modifier 801, the master drives the AS* signal low 805. The slave modules receive the AS* low signal 807. Each slave individually determines whether it will participate in the data transfer by determining whether the broadcasted address is valid for the slave in question 809. If the address is not valid, the data transfer does not involve that particular slave and it ignores the remainder of the data transfer cycle.

The master drives WRITE* high to indicate that the transfer cycle about to occur is a READ operation 811. The slave receives the WRITE* high signal 813 and, knowing that the data transfer operation is a READ operation, places the first segment of the data to be transferred on data lines D00 through D31 819. The master will wait until both DTACK* and BERR* are high 818, which indicates that the previous slave is no longer driving the DTB.

The master then drives DS0* low 821 and, after a predetermined interval, drives DS0* high 823. The master then awaits a high to low transition on the DTACK* signal line 824. As shown in Fig. 8B, the slave then drives the DTACK* signal low 825 and, after a predetermined period of time, drives the DTACK* signal high 827.

In response to the transition of DTACK* from high to low, respectively 825 and 827, the master latches the data being transmitted by the slave over data

lines D00 through D31, 831. The data latched by the master, 831, is written to a device, which has been selected to store the data the device address is incremented 833.

The slave places the next segment of the data to be transferred on data lines D00 through D31, 829, and then waits for another transition of DS0* from high to low 837.

To commence the transfer of the next segment of the block of data to be transferred, the master drives DS0* low 839 and, after a predetermined period of time, drives DS0* high 841. The master then waits for the DTACK* line to transition from high to low, 843.

The slave drives DTACK* low, 845, and, after a predetermined period of time, drives DTACK* high, 847. In response to the transition of DTACK* from high to low, respectively 839 and 841, the master latches the data being transmitted by the slave over data lines D00 through D31, 845. The data latched by the master, 845, is written to the device selected to store the data, 851 in Fig. 8C, and the device address is incremented. The slave places the next segment of the data to be transferred on data lines D00 through D31, 849.

The transfer of data will continue in the above-described manner until all of the data to be transferred from the slave to the master has been written into the device selected to store the data. After all of the data to be transferred has been written into the storage device, the master will release the address lines, address modifier lines, data lines, the IACK* line, the LWORD line and DS0* line 852. The master will then wait for receipt of a DTACK* high to low transition 853. The slave will drive DTACK* low 855 and, after a predetermined period of time, drive DTACK* high 857. In response to the

receipt of the DTACK* high to low transition, the master will drive AS* high 859 and release the AS* line 861.

To implement the fast transfer protocol, a conventional 64 mA tri-state driver is substituted for the 48 mA open collector driver conventionally used in VME slave modules to drive DTACK*. Similarly, the conventional VMEbus data drivers are replaced with 64 mA tri-state drivers in SO-type packages. The latter modification reduces the ground lead inductance of the actual driver package itself and, thus, reduces "ground bounce" effects which contribute to skew between data, DS0* and DTACK*. In addition, signal return inductance along the bus backplane is reduced by using a connector system having a greater number of ground pins so as to minimize signal return and mated-pair pin inductance. One such connector system is the "High Density Plus" connector, Model No. 420-8015-000, manufactured by Teradyne Corporation.

APPENDIX C

Parity FIFO

The parity FIFOs 240, 260 and 270 (on the network controllers 110), and 544 and 554 (on storage processors 114) are each implemented as an ASIC. All the parity FIFOs are identical, and are configured on power-up or during normal operation for the particular function desired. The parity FIFO is designed to allow speed matching between buses of different speed, and to perform the parity generation and correction for the parallel SCSI drives.

The FIFO comprises two bidirectional data ports, Port A and Port B, with 36 x 64 bits of RAM buffer between them. Port A is 8 bits wide and Port B is 32 bits wide. The RAM buffer is divided into two parts, each 36 x 32 bits, designated RAM X and RAM Y. The two ports access different halves of the buffer alternating to the other half when available. When the chip is configured as a parallel parity chip (e.g. one of the FIFOs 544 on SP 114a), all accesses on Port B are monitored and parity is accumulated in RAM X and RAM Y alternately.

The chip also has a CPU interface, which may be 8 or 16 bits wide. In 16 bit mode the Port A pins are used as the most significant data bits of the CPU interface and are only actually used when reading or writing to the Fifo Data Register inside the chip.

A REQ, ACK handshake is used for data transfer on both Ports A and B. The chip may be configured as either a master or a slave on Port A in the sense that, in master mode the Port A ACK / RDY output signifies that the chip is ready to transfer data on Port A, and the Port A REQ input specifies that the slave is responding. In slave mode, however, the Port A REQ input specifies that the master requires a data

transfer, and the chip responds with Port A ACK / RDY when data is available. The chip is a master on Port B since it raises Port B REQ and waits for Port B ACK to indicate completion of the data transfer.

SIGNAL DESCRIPTIONS

Port A 0-7, P

Port A is the 8 bit data port. Port A P, if used, is the odd parity bit for this port.

A Req, A Ack/Rdy

These two signals are used in the data transfer mode to control the handshake of data on Port A.

uP Data 0-7, uP Data P, uPAdd 0-2, CS

These signals are used by a microprocessor to address the programmable registers within the chip. The odd parity signal uP Data P is only checked when data is written to the Fifo Data or Checksum Registers and microprocessor parity is enabled.

Clk

The clock input is used to generate some of the chip timing. It is expected to be in the 10-20 Mhz range.

Read En, Write En

During microprocessor accesses, while CS is true, these signals determine the direction of the microprocessor accesses. During data transfers in the WD mode these signals are data strobes used in conjunction with Port A Ack.

Port B 00-07, 10-17, 20-27, 30-37, 0P-3P

Port B is a 32 bit data port. There is one odd parity bit for each byte. Port B 0P is the parity of bits 00-07, PortB 1P is the parity of bits 10-17, Port B 2P is the parity of bits 20-27, and Port B 3P is the parity of bits 30-37.

B Select, B Req, B Ack, Parity Sync, B Output Enable

These signals are used in the data transfer mode to control the handshake of data on Port B. Port B Req and Port B Ack are both gated with Port B Select. The Port B Ack signal is used to strobe the data on the Port B data lines. The parity sync signal is used to indicate to a chip configured as the parity chip to indicate that the last words of data involved in the parity accumulation are on Port B. The Port B data lines will only be driven by the Fifo chip if all of the following conditions are met:

a. the data transfer is from Port A to Port B;
b. the Port B select signal is true;
c. the Port B output enable signal is true; and
d. the chip is not configured as the parity chip or it is in parity correct mode and the Parity Sync signal is true.

Reset

This signal resets all the registers within the chip and causes all bidirectional pins to be in a high impedance state.

DESCRIPTION OF OPERATION

Normal Operation. Normally the chip acts as a simple FIFO chip. A FIFO is simulated by using two RAM buffers in a simple ping-pong mode. It is intended, but not mandatory, that data is burst into or out of the FIFO on Port B. This is done by holding Port B Sel signal low and pulsing the Port B Ack signal. When transferring data from Port B to Port A,

data is first written into RAM X and when this is full, the data paths will be switched such that Port B may start writing to RAM Y. Meanwhile the chip will begin emptying RAM X to Port A. When RAM Y is full and RAM X empty the data paths will be switched again such that Port B may reload RAM X and Port A may empty RAM Y.

Port A Slave Mode. This is the default mode and the chip is reset to this condition. In this mode the chip waits for a master such as one of the SCSI adapter chips 542 to raise Port A Request for data transfer. If data is available the Fifo chip will respond with Port A Ack/Rdy.

Port A WD Mode. The chip may be configured to run in the WD or Western Digital mode. In this mode the chip must be configured as a slave on Port A. It differs from the default slave mode in that the chip responds with Read Enable or Write Enable as appropriate together with Port A Ack/Rdy. This mode is intended to allow the chip to be interfaced to the Western Digital 33C93A SCSI chip or the NCR 53C90 SCSI chip.

Port A Master Mode. When the chip is configured as a master, it will raise Port A Ack/Rdy when it is ready for data transfer. This signal is expected to be tied to the Request input of a DMA controller which will respond with Port A Req when data is available. In order to allow the DMA controller to burst, the Port A Ack/Rdy signal will only be negated after every 8 or 16 bytes transferred.

Port B Parallel Write Mode. In parallel write mode, the chip is configured to be the parity chip for a parallel transfer from Port B to Port A. In this mode, when Port B Select and Port B Request are asserted, data is written into RAM X or RAM Y each time the Port B Ack signal is received. For the first

block of 128 bytes data is simply copied into the selected RAM. The next 128 bytes driven on Port B will be exclusive-ORed with the first 128 bytes. This procedure will be repeated for all drives such that the parity is accumulated in this chip. The Parity Sync signal should be asserted to the parallel chip together with the last block of 128 bytes. This enables the chip to switch access to the other RAM and start accumulating a new 128 bytes of parity.

Port B Parallel Read Mode - Check Data. This mode is set if all drives are being read and parity is to be checked. In this case the Parity Correct bit in the Data Transfer Configuration Register is not set. The parity chip will first read 128 bytes on Port A as in a normal read mode and then raise Port B Request. While it has this signal asserted the chip will monitor the Port B Ack signals and exclusive-or the data on Port B with the data in its selected RAM. The Parity Sync should again be asserted with the last block of 128 bytes. In this mode the chip will not drive the Port B data lines but will check the output of its exclusive-or logic for zero. If any bits are set at this time a parallel parity error will be flagged.

Port B Parallel Read Mode - Correct Data. This mode is set by setting the Parity Correct bit in the Data Transfer Configuration Register. In this case the chip will work exactly as in the check mode except that when Port B Output Enable, Port B Select and Parity Sync are true the data is driven onto the Port B data lines and a parallel parity check for zero is not performed.

Byte Swap. In the normal mode it is expected that Port B bits 00-07 are the first byte, bits 10-17 the second byte, bits 20-27 the third byte, and bits 30-37 the last byte of each word. The order of these bytes

may be changed by writing to the byte swap bits in the configuration register such that the byte address bits are inverted. The way the bytes are written and read also depend on whether the CPU interface is configured as 16 or 8 bits. The following table shows the byte alignments for the different possibilities for data transfer using the Port A Request / Acknowledge handshake:

CPU I/F	Invert Addr 1	Invert Addr 0	Port B 00-07	Port B 10-17	Port B 20-27	Port B 30-37
8	False	False	Port A byte 0	Port A byte 1	Port A byte 2	Port A byte 1
8	False	True	Port A byte 1	Port A byte 0	Port A byte 3	Port A byte 2
8	True	False	Port A byte 2	Port A byte 3	Port A byte 0	Port A byte 1
8	True	True	Port A byte 3	Port A byte 2	Port A byte 1	Port A byte 0
16	False	False	Port A byte 0	uProc byte 0	Port A byte 1	uProc byte 1
16	False	True	uProc byte 0	Port A byte 0	uProc byte 1	Port A byte 1
16	True	False	Port A byte 1	uProc byte 1	Port A byte 0	uProc byte 0
16	True	True	uProc byte 1	Port A byte 1	uProc byte 0	Port A byte 0

When the Fifo is accessed by reading or writing the Fifo Data Register through the microprocessor port in 8 bit mode, the bytes are in the same order as the table above but the uProc data port is used instead of Port A. In 16 bit mode the table above applies.

Odd Length Transfers. If the data transfer is not a multiple of 32 words, or 128 bytes, the microprocessor must manipulate the internal registers of the chip to ensure all data is transferred. Port A Ack and Port B Req are normally not asserted until

all 32 words of the selected RAM are available. These signals may be forced by writing to the appropriate RAM status bits of the Data Transfer Status Register.

When an odd length transfer has taken place the microprocessor must wait until both ports are quiescent before manipulating any registers. It should then reset both of the Enable Data Transfer bits for Port A and Port B in the Data Transfer Control Register. It must then determine by reading their Address Registers and the RAM Access Control Register whether RAM X or RAM Y holds the odd length data. It should then set the corresponding Address Register to a value of 20 hexadecimal, forcing the RAM full bit and setting the address to the first word. Finally the microprocessor should set the Enable Data Transfer bits to allow the chip to complete the transfer.

At this point the Fifo chip will think that there are now a full 128 bytes of data in the RAM and will transfer 128 bytes if allowed to do so. The fact that some of these 128 bytes are not valid must be recognized externally to the FIFO chip.

PROGRAMMABLE REGISTERS

Data Transfer Configuration Register (Read/Write)

Register Address 0. This register is cleared by the reset signal.

Bit 0 WD Mode. Set if data transfers are to use the Western Digital WD33C93A protocol, otherwise the Adaptec 6250 protocol will be used.

Bit 1 Parity Chip. Set if this chip is to accumulate Port B parities.

Bit 2 Parity Correct Mode. Set if the parity chip is to correct parallel parity on Port B.

Bit 3 CPU Interface 16 bits wide. If set, the microprocessor data bits are combined with the Port A data bits to effectively produce a 16 bit Port. All accesses by the microprocessor as well as all data transferred using the Port A Request and Acknowledge handshake will transfer 16 bits.

Bit 4 Invert Port A byte address 0. Set to invert the least significant bit of Port A byte address.

Bit 5 Invert Port A byte address 1. Set to invert the most significant bit of Port A byte address.

Bit 6 Checksum Carry Wrap. Set to enable the carry out of the 16 bit checksum adder to carry back into the least significant bit of the adder.

Bit 7 Reset. Writing a 1 to this bit will reset the other registers. This bit resets itself after a maximum of 2 clock cycles and will therefore normally be read as a 0. No other register should be written for a minimum of 4 clock cycles after writing to this bit.

Data Transfer Control Register (Read/Write)

Register Address 1. This register is cleared by the reset signal or by writing to the reset bit.

Bit 0 Enable Data Transfer on Port A. Set to enable the Port A Req/Ack handshake.

Bit 1 Enable Data Transfer on Port B. Set to enable the Port B Req/Ack handshake.

Bit 2 Port A to Port B. If set, data transfer is from Port A to Port B. If reset, data transfer is from Port B to Port A. In order to avoid any glitches on the request lines, the state of this bit should not be altered at the same time as the enable data transfer bits 0 or 1 above.

Bit 3 uProcessor Parity Enable. Set if parity is to be checked on the microprocessor interface. It will only be checked when writing to the Fifo Data Register or reading from the Fifo Data or Checksum Registers, or during a Port A Request/Acknowledge transfer in 16 bit mode. The chip will, however, always re-generate parity ensuring that correct parity is written to the RAM or read on the microprocessor interface.

Bit 4 Port A Parity Enable. Set if parity is to be checked on Port A. It is checked when accessing the Fifo Data Register in 16 bit mode, or during a Port A Request/Acknowledge transfer. The chip will, however, always re-generate parity ensuring that correct parity is written to the RAM or read on the Port A interface.

Bit 5 Port B Parity Enable. Set if Port B data has valid byte parities. If it is not set, byte parity is generated internally to the chip when writing to the RAMs. Byte parity is not checked when writing from Port B, but always checked when reading to Port B.

Bit 6 Checksum Enable. Set to enable writing to the 16 bit checksum register. This register accumulates a 16 bit checksum for all RAM accesses, including accesses to the Fifo Data Register, as well as all writes to the checksum register. This bit must be reset before reading from the Checksum Register.

Bit 7 Port A Master. Set if Port A is to operate in the master mode on Port A during the data transfer.

Data Transfer Status Register (Read Only)

Register Address 2. This register is cleared by the reset signal or by writing to the reset bit.

Bit 0 Data in RAM X or RAM Y. Set if any bits are true in the RAM X, RAM Y, or Port A byte address registers.

Bit 1 uProc Port Parity Error. Set if the uProc Parity Enable bit is set and a parity error is detected on the microprocessor interface during any RAM access or write to the Checksum Register in 16 bit mode.

Bit 2 Port A Parity Error. Set if the Port A Parity Enable bit is set and a parity error is detected on the Port A interface during any RAM access or write to the Checksum Register.

Bit 3 Port B Parallel Parity Error. Set if the chip is configured as the parity chip, is not in parity correct mode, and a non zero result is detected when the Parity Sync signal is true. It is also set whenever data is read out onto Port B and the data being read back through the bidirectional buffer does not compare.

Bits 4-7 Port B Bytes 0-3 Parity Error. Set whenever the data being read out of the RAMs on the Port B side has bad parity.

Ram Access Control Register (Read/Write)

Register Address 3. This register is cleared by the reset signal or by writing to the reset bit. The Enable Data Transfer bits in the Data Transfer Control Register must be reset before attempting to write to this register, else the write will be ignored.

Bit 0 Port A byte address 0. This bit is the least significant byte address bit. It is read directly bypassing any inversion done by the invert bit in the Data Transfer Configuration Register.

Bit 1 Port A byte address 1. This bit is the most significant byte address bit. It is read directly bypassing any inversion done by the invert bit in the Data Transfer Configuration Register.

Bit 2 Port A to RAM Y. Set if Port A is accessing RAM Y, and reset if it is accessing RAM X .

Bit 3 Port B to RAM Y. Set if Port B is accessing RAM Y, and reset if it is accessing RAM X .

Bit 4 Long Burst. If the chip is configured to transfer data on Port A as a master, and this bit is reset, the chip will only negate Port A Ack/Rdy after every 8 bytes, or 4 words in 16 bit mode, have been transferred. If this bit is set, Port A Ack/Rdy will be negated every 16 bytes, or 8 words in 16 bit mode.

Bits 5-7 Not Used.

RAM X Address Register (Read/Write)

Register Address 4. This register is cleared by the reset signal or by writing to the reset bit. The Enable Data Transfer bits in the Data Transfer Control Register must be reset before attempting to write to this register, else the write will be ignored.

Bits 0-4	RAM X word address
Bit 5	RAM X full
Bits 6-7	Not Used

RAM Y Address Register (Read/Write)

Register Address 5. This register is cleared by the reset signal or by writing to the reset bit. The Enable Data Transfer bits in the Data Transfer Control Register must be reset before attempting to write to this register, else the write will be ignored.

Bits 0-4	RAM Y word address
Bit 5	RAM Y full
Bits 6-7	Not Used

Fifo Data Register (Read/Write)

Register Address 6. The Enable Data Transfer bits in the Data Transfer Control Register must be reset before attempting to write to this register, else the write will be ignored. The Port A to Port B bit in

the Data Transfer Control register must also be set before writing this register. If it is not, the RAM controls will be incremented but no data will be written to the RAM. For consistency, the Port A to PortB should be reset prior to reading this register.

Bits 0-7 are Fifo Data. The microprocessor may access the FIFO by reading or writing this register. The RAM control registers are updated as if the access was using Port A. If the chip is configured with a 16 bit CPU Interface the most significant byte will use the Port A 0-7 data lines, and each Port A access will increment the Port A byte address by 2.

Port A Checksum Register (Read/Write)

Register Address 7. This register is cleared by the reset signal or by writing to the reset bit.

Bits 0-7 are Checksum Data. The chip will accumulate a 16 bit checksum for all Port A accesses. If the chip is configured with a 16 bit CPU interface, the most significant byte is read on the Port A 0-7 data lines. If data is written directly to this register it is added to the current contents rather than overwriting them. It is important to note that the Checksum Enable bit in the Data Transfer Control Register must be set to write this register and reset to read it.

PROGRAMMING THE FIFO CHIP

In general the fifo chip is programmed by writing to the data transfer configuration and control registers to enable a data transfer, and by reading the data transfer status register at the end of the transfer to check the completion status. Usually the data transfer itself will take place with both the Port A and the Port B handshakes enabled, and in this case the data transfer itself should be done without

any other microprocessor interaction. In some applications, however, the Port A handshake may not be enabled, and it will be necessary for the microprocessor to fill or empty the fifo by repeatedly writing or reading the Fifo Data Register.

Since the fifo chip has no knowledge of any byte counts, there is no way of telling when any data transfer is complete by reading any register within this chip itself. Determination of whether the data transfer has been completed must therefore be done by some other circuitry outside this chip.

The following C language routines illustrate how the parity FIFO chip may be programmed. The routines assume that both Port A and the microprocessor port are connected to the system microprocessor, and return a size code of 16 bits, but that the hardware addresses the Fifo chip as long 32 bit registers.

```
struct FIFO_regs {
    unsigned char config,a1,a2,a3 ;
    unsigned char control,b1,b2,b3;
    unsigned char status,c1,c2,c3;
    unsigned char ram_access_control,d1,d2,d3;
    unsigned char ram_X_addr,e1,e2,e3;
    unsigned char ram_Y_addr,f1,f2,f3;
    unsigned long data;
    unsigned int checksum,h1;
    };

#define FIFO1 ((struct  FIFO_regs*) FIFO_BASE_ADDRESS)

#define FIFO_RESET 0x80
#define FIFO_16_BITS 0x08
#define FIFO_CARRY_WRAP 0x40
#define FIFO_PORT_A_ENABLE 0x01
#define FIFO_PORT_B_ENABLE 0x02
#define FIFO_PORT_ENABLES 0x03
#define FIFO_PORT_A_TO_B 0x04
#define FIFO_CHECKSUM_ENABLE 0x40
#define FIFO_DATA_IN_RAM 0x01
#define FIFO_FORCE_RAM_FULL 0x20

#define PORT_A_TO_PORT_B(fifo) ((fifo-> control ) & 0x04)
#define PORT_A_BYTE_ADDRESS(fifo) ((fifo->ram_access_control) &
0x03)
#define PORT_A_TO_RAM_Y(fifo)  ((fifo->ram_access_control ) &   0x04)
#define PORT_B_TO_RAM_Y(fifo)  ((fifo-> ram_access_control ) &   0x08)
```

```
/*****************************************************************
        The following routine initiates a Fifo data transfer using two
values passed to it.

    config_data   This is the data to be written to the configuration register.

    control_data  This is the data to be written to the Data Transfer Control
                  Register.  If the data transfer is to take place
                  automatically using both the Port Aand Port B
                  handshakes, both data transfer enables bits should be
                  set in this parameter.
*****************************************************************/

FIFO_initiate_data_transfer(config_data, control_data)
unsigned char config_data, control_data;
{
    FIFO1->config = config_data | FIFO_RESET;       /* Set
Configuration value & Reset */
    FIFO1->control = control_data & (~FIFO_PORT_ENABLES);  /* Set
        everything but enables */
    FIFO1->control = control_data ;                 /* Set data transfer
enables */
}

/*****************************************************************
        The following routine forces the transfer of any odd bytes that
have been left in the Fifo at the end of a data transfer.
It first disables both ports, then forces the Ram Full bits, and then
re-enables the appropriate Port.
*****************************************************************/

FIFO_force_odd_length_transfer()
{
    FIFO1->control &= ~FIFO_PORT_ENABLES; /* Disable Ports A & B
*/
    if (PORT_A_TO_PORT_B(FIFO1)) {
        if (PORT_A_TO_RAM_Y(FIFO1)) {
            FIFO1->ram_Y_addr = FIFO_FORCE_RAM_FULL; /*
Set RAM Y full */
        }
        else FIFO1->ram_X_addr = FIFO_FORCE_RAM_FULL ;  /* Set
RAM X full */
        FIFO1->control |= FIFO_PORT_B_ENABLE ;          /*
Re-Enable Port B */
    }
    else {
        if (PORT_B_TO_RAM_Y(FIFO1)) {
            FIFO1->ram_Y_addr = FIFO_FORCE_RAM_FULL ;   /*
Set RAM Y full */
        }
        else FIFO1->ram_X_addr = FIFO_FORCE_RAM_FULL ;  /* Set
RAM X full */
```

```
            FIFO1->control |= FIFO_PORT_A_ENABLE ;        /*
Re-Enable Port A */
        }
}

/*****************************************************************
            The following routine returns how many odd bytes have been
left in the Fifo at the end of a data transfer.
*****************************************************************/

int FIFO_count_odd_bytes()
{
    int number_odd_bytes;
    number_odd_bytes=0;
    if (FIFO1->status & FIFO_DATA_IN_RAM)  {
        if (PORT_A_TO_PORT_B(FIFO1))  {
            number_odd_bytes =
(PORT_A_BYTE_ADDRESS(FIFO1)) ;
            if (PORT_A_TO_RAM_Y(FIFO1))
                number_odd_bytes += (FIFO1->ram_Y_addr) *
4 ;
            else number_odd_bytes += (FIFO1->ram_X_addr) * 4 ;
        }
        else {
            if (PORT_B_TO_RAM_Y(FIFO1))
                number_odd_bytes = (FIFO1->ram_Y_addr) * 4 ;
            else number_odd_bytes = (FIFO1->ram_X_addr) * 4 ;
        }
    }
    return (number_odd_bytes);
}

/*****************************************************************
            The following routine tests the microprocessor interface of the
chip.  It first writes and reads the first 6 registers.  It then writes 1s, 0s, and
an address pattern to the RAM, reading the data back and checking it.

            The test returns a bit significant error code where each bit
represents the address of the registers that failed.

    Bit 0 = config register failed
    Bit 1 = control register failed
    Bit 2 = status register failed
    Bit 3 = ram access control register failed
    Bit 4 = ram X address register failed
    Bit 5 = ram Y address register failed
    Bit 6 = data register failed
    Bit 7 = checksum register failed
*****************************************************************/

#define RAM_DEPTH 64          /* number of long words in Fifo Ram */

reg_expected_data[6] = { 0x7F, 0xFF, 0x00, 0x1F, 0x3F, 0x3F };
```

```
char FIFO_uprocessor_interface_test()
{
    unsigned long test_data;
    char *register_addr;
    int i;
    char j,error;
    FIFO1->config = FIFO_RESET;              /* reset the chip */
    error=0;
    register_addr =(char *) FIFO1;
    j=1;

    /* first test registers 0 thru 5 */

    for (i=0; i<6; i++) {
        *register_addr = 0xFF;               /* write test data */
        if (*register_addr != reg_expected_data[i]) error |= j;
        *register_addr = 0;                  /* write 0s to register */
        if (*register_addr) error |= j;
        *register_addr = 0xFF;               /* write test data again */
        if (*register_addr != reg_expected_data[i]) error |= j;
        FIFO1->config = FIFO_RESET;          /* reset the chip */
        if (*register_addr) error |= j; /* register should be 0 */
        register_addr++;                     /* go to next register */
        j <<=1;
    }

        /* now test Ram data & checksum registers
        test 1s throughout Ram & then test 0s */

    for (test_data = -1; test_data != 1; test_data++)  {     /* test for 1s
& 0s */
        FIFO1->config = FIFO_RESET | FIFO_16_BITS ;
        FIFO1->control = FIFO_PORT_A_TO_B;
        for (i=0;i<RAM_DEPTH;i++)                /* write data to RAM
*/
            FIFO1->data = test_data;
        FIFO1->control = 0;
        for (i=0;i<RAM_DEPTH;i++)
            if (FIFO1->data != test_data) error |= j;    /* read &
check data */
        if (FIFO1->checksum) error |= 0x80;              /* checksum
should = 0 */
    }

        /* now test Ram data with address pattern
         uses a different pattern for every byte */

    test_data=0x00010203;                /* address pattern start */
    FIFO1->config = FIFO_RESET | FIFO_16_BITS |
FIFO_CARRY_WRAP;
    FIFO1->control = FIFO_PORT_A_TO_B |
FIFO_CHECKSUM_ENABLE;
    for (i=0;i<RAM_DEPTH;i++) {
        FIFO1->data = test_data;             /* write address pattern */
```

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```
            test_data + = 0x04040404;
        }
        test_data=0x00010203;              /* address pattern start */
        FIFO1->control = FIFO_CHECKSUM_ENABLE;
        for (i=0;i<RAM_DEPTH;i++) {
            if (FIFO1->status != FIFO_DATA_IN_RAM)
                error | = 0x04;                /* should be data in ram */
            if (FIFO1->data != test_data) error | = j;    /* read & check
address pattern */
            test_data + = 0x04040404;
        }
        if (FIFO1->checksum != 0x0102) error | = 0x80;  /* test checksum of
address pattern */
        FIFO1->config = FIFO_RESET | FIFO_16_BITS ; /* inhibit carry wrap
*/
        FIFO1->checksum = 0xFEFE;       /* writing adds to checksum */
        if (FIFO1->checksum) error | =0x80;        /* checksum should be 0
*/
        if (FIFO1->status) error | = 0x04;    /* status should be 0 */
        return (error);
    }
```

SUBSTITUTE SHEET

Claims:

1. Network server apparatus for use with a data network and a mass storage device, comprising:

an interface processor unit coupleable to said network and to said mass storage device;

a host processor unit capable of running remote procedures defined by a client node on said network;

means in said interface processor unit for satisfying requests from said network to store data from said network on said mass storage device;

means in said interface processor unit for satisfying requests from said network to retrieve data from said mass storage device to said network; and

means in said interface processor unit for transmitting predefined categories of messages from said network to said host processor unit for processing in said host processor unit, said transmitted messages including all requests by a network client to run client-defined procedures on said network server apparatus.

2. Apparatus according to claim 1, wherein said interface processor unit comprises:

a network control unit coupleable to said network;

a data control unit coupleable to said mass storage device;

a buffer memory;

means in said network control unit for transmitting to said data control unit requests from said network to store specified storage data from said network on said mass storage device;

means in said network control unit for transmitting said specified storage data from said network to said buffer memory and from said buffer memory to said data control unit;

means in said network control unit for transmitting to said data control unit requests from said network to retrieve specified retrieval data from said mass storage device to said network;

means in said network control unit for transmitting said specified retrieval data from said data control unit to said buffer memory and from said buffer memory to said network; and

means in said network control unit for transmitting said predefined categories of messages from said network to said host processing unit for processing by said host processing unit.

3. Apparatus according to claim 2, wherein said data control unit comprises:

a storage processor unit coupleable to said mass storage device;

a file processor unit;

means on said file processor unit for translating said file system level storage requests from said network into requests to store data at specified physical storage locations in said mass storage device;

means on said file processor unit for instructing said storage processor unit to write data from said buffer memory into said specified physical storage locations in said mass storage device;

means on said file processor unit for translating file system level retrieval requests from said network into requests to retrieve data from specified physical retrieval locations in said mass storage device;

means on said file processor unit for instructing said storage processor unit to retrieve data from said specified physical retrieval locations in said mass storage device to said buffer memory if said data from said specified physical locations is not already in said buffer memory; and

means in said storage processor unit for transmitting data between said buffer memory and said mass storage device.

4. Network server apparatus for use with a data network and a mass storage device, comprising:

a network control unit coupleable to said network;

a data control unit coupleable to said mass storage device;

a buffer memory;

means for transmitting from said network control unit to said data control unit requests from said network to store specified storage data from said network on said mass storage device;

means for transmitting said specified storage data by DMA from said network control unit to said buffer memory and by DMA from said buffer memory to said data control unit;

means for transmitting from said network control unit to said data control unit requests from said network to retrieve specified retrieval data from said mass storage device to said network; and

means for transmitting said specified retrieval data by DMA from said data control unit to said buffer memory and by DMA from said buffer memory to said network control unit.

5. Apparatus according to claim 1, for use further with a buffer memory, and wherein said requests from said network to store and retrieve data include file system level storage and retrieval requests respectively, and wherein said interface processor unit comprises:

a storage processor unit coupleable to said mass storage device;

a file processor unit;

means on said file processor unit for translating said file system level storage requests into requests to store data at specified physical storage locations in said mass storage device;

means on said file processor unit for instructing said storage processor unit to write data from said buffer memory into said specified physical storage locations in said mass storage device;

means on said file processor unit for translating said file system level retrieval requests into requests to retrieve data from specified physical retrieval locations in said mass storage device;

means on said file processor unit for instructing said storage processor unit to retrieve data from said specified physical retrieval locations in said mass storage

device to said buffer memory if said data from said specified physical locations is not already in said buffer memory; and

means in said storage processor unit for transmitting data between said buffer memory and said mass storage device.

6. A data control unit for use with a data network and a mass storage device, and in response to file system level storage and retrieval requests from said data network, comprising:

a data bus different from said network;

a buffer memory bank coupled to said bus;

storage processor apparatus coupled to said bus and coupleable to said mass storage device;

file processor apparatus coupled to said bus, said file processor apparatus including a local memory bank

first means on said file processor apparatus for translating said file system level storage requests into requests to store data at specified physical storage locations in said mass storage device; and

second means on said file processor apparatus for translating said file system level retrieval requests into requests to retrieve data from specified physical retrieval locations in said mass storage device, said first and second means for translating collectively including means for caching file control information through said local memory bank in said file processor unit,

said data control unit further comprising means for caching the file data, to be stored or retrieved according to said storage and retrieval requests, through said buffer memory bank.

7. A network node for use with a data network and a mass storage device, comprising:

a system buffer memory;

a host processor unit having direct memory access to said system buffer memory;

a network control unit coupleable to said network and having direct memory access to said system buffer memory;

a data control unit coupleable to said mass storage device and having direct memory access to said system buffer memory;

first means for satisfying requests from said network to store data from said network on said mass storage device;

second means for satisfying requests from said network to retrieve data from said mass storage device to said network; and

third means for transmitting predefined categories of messages from said network to said host processor unit for processing in said host processor unit, said first, second and third means collectively including

means for transmitting from said network control unit to said system memory bank by direct memory access file data from said network for storage on said mass storage device,

means for transmitting from said system memory bank to said data control unit by direct memory access said file data from said network for storage on said mass storage device,

means for transmitting from said data control unit to said system memory bank by direct memory access file data for retrieval from said mass storage device to said network, and

means for transmitting from said system memory bank to said network control unit said file data for retrieval from said mass storage device to said network;

at least said network control unit including a microprocessor and local instruction storage means distinct from said system buffer memory, all instructions for said microprocessor residing in said local instruction storage means.

8. A network file server for use with a data network and a mass storage device, comprising:

a host processor unit running a Unix operating system;

an interface processor unit coupleable to said network and to said mass storage device, said interface processor unit including means for decoding all NFS requests from said network, means for performing all procedures for satisfying said NFS requests, means for encoding any NFS reply messages for return transmission on said network, and means for transmitting predefined non-NFS categories of messages from said network to said host processor unit for processing in said host processor unit.

9. Network server apparatus for use with a data network, comprising:

a network controller coupleable to said network to receive incoming information packets over said network, said incoming information packets including certain packets which contain part or all of a request to said server apparatus, said request being in either a first or a second class of requests to said server apparatus;

a first additional processor;

an interchange bus different from said network and coupled between said network controller and said first additional processor;

means in said network controller for detecting and satisfying requests in said first class of requests contained in said certain incoming information packets, said network controller lacking means in said network controller for satisfying requests in said second class of requests;

means in said network controller for detecting and assembling into assembled requests, requests in said second class of requests contained in said certain incoming information packets;

means for delivering said assembled requests from said network controller to said first additional processor over said interchange bus; and

means in said first additional processor for further processing said assembled requests in said second class of requests.

10. Apparatus according to claim 9, wherein said packets each include a network node destination address, and wherein said means in said network controller for detecting and assembling into assembled requests, assembles said assembled requests in a format which omits said network node destination addresses.

11. Apparatus according to claim 9, wherein said means in said network controller for detecting and satisfying requests in said first class of requests, assembles said requests in said first class of requests into assembled requests before satisfying said requests in said first class of requests.

12. Apparatus according to claim 9, wherein said packets each include a network node destination address, wherein said means in said network controller for detecting and assembling into assembled requests, assembles said assembled requests in a format which omits said network node destination addresses, and wherein said means in said network controller for detecting and satisfying requests in said first class of requests, assembles said requests in said first class of requests, in a format which omits said network node destination addresses, before satisfying said requests in said first class of requests.

13. Apparatus according to claim 9, wherein said means in said network controller for detecting and satisfying requests in said first class includes means for preparing an outgoing message in response to one of said first class of requests, means for packaging said outgoing message in outgoing information packets suitable for transmission over said network, and means for transmitting said outgoing information packets over said network.

14. Apparatus according to claim 9, further comprising a buffer memory coupled to said interchange bus, and wherein said means for delivering said assembled requests comprises:

means for transferring the contents of said assembled requests over said interchange bus into said buffer memory; and

means for notifying said first additional processor of the presence of said contents in said buffer memory.

15. Apparatus according to claim 9, wherein said means in said first additional processor for further processing said assembled requests includes means for preparing an outgoing message in response to one of said second class of requests, said apparatus further comprising means for delivering said outgoing message from said first additional processor to said network controller over said interchange bus, said network controller further comprising means in said network controller for packaging said outgoing message in outgoing information packets suitable for transmission over said network, and means in said network controller for transmitting said outgoing information packages over said network.

16. Apparatus according to claim 9, wherein said first class of requests comprises requests for an address of said server apparatus, and wherein said means in said network controller for detecting and satisfying requests in said first class comprises means for preparing a response packet to such an address request and means for transmitting said response packet over said network.

17. Apparatus according to claim 9, for use further with a second data network, said network controller being coupleable further to said second network, wherein said first class of requests comprises requests to route a message to a destination reachable over said second network, and wherein said means in said network controller for detecting and satisfying requests in said first class comprises means for detecting that one of said certain packets comprises a request to route a message contained in said one of said certain packets to a destination reachable over said second network, and means for transmitting said message over said second network.

18. Apparatus according to claim 17, for use further with a third data network, said network controller further comprising means in said network controller for detecting particular requests in said incoming information packets to route a message contained in said particular requests, to a destination reachable over said third network, said apparatus further comprising:

a second network controller coupled to said interchange bus and couplable to said third data network;

means for delivering said message contained in said particular requests to said second network controller over said interchange bus; and

means in said second network controller for transmitting said message contained in said particular requests over said third network.

19. Apparatus according to claim 9, for use further with a third data network, said network controller further comprising means in said network controller for detecting particular requests in said incoming information packets to route a message contained in said particular requests, to a destination reachable over said third network, said apparatus further comprising:

a second network controller coupled to said interchange bus and couplable to said third data network;

means for delivering said message contained in said particular requests to said second network controller over said interchange bus; and

means in said second network controller for transmitting said message contained in said particular requests over said third network.

20. Apparatus according to claim 9, for use further with a mass storage device, wherein said first additional processor comprises a data control unit couplable to said mass storage device, wherein said second class of requests comprises remote calls to procedures for managing a file system in said mass storage device, and wherein said means in said first additional processor for further processing said assembled requests in said second class of requests comprises

means for executing file system procedures on said mass storage device in response to said assembled requests.

21. Apparatus according to claim 20, wherein said file system procedures include a read procedure for reading data from said mass storage device,

said means in said first additional processor for further processing said assembled requests including means for reading data from a specified location in said mass storage device in response to a remote call to said read procedure,

said apparatus further including means for delivering said data to said network controller,

said network controller further comprising means on said network controller for packaging said data in outgoing information packets suitable for transmission over said network, and means for transmitting said outgoing information packets over said network.

22. Apparatus according to claim 21, wherein said means for delivering comprises:

a system buffer memory coupled to said interchange bus;

means in said data control unit for transferring said data over said interchange bus into said buffer memory; and

means in said network controller for transferring said data over said interchange bus from said system buffer memory to said network controller.

23. Apparatus according to claim 20, wherein said file system procedures include a read procedure for reading a specified number of bytes of data from said mass storage device beginning at an address specified in logical terms including a file system ID and a file ID, said means for executing file system procedures comprising:

means for converting the logical address specified in a remote call to said read procedure to a physical address; and

means for reading data from said physical address in said mass storage device.

24. Apparatus according to claim 23, wherein said mass storage device comprises a disk drive having a numbered tracks and sectors, wherein said logical address specifies said file system ID, said file ID, and a byte offset, and wherein said physical address specifies a corresponding track and sector number.

25. Apparatus according to claim 20, wherein said file system procedures include a read procedure for reading a specified number of bytes of data from said mass storage device beginning at an address specified in logical terms including a file system ID and a file ID,

said data control unit comprising a file processor coupled to said interchange bus and a storage processor coupled to said interchange bus and couplable to said mass storage device,

said file processor comprising means for converting the logical address specified in a remote call to said read procedure to a physical address,

said apparatus further comprising means for delivering said physical address to said storage processor,

said storage processor comprising means for reading data from said physical address in said mass storage device and for transferring said data over said interchange bus into said buffer memory; and

means in said network controller for transferring said data over said interchange bus from said system buffer memory to said network controller.

26. Apparatus according to claim 20, wherein said file system procedures include a write procedure for writing data contained in an assembled request, to said mass storage device,

said means in said first additional processor for further processing said assembled requests including means for writing said data to a specified location in said mass storage device in response to a remote call to said read procedure.

27. Apparatus according to claim 9, wherein said first additional processor comprises a host computer coupled to said interchange bus, wherein said second class of requests comprises remote calls to procedures other than procedures for managing a file system, and wherein said means in said first additional processor for further processing said assembled requests in said second class of requests comprises means for executing remote procedure calls in response to said assembled requests.

28. Apparatus according to claim 27, for use further with a mass storage device and a data control unit couplable to said mass storage device and coupled to said interchange bus, wherein said network controller further comprises means in said network controller for detecting and assembling remote calls, received over said network, to procedures for managing a file system in said mass storage device, and wherein said data control unit comprises means for executing file system procedures on said mass storage device in response to said remote calls to procedures for managing a file system in said mass storage device.

29. Apparatus according to claim 27, further comprising means for delivering all of said incoming information packets not recognized by said network controller to said host computer over said interchange bus.

30. Apparatus according to claim 9, wherein said network controller comprises:

a microprocessor;

a local instruction memory containing local instruction code;

a local bus coupled between said microprocessor and said local instruction memory;

bus interface means for interfacing said microprocessor with said interchange bus at times determined by said microprocessor in response to said local instruction code; and

network interface means for interfacing said microprocessor with said data network,

said local instruction memory including all instruction code necessary for said microprocessor to perform said function of detecting and satisfying requests in said first class of requests, and all instruction code necessary for said microprocessor to perform said function of detecting and assembling into assembled requests, requests in said second class of requests.

31. Network server apparatus for use with a data network, comprising:

a network controller coupleable to said network to receive incoming information packets over said network, said incoming information packets including certain packets which contain part or all of a message to said server apparatus, said message being in either a first or a second class of messages to said server apparatus, said messages in said first class or messages including certain messages containing requests;

a host computer;

an interchange bus different from said network and coupled between said network controller and said host computer;

means in said network controller for detecting and satisfying said requests in said first class of messages;

means for delivering messages in said second class of messages from said network controller to said host computer over said interchange bus; and

means in said host computer for further processing said messages in said second class of messages.

32. Apparatus according to claim 31, wherein said packets each include a network node destination address, and wherein said means for delivering messages in said second class of messages comprises means in said network controller for detecting said messages in said second class of messages and assembling them into assembled messages in a format which omits said network node destination addresses.

33. Apparatus according to claim 31, wherein said means in said network controller for detecting and satisfying requests in said first class includes means for preparing an outgoing message in response to one of said requests in said first class of messages, means for packaging said outgoing message in outgoing information packets suitable for transmission over said network, and means for transmitting said outgoing information packets over said network.

34. Apparatus according to claim 31, for use further with a second data network, said network controller being coupleable further to said second network, wherein said first class of messages comprises messages to be routed to a destination reachable over said second network, and wherein said means in said network controller for detecting and satisfying requests in said first class comprises means for detecting that one of said certain packets includes a request to route a message contained in said one of said certain packets to a destination reachable over said second network, and means for transmitting said message over said second network.

35. Apparatus according to claim 31, for use further with a third data network, said network controller further comprising means in said network controller for detecting particular messages in said incoming information packets to be routed to a destination reachable over said third network, said apparatus further comprising:

a second network controller coupled to said interchange bus and couplable to said third data network;

means for delivering said particular messages to said second network controller over said interchange bus, substantially without involving said host computer; and

means in said second network controller for transmitting said message contained in said particular requests over said third network, substantially without involving said host computer.

36. Apparatus according to claim 31, for use further with a mass storage device, further comprising a data control unit coupleable to said mass storage device,

said network controller further comprising means in said network controller for detecting ones of said incoming information packets containing remote calls to procedures for managing a file system in said mass storage device, and means in said network controller for assembling said remote calls from said incoming packets into assembled calls, substantially without involving said host computer,

said apparatus further comprising means for delivering said assembled file system calls to said data control unit over said interchange bus substantially without involving said host computer, and said data control unit comprising means in said data control unit for executing file system procedures on said mass storage device in response to said assembled file system calls, substantially without involving said host computer.

37. Apparatus according to claim 31, further comprising means for delivering all of said incoming information packets not recognized by said network controller to said host computer over said interchange bus.

38. Apparatus according to claim 31, wherein said network controller comprises:

a microprocessor;

a local instruction memory containing local instruction code;

a local bus coupled between said microprocessor and said local instruction memory;

bus interface means for interfacing said microprocessor with said interchange bus at times determined by said microprocessor in response to said local instruction code; and

network interface means for interfacing said microprocessor with said data network,

said local instruction memory including all instruction code necessary for said microprocessor to perform said function of detecting and satisfying requests in said first class of requests.

39. File server apparatus for use with a mass storage device, comprising:

a requesting unit capable of issuing calls to file system procedures in a device-independent form;

a file controller including means for converting said file system procedure calls from said device-independent form to a device-specific form and means for issuing device-specific commands in response to at least a subset of said procedure calls, said file controller operating in parallel with said requesting unit; and

a storage processor including means for executing said device-specific commands on said mass storage device, said storage processor operating in parallel with said requesting unit and said file controller.

40. Apparatus according to claim 39, further comprising:

an interchange bus;

first delivery means for delivering said file system procedure calls from said requesting unit to said file controller over said interchange bus; and

second delivery means for delivering said device-specific commands from said file controller to said storage processor over said interchange bus.

41. Apparatus according to claim 39, further comprising:

an interchange bus coupled to said requesting unit and to said file controller;

first memory means in said requesting unit and addressable over said interchange bus;

second memory means in said file controller;

means in said requesting unit for preparing in said first memory means one of said calls to file system procedures;

means for notifying said file controller of the availability of said one of said calls in said first memory means; and

means in said file controller for controlling an access to said first memory means for reading said one of said calls over said interchange bus into said second memory means in response to said notification.

42. Apparatus according to claim 41, wherein said means for notifying said file controller comprises:

a command FIFO in said file controller addressable over said interchange bus; and

means in said requesting unit for controlling an access to said FIFO for writing a descriptor into said FIFO over said interchange bus, said descriptor describing an address in said first memory means of said one of said calls and an indication that said address points to a message being sent.

43. Apparatus according to claim 41, further comprising:

means in said file controller for controlling an access to said first memory means over said interchange bus for modifying said one of said calls in said first memory means to prepare a reply to said one of said calls; and

means for notifying said requesting unit of the availability of said reply in said first memory.

44. Apparatus according to claim 41, further comprising:

a command FIFO in said requesting processor addressable over said interchange bus; and

means in said file controller for controlling an access to said FIFO for writing a descriptor into said FIFO over said interchange bus, said descriptor describing said address in said first memory and an indication that said address points to a reply to said one of said calls.

45. Apparatus according to claim 39, further comprising:

an interchange bus coupled to said file controller and to said storage processor;

second memory means in said file controller and addressable over said interchange bus;

means in said file controller for preparing one of said device-specific commands in said second memory means;

means for notifying said storage processor of the availability of said one of said commands in said second memory means; and

means in said storage processor for controlling an access to said second memory means for reading said one of said commands over said interchange bus in response to said notification.

46. Apparatus according to claim 45, wherein said means for notifying said storage processor comprises:

a command FIFO in said storage processor addressable over said interchange bus; and

means in said file controller for controlling an access to said FIFO for writing a descriptor into said FIFO over said interchange bus, said descriptor describing an address in said second memory of said one of said calls and an indication that said address points to a message being sent.

47. Apparatus according to claim 39, wherein said means for converting said file system procedure calls comprises:

a file control cache in said file controller, storing device-independent to device-specific conversion information; and

means for performing said conversions in accordance with said conversion information in said file control cache.

48. Apparatus according to claim 39, wherein said mass storage device includes a disk drive having numbered sectors, wherein one of said file system procedure calls is a read data procedure call,

said apparatus further comprising an interchange bus and a system buffer memory addressable over said interchange bus,

said means for converting said file system procedure calls including means for issuing a read sectors command in response to one of said read data procedure calls, said read sectors command specifying a starting sector on said disk drive, a count indicating the amount of data to read, and a pointer to a buffer in said system buffer memory, and

said means for executing device-specific commands including means for reading data from said disk drive beginning at said starting sector and continuing for the number of sectors indicated by said count, and controlling an access to said system buffer memory for writing said data over said interchange bus to said buffer in said system buffer memory.

49. Apparatus according to claim 48, wherein said file controller further includes means for determining whether the data specified in said one of said read data procedure calls is already present in said system buffer memory, said means for converting issuing said read sectors command only if said data is not already present in said system buffer memory.

50. Apparatus according to claim 48, further comprising:

means in said storage processor for controlling a notification of said file controller when said read sectors command has been executed;

means in said file controller, responsive to said notification from said storage processor, for controlling a notification of said requesting unit that said read data procedure call has been executed; and

means in said requesting unit, responsive to said notification from said file controller, for controlling an access to said system buffer memory for reading said data over said interchange bus from said buffer in said system buffer memory to said requesting unit.

51. Apparatus according to claim 39, wherein said mass storage device includes a disk drive having numbered sectors, wherein one of said file system procedure calls is a write data procedure call,

said apparatus further comprising an interchange bus and a system buffer memory addressable over said interchange bus,

said means for converting said file system procedure calls including means for issuing a write sectors command in response to one of said write data procedure calls, said write data procedure call including a pointer to a buffer in said system buffer memory containing data to be written, and said write sectors command including a starting sensor on said disk drive, a count indicating the amount of data to write, and said pointer to said buffer in said buffer memory, and

said means for executing device-specific commands including means for controlling an access to said buffer memory for reading said data over said interchange bus from said buffer in said system buffer memory, and writing said data to said disk drive beginning at said starting sector and continuing for the number of sectors indicated by said count.

52. Apparatus according to claim 51, further comprising:

means in said requesting unit for controlling an access to said system buffer memory for writing said data over said interchange bus to said buffer in said system buffer memory; and

means in said requesting unit for issuing said one of said write data procedure calls when said data has been written to said buffer in said system buffer memory.

53. Apparatus according to claim 52, further comprising:

means in said requesting unit for issuing a buffer allocation request; and

means in said file controller for allocating said buffer in said system buffer memory in response to said buffer allocation request, and for providing said pointer, before said data is written to said buffer in said system buffer memory.

54. Network controller apparatus for use with a first data network carrying signals representing information packets encoded according to a first physical layer protocol, comprising:

a first network interface unit, a first packet bus and first packet memory addressable by said first network interface unit over said first packet bus, said first network interface unit including means for receiving signals over said first network representing incoming information packets, extracting said incoming information packets and writing said incoming information packets into said first packet memory over said first packet bus;

a first packet bus port;

first packet DMA means for reading data over said first packet bus from said first packet memory to said first packet bus port; and

a local processor including means for accessing said incoming information packets in said first packet memory and, in response to the contents of said incoming information packets, controlling said first packet DMA means to read selected data over said first packet bus from said first packet memory to said first packet bus port, said local processor including a CPU, a CPU bus and CPU memory containing CPU instructions, said local processor operating in response to said CPU instructions, said CPU instructions being received by said CPU over said CPU bus independently of any of said writing by said first network interface unit of incoming information packets into said first packet memory over said first packet bus and independently of any of said reading by said first packet DMA means of data over said first packet bus from said first packet memory to said first packet bus port.

55. Apparatus according to claim 54, wherein said first network interface unit further includes means for reading outgoing information packets from said first packet memory over said first packet bus, encoding said outgoing information packets according to said first physical layer protocol, and transmitting signals over said first network representing said outgoing information packets,

said local processor further including means for preparing said outgoing information packets in said first packet memory, and for controlling said first network interface unit to read, encode and transmit said outgoing information packets,

said receipt of CPU instructions by said CPU over said CPU bus being

independent further of any of said reading by said first network interface unit of outgoing information packets from said first packet memory over said first packet bus.

56. Apparatus according to claim 54, further comprising a first FIFO having first and second ports, said first port of said first FIFO being said first packet bus port.

57. Apparatus according to claim 56, for use further with an interchange bus, further comprising interchange bus DMA means for reading data from said second port of said first FIFO onto said interchange bus,

said local processor further including means for controlling said interchange bus DMA means to read said data from said second port of said first FIFO onto said interchange bus.

58. Apparatus according to claim 54, for use further with a second data network carrying signals representing information packets encoded according to a second physical layer protocol, further comprising:

a second network interface unit, a second packet bus and second packet memory addressable by said second network interface unit over said second packet bus, said second network interface unit including means for reading outgoing information packets from said second packet memory over said second packet bus, encoding said outgoing information packets according to said second physical layer protocol, and transmitting signals over said second network representing said outgoing information packets;

a second packet bus port; and

second packet DMA means for reading data over said second packet bus from said second packet bus port to said second packet memory,

said local processor further including means for controlling said second packet DMA means to read data over said second packet bus from said second packet bus port to said second packet memory, and for controlling said second network interface

unit to read, encode and transmit outgoing information packets from said data in said second packet memory,

said receipt of CPU instructions by said CPU over said CPU bus being independent further of any of said reading by said second packet DMA means of data over said second packet bus from said second packet bus port to said second packet memory, and independent further of any of said reading by said second network interface unit of outgoing information packets from said second packet memory over said second packet bus,

and all of said accesses to said first packet memory over said first packet bus being independent of said accesses to said second packet memory over said second packet bus.

59. Apparatus according to claim 58, wherein said second physical layer protocol is the same as said first physical layer protocol.

60. Apparatus according to claim 58, further comprising means, responsive to signals from said processor, for coupling data from said first packet bus port to said second packet bus port.

61. Apparatus according to claim 61, further comprising:

first and second FIFOs, each having first and second ports, said fist port of said first FIFO being said first packet bus port and said first port of said second FIFO being said second packet bus port;

an interchange bus; and

interchange bus DMA means for transferring data between said interchange bus and either said second port of said first FIFO or said second port of said second FIFO, selectably in response to DMA control signals from said local processor.

62. Apparatus according to claim 58, wherein said interchange bus DMA means comprises:

a transfer bus coupled to said second port of said first FIFO and to said second port of said second FIFO;

coupling means coupled between said transfer bus and said interchange bus; and

a controller coupled to receive said DMA control signals from said processor and coupled to said first and second FIFOs and to said coupling means to control data transfers over said transfer bus.

63. Storage processing apparatus for use with a plurality of storage devices on a respective plurality of channel buses, and an interchange bus, said interchange bus capable of transferring data at a higher rate than any of said channel buses, comprising:

data transfer means coupled to each of said channel buses and to said interchange bus, for transferring data in parallel between said data transfer means and each of said channel buses at the data transfer rates of each of said channel buses, respectively, and for transferring data between said data transfer means and said interchange bus at a data transfer rate higher than said data transfer rates of any of said channel buses; and

a local processor including transfer control means for controlling said data transfer means to transfer data between said data transfer means and specified ones of said channel buses and for controlling said data transfer means to transfer data between said data transfer means and said interchange bus,

said local processor including a CPU, a CPU bus and CPU memory containing CPU instructions, said local processor operating in response to said CPU instructions, said CPU instructions being received by said CPU over said CPU bus independently of any of said data transfers between said channel buses and said data transfer means and independently of any of said data transfers between said data transfer means and said interchange bus.

64. Apparatus according to claim 63, wherein the highest data transfer rate of said interchange bus is substantially equal to the sum of the highest data transfer rates of all of said channel buses.

65. Apparatus according to claim 63, wherein said data transfer means comprises:

a FIFO corresponding to each of said channel buses, each of said FIFOs having a first port and a second port;

a channel adapter coupled between the first port of each of said FIFOs and a respective one of said channels; and

DMA means coupled to the second port of each of said FIFOs and to said interchange bus, for transferring data between said interchange bus and one of said FIFOs as specified by said local processor,

said transfer control means in said local processor comprising means for controlling each of said channel adapters separately to transfer data between the channel bus coupled to said channel adapter and the FIFO coupled to said channel adapter, and for controlling said DMA controller to transfer data between separately specified ones of said FIFOs and said interchange bus, said DMA means performing said transfers sequentially.

66. Apparatus according to claim 65, wherein said DMA means comprises a command memory and a DMA processor, said local processor having means for writing FIFO/interchange bus DMA commands into said command memory, each of said commands being specific to a given one said FIFOs and including an indication of the direction of data transfer between said interchange bus and said given FIFO, each of said FIFOs generating a ready status indication, said DMA processor controlling the data transfer specified in each of said commands sequentially after the corresponding FIFO indicates a ready status, and notifying said local processor upon completion of the data transfer specified in each of said commands.

67. Apparatus according to claim 65 further comprising an additional FIFO coupled between said CPU bus and said DMA memory, said local processor further having means for transferring data between said CPU and said additional FIFO, and said DMA means being further for transferring data between said interchange bus and said additional FIFO in response to commands issued by said local processor.

68. Network server apparatus for use with a data network and a mass storage device, comprising:

an interface processor unit coupleable to said network and to said mass storage device;

a host processor unit coupleable to said interface processor unit by a second path different from said network;

means in said interface processor unit for satisfying requests from said network to store data from said network on said mass storage device;

means in said interface processor unit for satisfying requests from said network to retrieve data from said mass storage device to said network;

means in said interface processor unit for satisfying requests received from said host processor unit over said second path to store data from said host processor unit on said mass storage device; and

means in said interface processor unit for satisfying requests received from said host processor unit over said second path to retrieve data from said mass storage device to said host processor unit.

69. Apparatus according to claim 68, wherein said interface processor unit comprises:

a network control unit coupleable to said network;

a data control unit coupleable to said mass storage device;

a buffer memory;

means in said network control unit for transmitting to said data control unit requests from said network to store specified storage data from said network on said mass storage device;

means in said network control unit for transmitting said specified storage data from said network to said buffer memory and from said buffer memory to said data control unit;

means in said network control unit for transmitting to said data control unit requests from said network to retrieve specified retrieval data from said mass storage device to said network; and

means in said network control unit for transmitting said specified retrieval data from said data control unit to said buffer memory and from said buffer memory to said network.

70. Apparatus according to claim 69, wherein said data control unit comprises:

a storage processor unit coupleable to said mass storage device;

a file processor unit;

means on said file processor unit for translating said file system level storage requests from said network into requests to store data at specified physical storage locations in said mass storage device;

means on said file processor unit for instructing said storage processor unit to write data from said buffer memory into said specified physical storage locations in said mass storage device;

means on said file processor unit for translating file system level retrieval requests from said network into requests to retrieve data from specified physical retrieval locations in said mass storage device;

means on said file processor unit for instructing said storage processor unit to retrieve data from said specified physical retrieval locations in said mass storage device to said buffer memory if said data from said specified physical locations is not already in said buffer memory; and

means in said storage processor unit for transmitting data between said buffer memory and said mass storage device.

71. Apparatus according to claim 68, for use further with a buffer memory, and wherein said requests from said network to store and retrieve data include file system level storage and retrieval requests respectively, and wherein said interface processor unit comprises:

a storage processor unit coupleable to said mass storage device;

a file processor unit;

means on said file processor unit for translating said file system level storage requests into requests to store data at specified physical storage locations in said mass storage device;

means on said file processor unit for instructing said storage processor unit to write data from said buffer memory into said specified physical storage locations in said mass storage device;

means on said file processor unit for translating said file system level retrieval requests into requests to retrieve data from specified physical retrieval locations in said mass storage device;

means on said file processor unit for instructing said storage processor unit to retrieve data from said specified physical retrieval locations in said mass storage device to said buffer memory if said data from said specified physical locations is not already in said buffer memory; and

means in said storage processor unit for transmitting data between said buffer memory and said mass storage device.

72. A network node for use with a data network and a mass storage device, comprising:

a system buffer memory;

a network control unit coupleable to said network and having direct memory access to said system buffer memory;

a data control unit coupleable to said mass storage device and having direct memory access to said system buffer memory;

first means for satisfying requests from said network to store data from said network on said mass storage device; and

second means for satisfying requests from said network to retrieve data from said mass storage device to said network, said first and second means collectively including

means for transmitting from said network control unit to said system memory bank by direct memory access file data from said network for storage on said mass storage device,

means for transmitting from said system memory bank to said data control unit by direct memory access said file data from said network for storage on said mass storage device,

means for transmitting from said data control unit to said system memory bank by direct memory access file data for retrieval from said mass storage device to said network, and

means for transmitting from said system memory bank to said network control unit said file data for retrieval from said mass storage device to said network;

at least said network control unit including a microprocessor and local instruction storage means distinct from said system buffer memory, all instructions for said microprocessor residing in said local instruction storage means.

73. A network file server for use with a data network and a mass storage device, comprising:

a host processor unit; and

an interface processor unit coupleable to said network, to said mass storage device and, over a second path different from said network, to said host processor unit, said interface processor unit including means for decoding all NFS requests from said network, means for performing all procedures for satisfying said NFS requests, means for encoding any NFS reply messages for return transmission on said network, and means for satisfying file system requests from said host processor unit over said second path.

74. Network server apparatus for use with a data network, comprising:

a network controller coupleable to said network to receive incoming information packets over said network, said incoming information packets including certain packets which contain part or all of a request to said server apparatus, said request being in either a first or a second class of requests to said server apparatus;

a first additional processor;

an interchange bus different from said network and coupled between said network controller and said first additional processor;

means in said network controller for detecting and satisfying requests in said first class of requests contained in said certain incoming information packets, said network controller lacking means in said network controller for satisfying requests in said second class of requests; and

means in said network controller for satisfying requests received over said interchange bus from said first additional processor.

75. Apparatus according to claim 74, wherein said means in said network controller for detecting and satisfying requests in said first class of requests, assembles said requests in said first class of requests into assembled requests before satisfying said requests in said first class of requests.

76. Apparatus according to claim 74, wherein said packets each include a network node destination address, wherein said means in said network controller for detecting and satisfying requests in said first class of requests, assembles said requests in said first class of requests, in a format which omits said network node destination addresses, before satisfying said requests in said first class of requests.

77. Apparatus according to claim 74, wherein said means in said network controller for detecting and satisfying requests in said first class includes means for preparing an outgoing message in response to one of said first class of requests, means for packaging said outgoing message in outgoing information packets suitable

for transmission over said network, and means for transmitting said outgoing information packets over said network.

78. Apparatus according to claim 74, wherein said first class of requests comprises requests for an address of said server apparatus, and wherein said means in said network controller for detecting and satisfying requests in said first class comprises means for preparing a response packet to such an address request and means for transmitting said response packet over said network.

79. Apparatus according to claim 74, for use further with a second data network, said network controller being coupleable further to said second network, wherein said first class of requests comprises requests to route a message to a destinationreachable over said second network, and wherein said means in said network controller for detecting and satisfying requests in said first class comprises means for detecting that one of said certain packets comprises a request to route a message contained in said one of said certain packets to a destination reachable over said second network, and means for transmitting said message over said second network.

80. Apparatus according to claim 79, for use further with a third data network, said network controller further comprising means in said network controller for detecting particular requests in said incoming information packets to route a message contained in said particular requests, to a destination reachable over said third network, said apparatus further comprising:

a second network controller coupled to said interchange bus and coupleable to said third data network;

means for delivering said message contained in said particular requests to said second network controller over said interchange bus; and

means in said second network controller for transmitting said message contained in said particular requests over said third network.

81. Apparatus according to claim 74, for use further with a third data network, said network controller further comprising means in said network controller for detecting particular requests in said incoming information packets to route a message contained in said particular requests, to a destination reachable over said third network, said apparatus further comprising:

a second network controller coupled to said interchange bus and coupleable to said third data network;

means for delivering said message contained in said particular requests to said second network controller over said interchange bus; and

means in said second network controller;for transmitting said message contained in said particular requests over said third network.

82. Apparatus according to claim 74, for use further with amass storage device, wherein said first additional processor comprises a data control unit coupleable to said mass storage device, wherein said second class of requests comprises remote calls to procedures for managing a file system in said mass storage device, and wherein said means in said first additional processor for further processing said assembled requests in said second class of requests comprises means for executing file system procedures on said mass storage device in response to said assembled requests.

83. Apparatus according to claim 82, wherein said file system procedures include a read procedure for reading data from said mass storage device,

said means in said first additional processor for further processing said assembled requests including means for reading data from a specified location in said mass storage device in response to a remote call to said read procedure,

said apparatus further including means for delivering said data to said network controller,

said network controller further comprising means on said network controller for packaging said data in outgoing information packets suitable for transmission over said network, and means for transmitting said outgoing information packets over said network.

84. Apparatus according to claim 83, wherein said means for delivering comprises:

a system buffer memory coupled to said interchange bus;

means in said data control unit for transferring said data over said interchange bus into said buffer memory; and

means in said network controller for transferring said data over said interchange bus from said system buffer memory to said network controller.

85. Apparatus according to claim 82, wherein said file system procedures include a read procedure for reading a specified number of bytes of data from said mass storage device beginning at an address specified in logical terms including a file system ID and a file ID, said means for executing file system procedures comprising:

means for converting the logical address specified in a remote call to said read procedure to a physical address; and

means for reading data from said physical address in said mass storage device.

86. Apparatus according to claim 85, wherein said mass storage device comprises a disk drive having a numbered tracks and sectors, wherein said logical address specifies said file system ID, said file ID, and a byte offset, and wherein said physical address specifies a corresponding track and sector number.

87. Apparatus according to claim 82, wherein said file system procedures include a read procedure for reading a specified number of bytes of data from said mass storage device beginning at an address specified in logical terms including a file system ID and a file ID,

said data control unit comprising a file processor coupled to said interchange bus and a storage processor coupled to said interchange bus and coupleable to said mass storage device,

said file processor comprising means for converting the logical address specified in a remote call to said read procedure to a physical address,

said apparatus further comprising means for delivering said physical address to said storage processor,

said storage processor comprising means for reading data from said physical address in said mass storage device and for transferring said data over said interchange bus into said buffer memory; and

means in said network controller for transferring said data over said interchange bus from said system buffer memory to said network controller.

88. Apparatus according to claim 82, wherein said file system procedures include a write procedure for writing data contained in an assembled request, to said mass storage device,

said means in said first additional processor for further processing said assembled requests including means for writing said data to a specified location in said mass storage device in response to a remote call to said read procedure.

89. Apparatus according to claim 74, wherein said network controller comprises:

a microprocessor;

a local instruction memory containing local instruction code;

a local bus coupled between said microprocessor and said local instruction memory;

bus interface means for interfacing said microprocessor with said interchange bus at times determined by said microprocessor in response to said local instruction code; and

network interface means for interfacing said microprocessor with said data network,

said local instruction memory including all instruction code necessary for said microprocessor to perform said function of detecting and satisfying requests in said first class of requests.

90. Network server apparatus for use with a data network, comprising:

a network controller coupleable to said network to receive incoming information packets over said network, said incoming information packets including certain packets which contain part or all of a message to said server apparatus, said message being in either a first or a second class of messages to said server apparatus, said messages in said first class of messages including certain messages containing requests;

a host computer;

an interchange bus different from said network and coupled between said network controller and said host computer;

means in said network controller for detecting and satisfying said requests in said first class of messages; and

means for satisfying requests received over said interchange bus from said host computer.

91. Apparatus according to claim 90, wherein said means in said network controller for detecting and satisfying requests in said first class includes means for preparing an outgoing message in response to one of said requests in said first class of messages, means for packaging said outgoing message in outgoing information packets suitable for transmission over said network, and means for transmitting said outgoing information packets over said network.

92. Apparatus according to claim 90, for use further with a second data network, said network controller being coupleable further to said second network, wherein said first class of messages comprises messages to be routed to a destination reachable over said second network, and wherein said means in said network controller for detecting and satisfying requests in said first class comprises means for detecting that one of said certain packets includes a request to route a message contained in said one of said certain packets to a destination reachable over said second network, and means for transmitting said message over said second network.

93. Apparatus according to claim 90, for use further with a third data network, said network controller further comprising means in said network controller for detecting particular messages in said incoming information packets to be routed to a destination reachable over said third network, said apparatus further comprising:

a second network controller coupled to said interchange bus and coupleable to said third data network;

means for delivering said particular messages to said second network controller over said interchange bus, substantially without involving said host computer; and

means in said second network controller for transmitting said message contained in said particular requests over said third network, substantially without involving said host computer.

94. Apparatus according to claim 90, for use further with a mass storage device, further comprising a data control unit coupleable to said mass storage device,

said network controller further comprising means in said network controller for detecting ones of said incoming information packets containing remote calls to procedures for managing a file system in said mass storage device, and means in said network controller for assembling said remote calls from said incoming packets into assembled calls, substantially without involving said host computer,

said apparatus further comprising means for delivering said assembled file system calls to said data control unit over said interchange bus substantially without involving said host computer, and

said data control unit comprising means in said data control unit for executing file system procedures on said mass storage device in response to said assembled file system calls, substantially without involving said host computer.

95. Apparatus according to claim 90, wherein said network controller comprises:

a microprocessor;

a local instruction memory containing local instruction code;

a local bus coupled between said microprocessor and said local instruction memory;

bus interface means for interfacing said microprocessor with said interchange bus at times determined by said microprocessor in response to said local instruction code; and

network interface means for interfacing said microprocessor with said data network,

said local instruction memory including all instruction code necessary for said microprocessor to perform said function of detecting and satisfying requests in said first class of requests.

96. A network file server for use with a data network and a mass storage device, comprising:

means for decoding NFS requests from said network;

means for performing procedures for satisfying said NFS requests, including accessing said mass storage device if required; and

means for encoding any NFS reply messages for return transmission on said network,

said network file server for satisfying only-NFS requests from said network.

97. A network file server for use with a data network and a mass storage device, said network file server including a first unit comprising:

means for decoding file system requests from said network;

means for performing procedures for satisfying said file system requests, including accessing said mass storage device if required; and

means for encoding any file system reply messages for return transmission on said network,

said first unit for executing any programs other than programs which make calls to any general purpose operating system.

98. A network file server according to claim 97, further including a second unit comprising means for executing programs which make calls to a general purpose operating system.

99. A network file server according to claim 97, wherein said file system requests from said network comprise NFS requests.

100. A network file server for use with a data network and a mass storage device, said network file server including a first unit comprising:

means for decoding file system requests from said network;

means for performing procedures for satisfying said file system requests, including accessing said mass storage device if required; and

means for encoding any file system reply messages for return transmission on said network,

said first unit for executing any application programs other than user-provided application programs on said first unit.

101. A network file server according to claim 100, further including a second unit running a user-provided application program.

102. A network file server according to claim 100, wherein said file system requests from said network comprise NFS requests.

103. A network file server for use with a data network and a mass storage device, said network file server comprising:

a network control module, including a network interface coupled to receive file system requests from said network;

a file system control module, including a mass storage device interface coupled to said mass storage device; and

a communication path coupled directly between said network control module and said file system control module, said communication path carrying file retrieval

requests prepared by said network control module in response to received file system requests to retrieve specified retrieval data from said mass storage device,

said file system control module retrieving said specified retrieval data from said mass storage device in response to said file retrieval requests and returning said specified retrieval data to said network control module, and

said network control module preparing reply messages containing said specified retrieval data from said file system control module for return transmission on said network.

104. A network file server according to claim 103, wherein said file system control module returns said specified retrieval data directly to said network control module.

105. A network file server according to claim 103, wherein said network control module further prepares file storage requests in response to received file system requests to store specified storage data on said mass storage device, said network control module communicating said file storage requests to said file system control module,

and wherein said file system control module further stores said specified storage data on said mass storage device in response to said file storage requests.

106. A network file server according to claim 105, wherein said file storage requests are communicated to said file system control module via said communication path.

107. A network file server according to claim 103, wherein said received file system requests to retrieve specified retrieval data comprise NFS requests.

108. A method for processing requests from a data network, for use by a network file server including a network control module coupled to receive file system requests from said network and a file system control module coupled to said mass storage device, comprising the steps of:

said network control module preparing file retrieval requests in response to received file system requests to retrieve specified retrieval data from said mass storage device;

said network control module communicating said file retrieval requests directly to said file system control module;

said file system control module retrieving said specified retrieval data from said mass storage device in response to said file retrieval requests and returning said specified retrieval data to said network control module; and

said network control module preparing reply messages containing said specified retrieval data from said file system control module for return transmission on said network.

109. A method according to claim 108, wherein said file system control module returns said specified retrieval data directly to said network control module.

110. A method according to claim 108, further comprising the steps of:

said network control module preparing file storage requests in response to received file system requests to store specified storage data on said mass storage device

said network control module communicating said file storage requests to said file system control module; and

said file system control module storing said specified storage data on said mass storage device in response to said file storage requests.

111. A method according to claim 110, wherein said file storage requests are communicated directly to said file system control module.

112. A method according to claim 108, wherein said received file system requests to retrieve specified retrieval data comprise NFS requests.

113. Apparatus for use with a data network and a mass storage device, comprising the combination of first and second processing units,

said first processing unit processing all requests from said network which are addressed to said apparatus and which are within a predefined non-NFS class of requests, and

said second processing unit being coupleable to said network and to said mass storage device and decoding all NFS requests from said network which are addressed to said apparatus, performing procedures for satisfying said NFS requests, and encoding NFS reply messages for return transmission on said network, said second processing unit not satisfying any of said requests from said network which are addressed to said apparatus and which are within said predefined non-NFS class of requests.

114. Apparatus according to claim 113, wherein said predefined non-NFS class of requests includes all requests to perform client-defined procedures on said combination.

115. Apparatus according to claim 113, wherein said first processing unit includes a UNIX kernel and wherein said second processing unit does not include a UNIX kernel.

116. Apparatus according to claim 113, wherein said second processing unit comprises:

a network control unit coupleable to said network;

a data control unit coupleable to said mass storage device;

a buffer memory;

means in said network control unit for decoding said NFS requests and for encoding said NFS reply messages;

means for transmitting to said data control unit requests responsive to NFS requests from said network to store specified data from said network on said mass storage device;

means for transmitting said specified storage data from said network to said buffer memory and from said buffer memory to said data control unit;

means for transmitting to said data control unit requests responsive to NFS requests from said network to retrieve specified retrieval data from said mass storage device to said network;

means for transmitting said specified retrieval data from said data control unit to said buffer memory and from said buffer memory to said network.

117. A network file server for use with a data network and a mass storage device, said network file server including a first unit comprising:

means for decoding NFS requests from said network;

means for performing procedures for satisfying said NFS requests, including accessing said mass storage device if required; and

means for encoding any NFS reply messages for return transmission on said network,

said first unit for executing any programs which make UNIX operating system calls.

118. A network file server according to claim 117, further including a second unit comprising means for executing programs which make UNIX operating system calls.

119. A network file server for use with a data network and a mass storage device, said network file server including a first unit comprising:

means for decoding NFS requests from said network;

means for performing procedures for satisfying said NFS requests, including accessing said mass storage device if required; and

means for encoding any NFS reply messages for return transmission on said network,

said first unit lacking any UNIX kernel.

120. A network file server according to claim 119, further including a second unit running a UNIX kernel.

121. A network file server unit for use with a data network and a mass storage device, said network file server unit comprising:

means for decoding NFS requests from said network;

means for performing procedures for satisfying said NFS requests, including accessing said mass storage device if required; and

means for encoding any NFS reply messages for return transmission on said network,

said first unit lacking any UNIX application programs running on said first unit.

122. A network file server according to claim 121, further including a second unit running a UNIX application program.

123. Apparatus for use with a data network and a mass storage device, comprising the combination of first and second processing units,

said first processing unit being coupled to said network and performing procedures for satisfying requests from said network which are within a predefined non-NFS class of requests, and

said second processing unit being coupled to said network and to said mass storage device and decoding NFS requests from said network, performing procedures for satisfying said NFS requests, and encoding NFS reply messages for return transmission on said network, said second processing unit not satisfying any requests from said network which are within said predefined non-NFS class of requests.

124. Apparatus according to claim 123, wherein said predefined non-NFS class of requests includes a predefined set of remote procedure calls.

125. Apparatus according to claim 123, wherein said first processing unit includes a general purpose operating system and wherein said second processing unit does not include a general purpose operating system.

126. Apparatus according to claim 123, wherein said second processing unit comprises:

a network control unit coupleable to said network;

a data control unit coupleable to said mass storage device;

a buffer memory;

means in said network control unit for decoding said NFS requests and for encoding said NFS reply messages;

means for transmitting to said data control unit requests responsive to NFS requests from said network to store specified data from said network on said mass storage device;

means for transmitting said specified storage data from said network to said buffer memory and from said buffer memory to said data control unit;

means for transmitting to said data control unit requests responsive to NFS requests from said network to retrieve specified retrieval data from said mass storage device to said network;

means for transmitting said specified retrieval data from said data control unit to said buffer memory and from said buffer memory to said network.

127. A network file server for use with a data network and a mass storage device, said network file server including a first unit comprising:

means for decoding NFS requests from said network;

means for performing procedures for satisfying said NFS requests, including accessing said mass storage device if required; and

means for encoding any NFS reply messages for return transmission on said network,

said first unit lacking means in said first unit for executing any programs which make calls to any general purpose operating system.

128. A network file server according to claim 127, further including a second unit comprising means for executing programs which make calls to a general purpose operating system.

129. A network file server according to claim 128, wherein said first unit lacks means in said first unit for executing any programs which make calls to a UNIX operating system, and wherein said second unit comprises means for executing programs which make calls to a UNIX operating system.

130. A network file server for use with a data network and a mass storage device, said network file server including a first unit comprising:

means for decoding NFS requests from said network;

means for performing procedures for satisfying said NFS requests, including accessing said mass storage device if required; and

means for encoding any NFS reply messages for return transmission on said network,

said first unit lacking means to execute any user-provided application programs on said first unit.

131. A network file server according to claim 130, further including a second unit running a user-provided application program.

132. A network file server for use with a data network and a mass storage device, said network file server comprising;

a network control module, including a network interface coupled to receive NFS requests from said network;

a file system control module, including a mass storage device interface coupled to said mass storage device; and

a communication path coupled directly between said network control module and said file system control module, said communication path carrying file retrieval requests prepared by said network control module in response to received NFS requests to retrieve specified retrieval data from said mass storage device,

said file system control module retrieving said specified retrieval data from said mass storage device in response to said file retrieval requests and returning said specified retrieval data to said network control module, and

said network control module preparing reply messages containing said specified retrieval data from said file system control module for return transmission on said network.

133. A network file server according to claim 132, wherein said file system control module returns said specified retrieval data directly to said network control module.

134. A network file server according to claim 132, wherein said network control module further prepares file storage requests in response to received NFS requests to store specified storage data on said mass storage device, said network control module communicating said file storage requests to said file system control module,

and wherein said file system control module further stores said specified storage data on said mass storage device in response to said file storage requests.

135. A network file server according to claim 134, wherein said file storage requests are communicated to said file system control module via said communication path.

136. A method for processing requests from a data network, for use by a network file server including a network control module coupled to receive NFS requests from said network and a file system control module coupled to said mass storage device, comprising the steps of:

said network control module preparing file retrieval requests in response to received NFS requests to retrieve specified retrieval data from said mass storage device;

said network control module communicating said file retrieval requests directly to said file system control module;

said file system control module retrieving said specified retrieval data from said mass storage device in response to said file retrieval requests and returning said specified retrieval data to said network control module; and

said network control module preparing reply messages containing said specified retrieval data from said file system control module for return transmission on said network.

137. A method according to claim 136, wherein said file system control module returns said specified retrieval data directly to said network control module.

138. A method according to claim 136, further comprising the steps of:

said network control module preparing file storage requests in response to received NFS requests to store specified storage data on said mass storage device

said network control module communicating said file storage requests to said file system control module; and

said file system control module storing said specified storage data on said mass storage device in response to said file storage requests.

139. A method according to claim 138, wherein said file storage requests are communicated directly to said file system control module.

140. A network file server for use with a network and at least one mass storage device, said network file server including:

a network interface, coupleable to said network, for receiving NFS requests from said network;

a file server processor, coupled to the network interface and coupleable to said at least one mass storage device, for executing essentially only NFS requests from said network interface, including accessing said at least one mass storage device if required.

141. A network file server for use with an Ethernet network and at least one mass storage device, said network file server including:

a network interface, coupleable to said Ethernet network, for receiving from said Ethernet network packets containing NFS requests to read data from or write data to said at least one mass storage device;

a parallel bus;

a dedicated file server processor, coupled to said network interface by means of said parallel bus, and coupleable to said at least one mass storage device, for executing essentially only NFS requests from said network interface, including accessing said at least one mass storage device if required.

142. A network file server for use with an Ethernet network, said network file server including:

a parallel bus;

at least one mass storage device coupled to said parallel bus;

a network interface, coupleable to said Ethernet network, and coupled to said parallel bus, for receiving from said Ethernet network packets containing NFS requests to read data from or write data to said at least one mass storage device;

a dedicated file server processor, coupled to said network interface and to said at least one mass storage device by means of said parallel bus, for executing essentially only NFS requests from said network interface, including accessing said at least one mass storage device if required.

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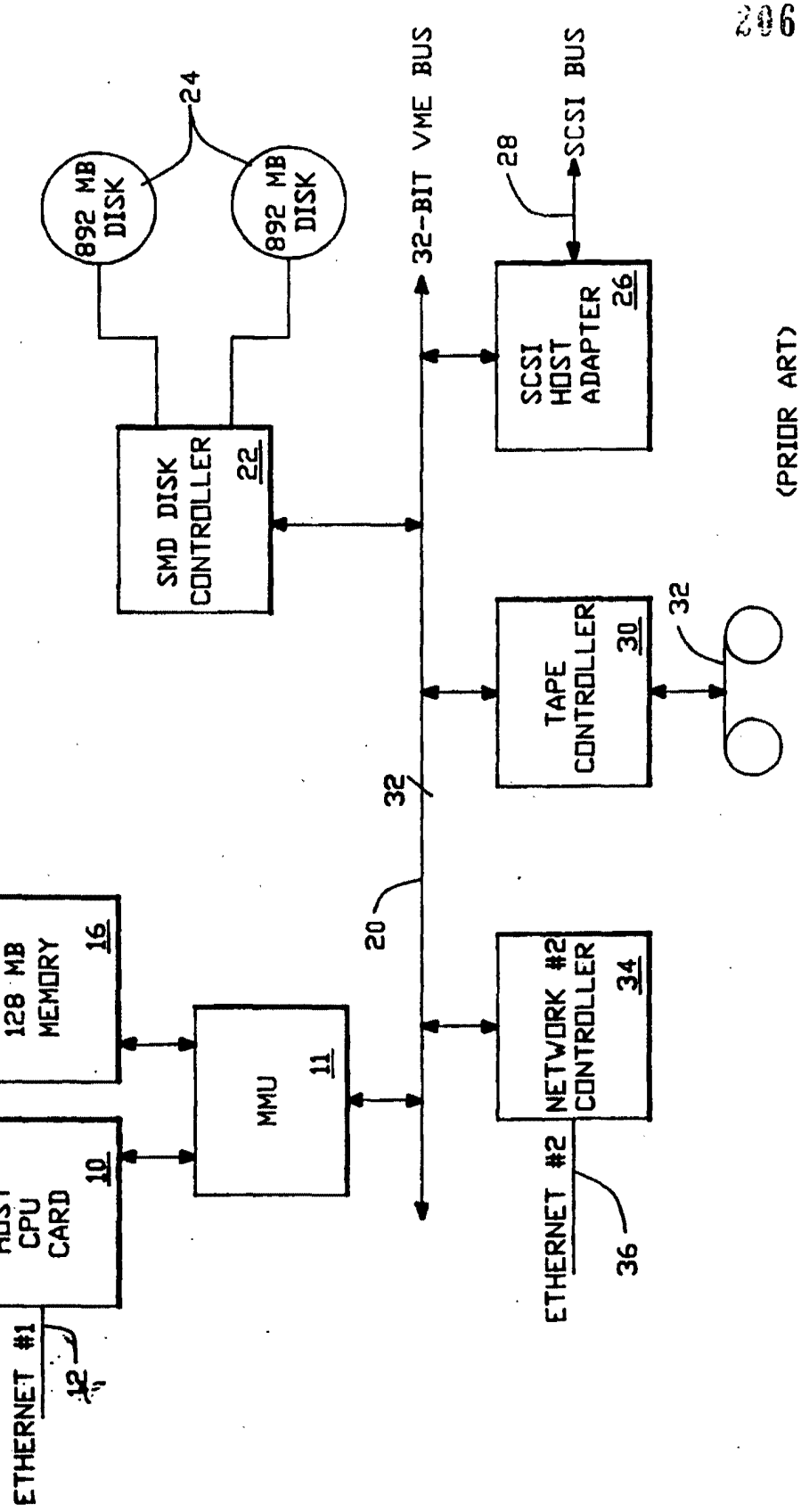


(PRIOR ART)

FIG.-1

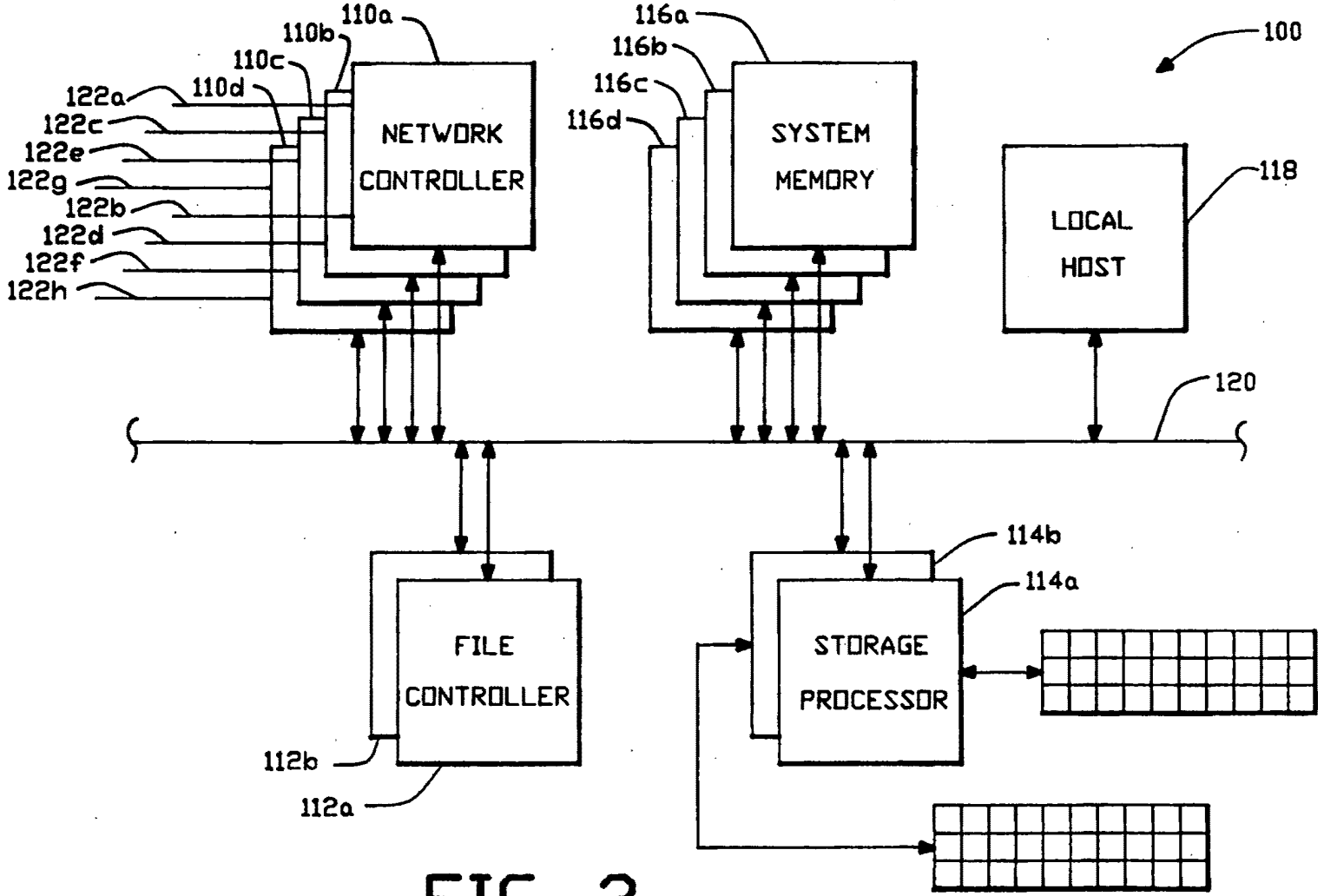

110a
110b
110c
110d
122a
122c
122e
122g
122b
122d
122f
122h
NETWORK CONTROLLER
116a
116b
116c
116d
SYSTEM MEMORY
100
LOCAL HOST
118
120
FILE CONTROLLER
112b
112a
114b
114a
STORAGE PROCESSOR

FIG.-2

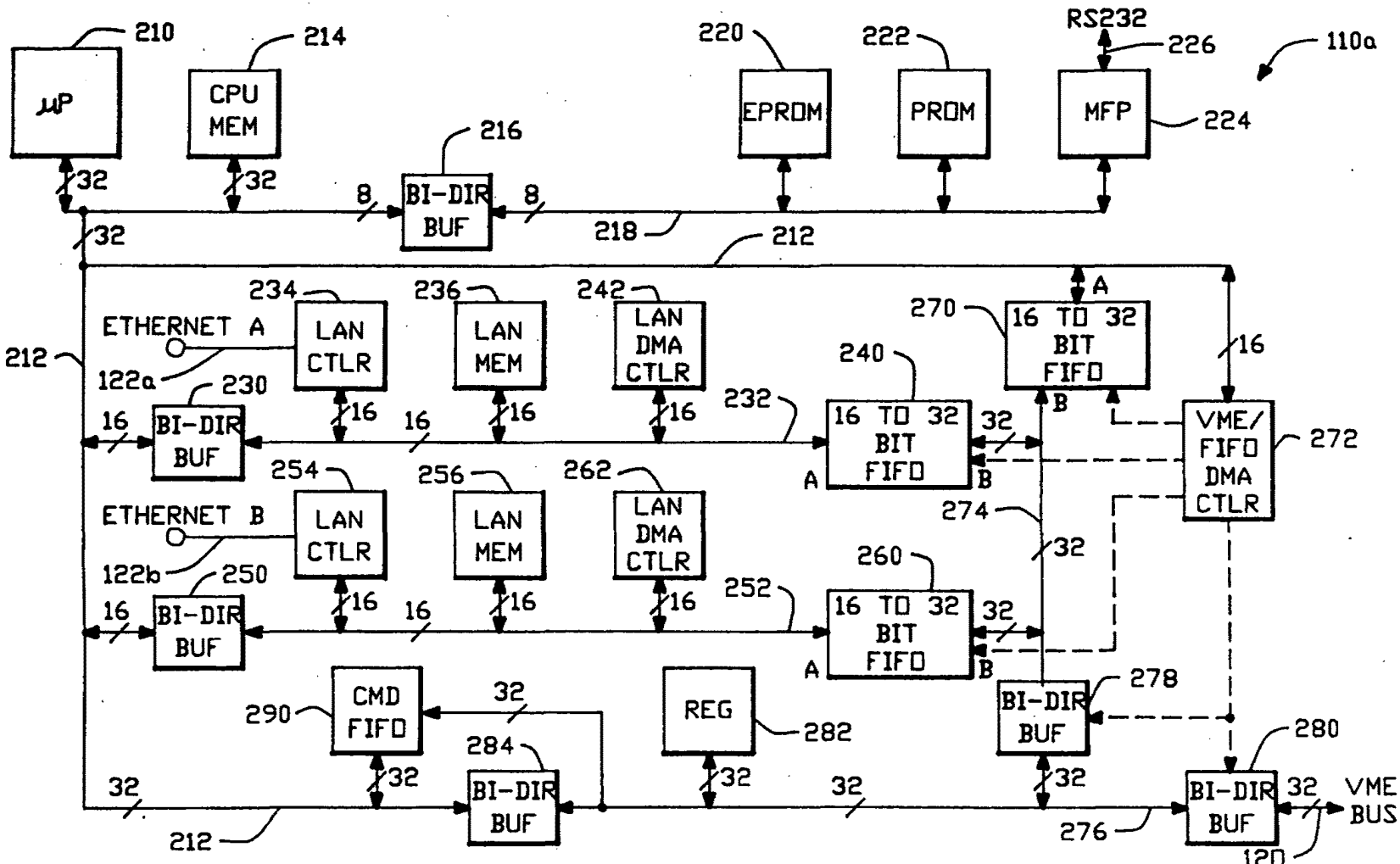


FIG.-3 (NETWORK CONTROLLER)

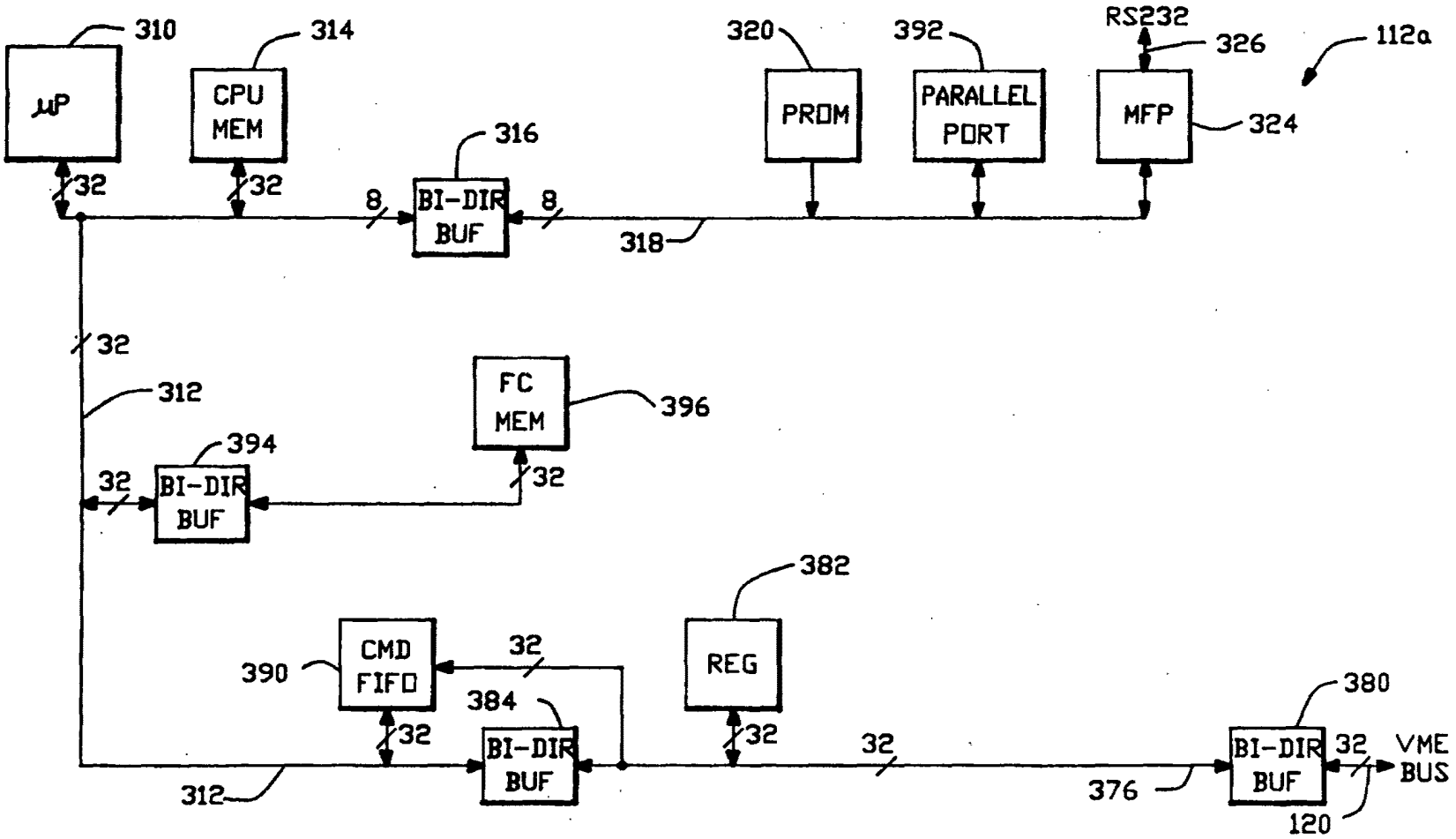
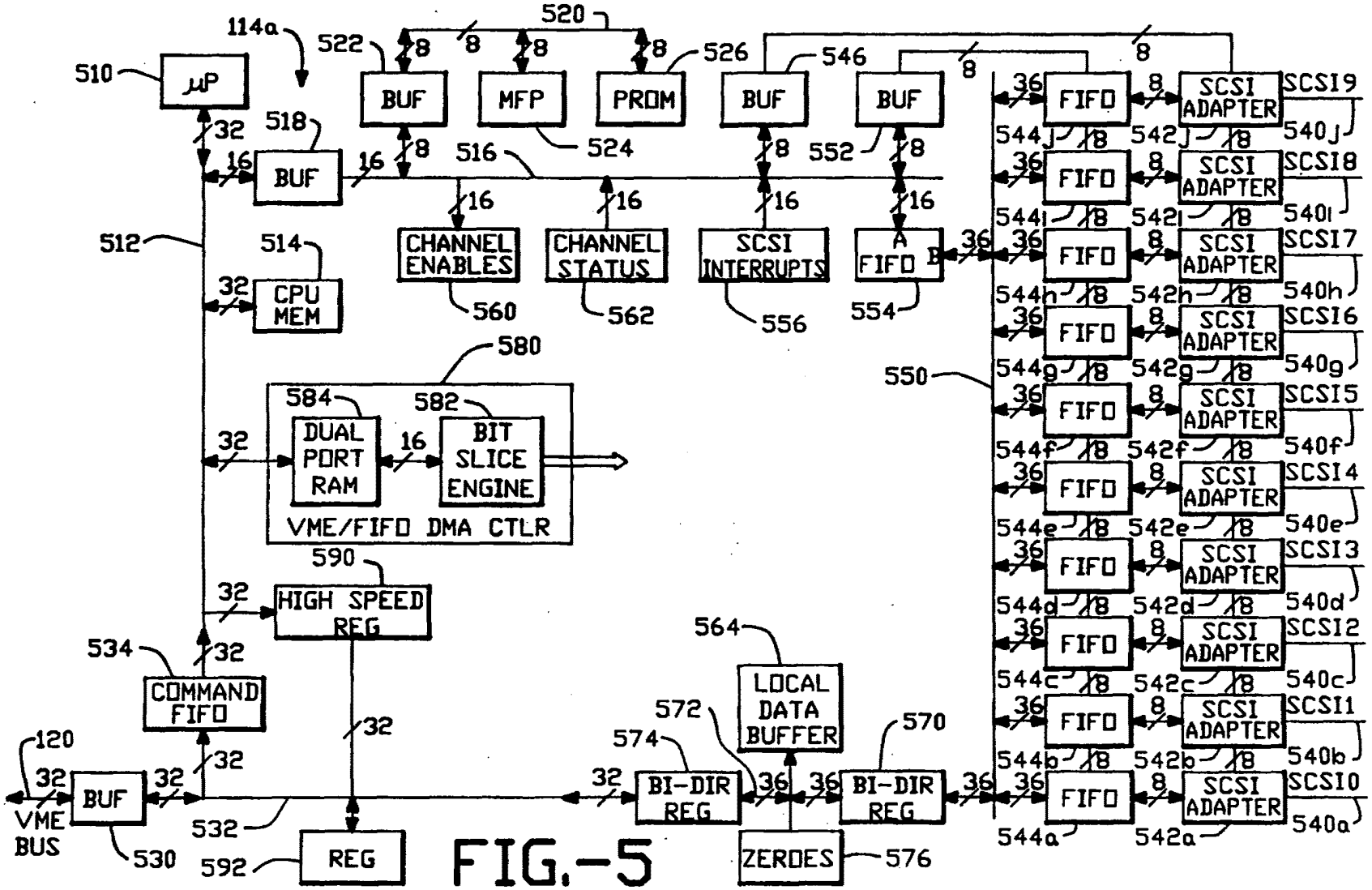


FIG.-4 (FILE CONTROLLER)


114a
520
522
526
546
510
μP
BUF
MFP
PROM
BUF
BUF
518
516
524
552
512
514
CHANNEL ENABLES
CHANNEL STATUS
SCSI INTERRUPTS
A FIFO B
CPU MEM
560
562
556
554
580
584
582
DUAL PORT RAM
BIT SLICE ENGINE
VME/FIFO DMA CTLR
550
590
HIGH SPEED REG
564
534
COMMAND FIFO
LOCAL DATA BUFFER
572
574
570
120
VME BUS
BUF
BI-DIR REG
BI-DIR REG
532
530
592
REG
ZEROES
576
FIFO
SCSI ADAPTER
SCSI19
SCSI18
SCSI17
SCSI16
SCSI15
SCSI14
SCSI13
SCSI12
SCSI11
SCSI10
540j
540i
540h
540g
540f
540e
540d
540c
540b
540a
542j
542i
542h
542g
542f
542e
542d
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544h
544g
544f
544e
544d
544c
544b
544a

FIG.-5

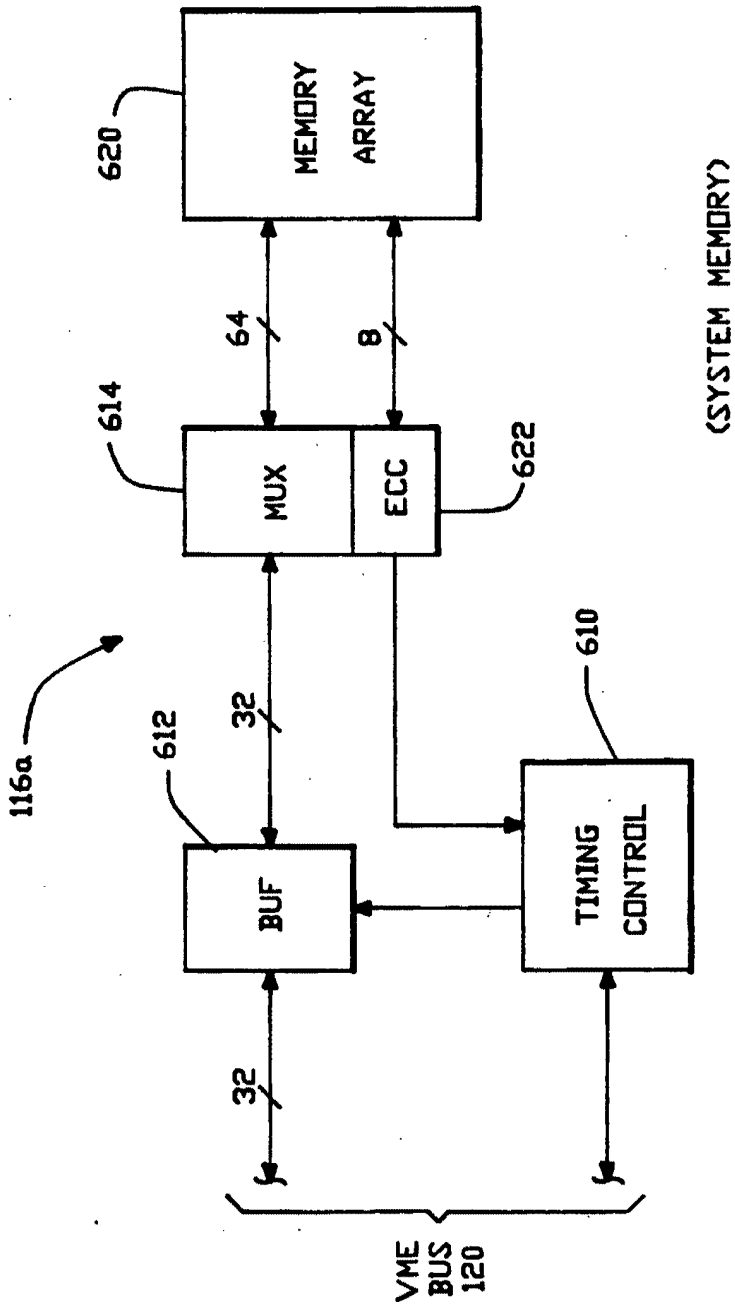

FIG.-6

WO 91/03788 PCT/US90/04711

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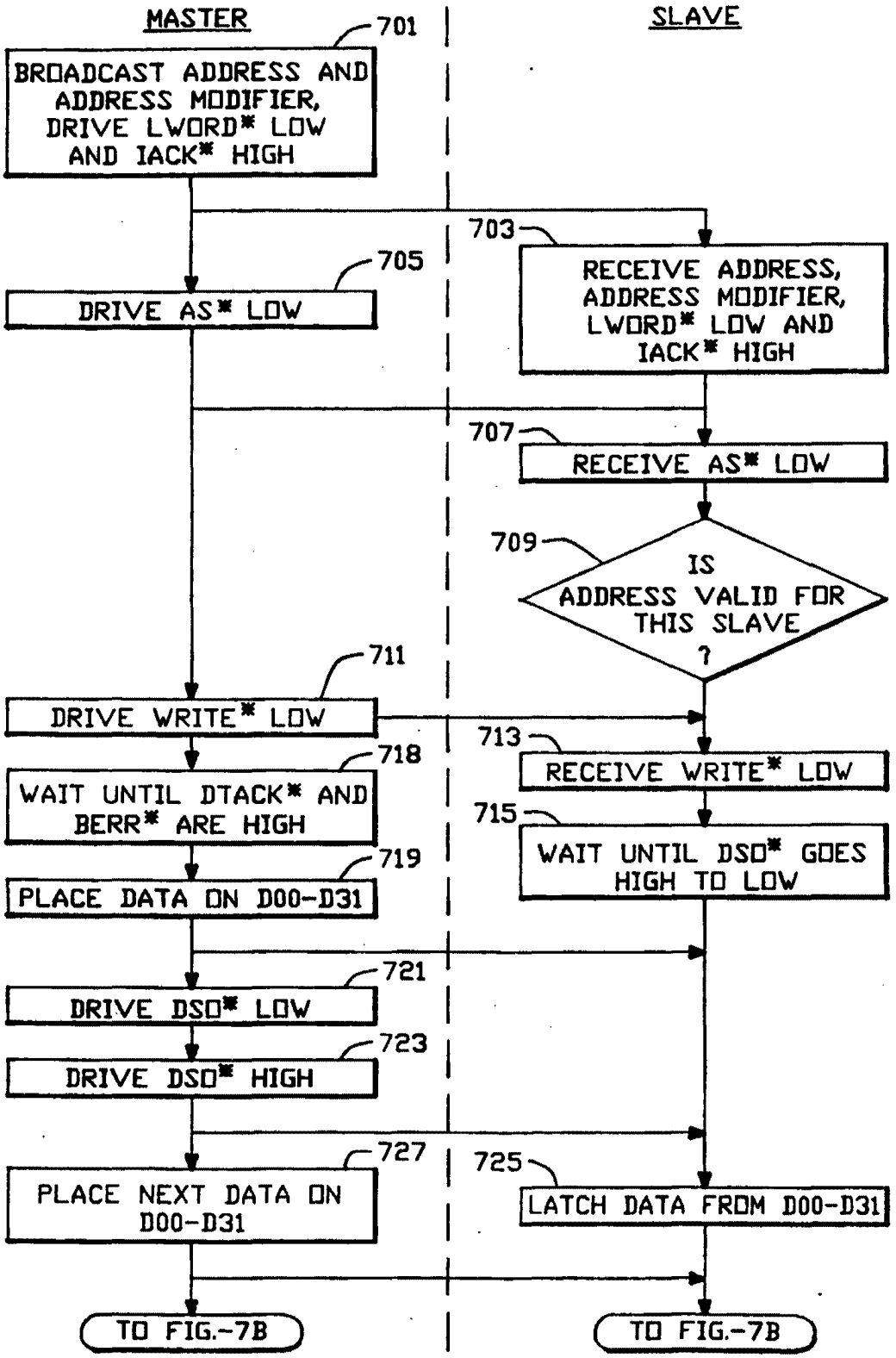

FIG.-7A

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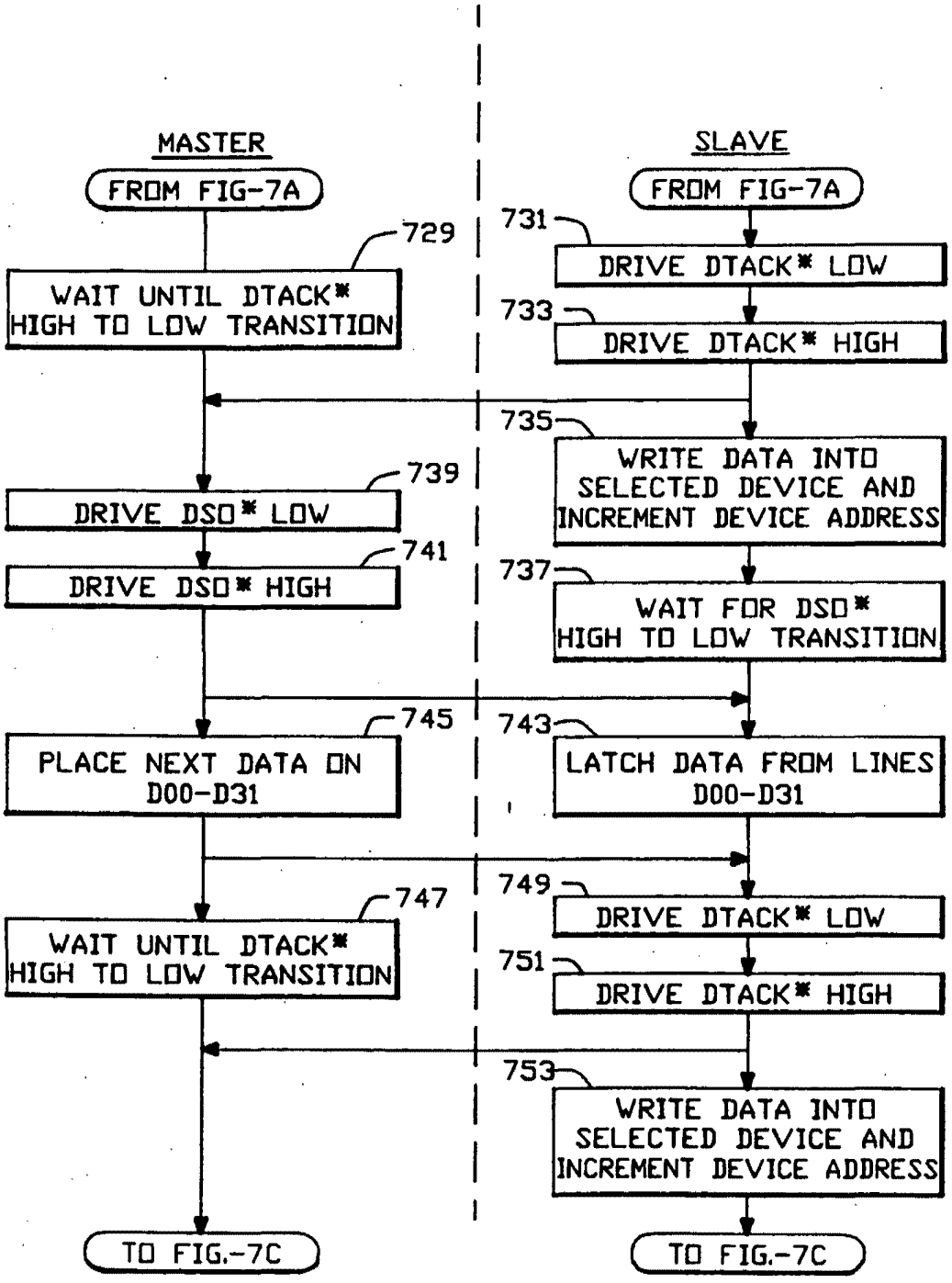

FIG.-7B

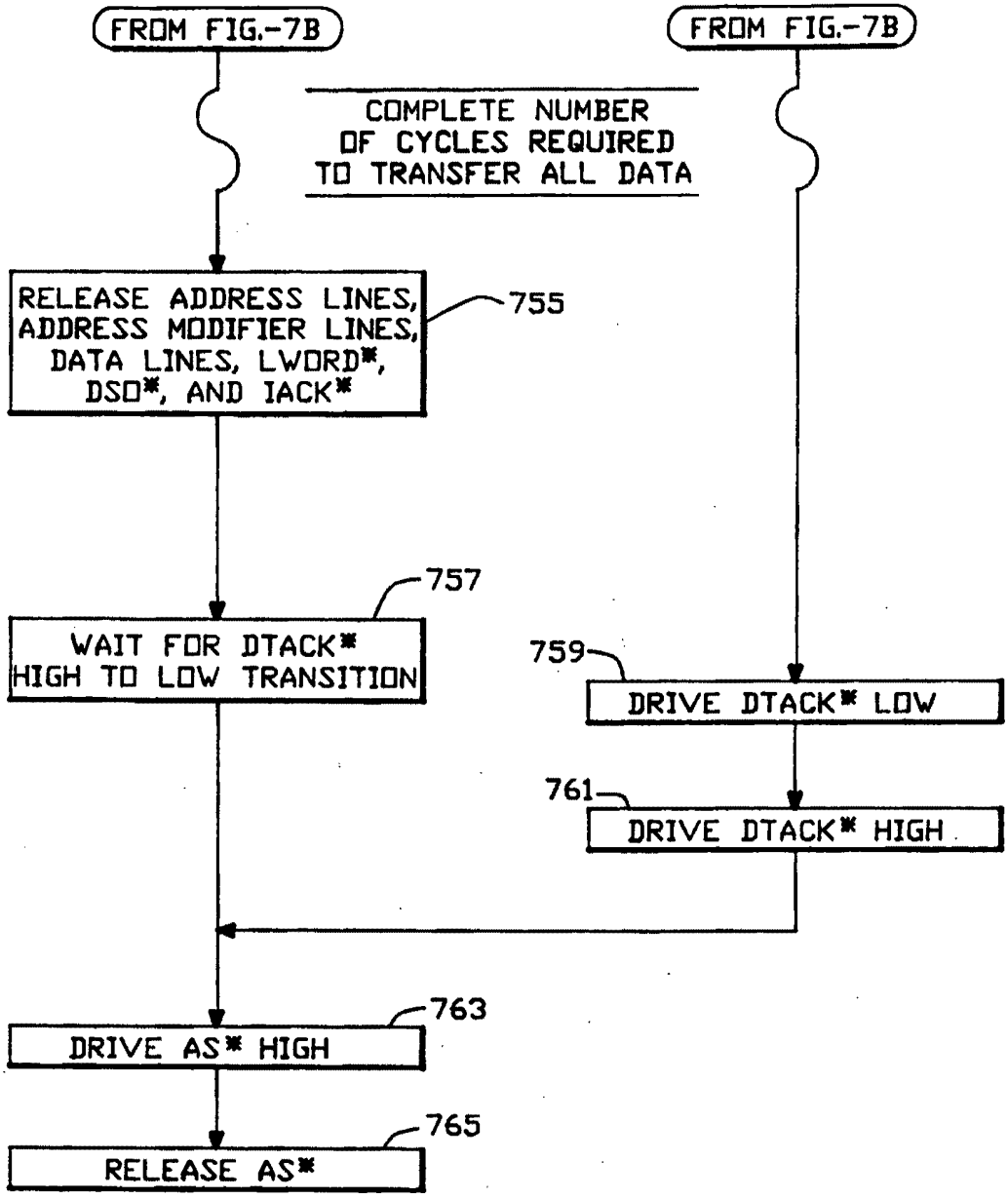
FROM FIG.-7B
FROM FIG.-7B
COMPLETE NUMBER OF CYCLES REQUIRED TO TRANSFER ALL DATA
RELEASE ADDRESS LINES, ADDRESS MODIFIER LINES, DATA LINES, LWORD*, DSO*, AND IACK*
755
757
WAIT FOR DTACK* HIGH TO LOW TRANSITION
759
DRIVE DTACK* LOW
761
DRIVE DTACK* HIGH
763
DRIVE AS* HIGH
765
RELEASE AS*

FIG.-7C

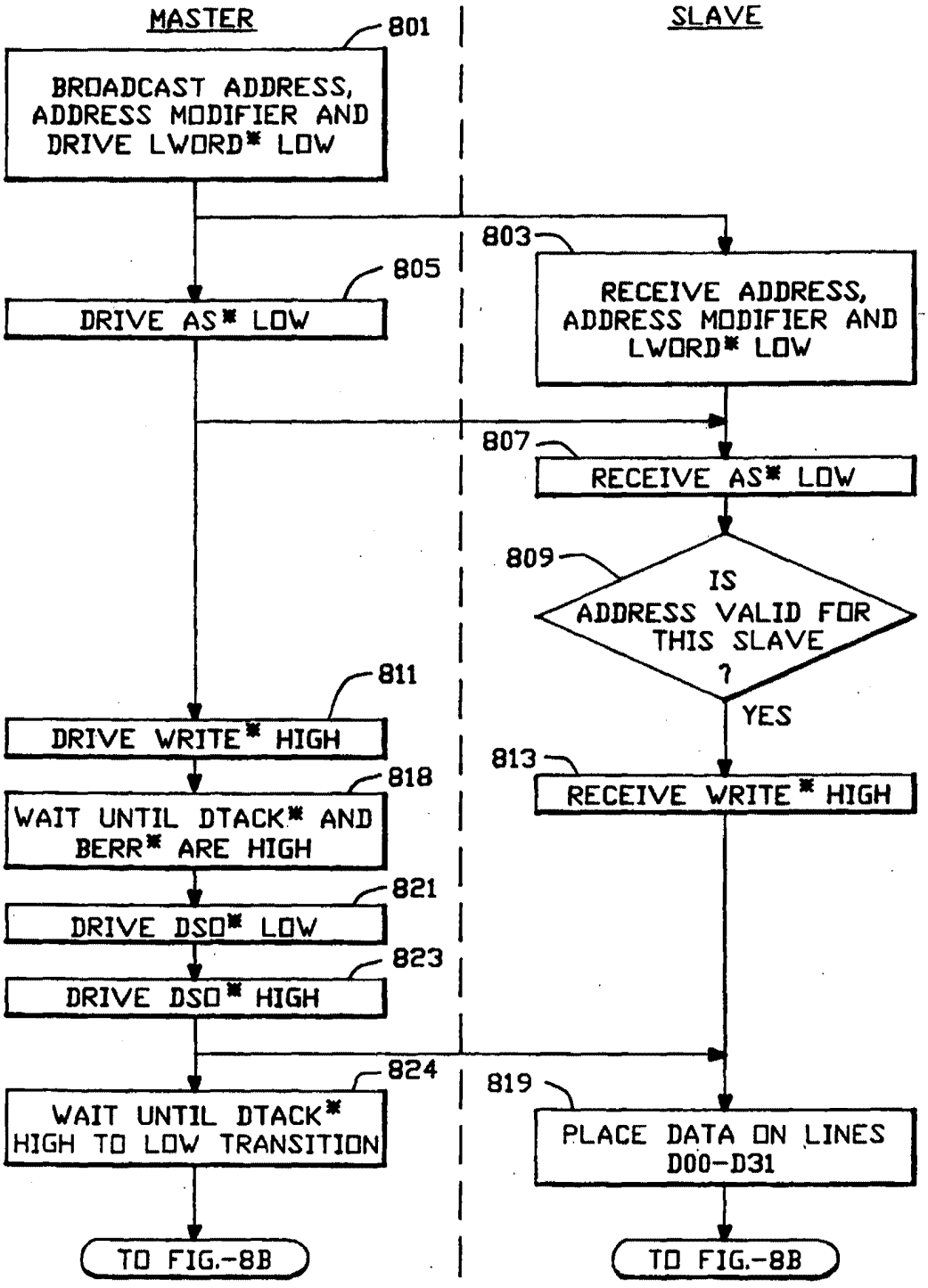
MASTER
SLAVE
801
BROADCAST ADDRESS, ADDRESS MODIFIER AND DRIVE LWORD* LOW
803
RECEIVE ADDRESS, ADDRESS MODIFIER AND LWORD* LOW
805
DRIVE AS* LOW
807
RECEIVE AS* LOW
809
IS ADDRESS VALID FOR THIS SLAVE ?
YES
811
DRIVE WRITE* HIGH
813
RECEIVE WRITE* HIGH
818
WAIT UNTIL DTACK* AND BERR* ARE HIGH
821
DRIVE DS0* LOW
823
DRIVE DS0* HIGH
824
WAIT UNTIL DTACK* HIGH TO LOW TRANSITION
819
PLACE DATA ON LINES D00-D31
TO FIG.-8B
TO FIG.-8B

FIG.-8A

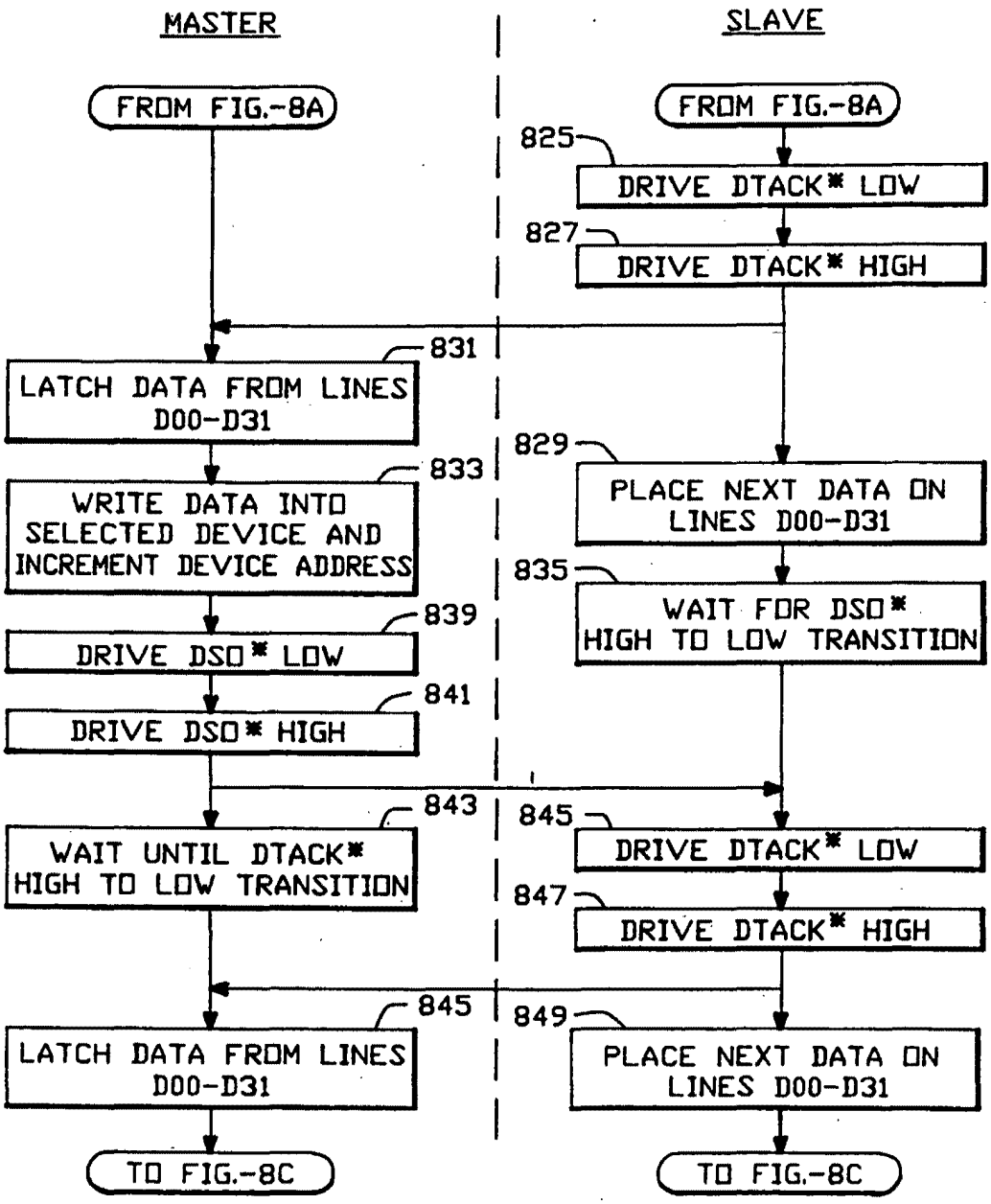
MASTER
SLAVE
FROM FIG.-8A
FROM FIG.-8A
825
DRIVE DTACK* LOW
827
DRIVE DTACK* HIGH
831
LATCH DATA FROM LINES D00-D31
829
PLACE NEXT DATA ON LINES D00-D31
833
WRITE DATA INTO SELECTED DEVICE AND INCREMENT DEVICE ADDRESS
835
WAIT FOR DS0* HIGH TO LOW TRANSITION
839
DRIVE DS0* LOW
841
DRIVE DS0* HIGH
843
WAIT UNTIL DTACK* HIGH TO LOW TRANSITION
845
DRIVE DTACK* LOW
847
DRIVE DTACK* HIGH
845
LATCH DATA FROM LINES D00-D31
849
PLACE NEXT DATA ON LINES D00-D31
TO FIG.-8C
TO FIG.-8C

FIG.-8B

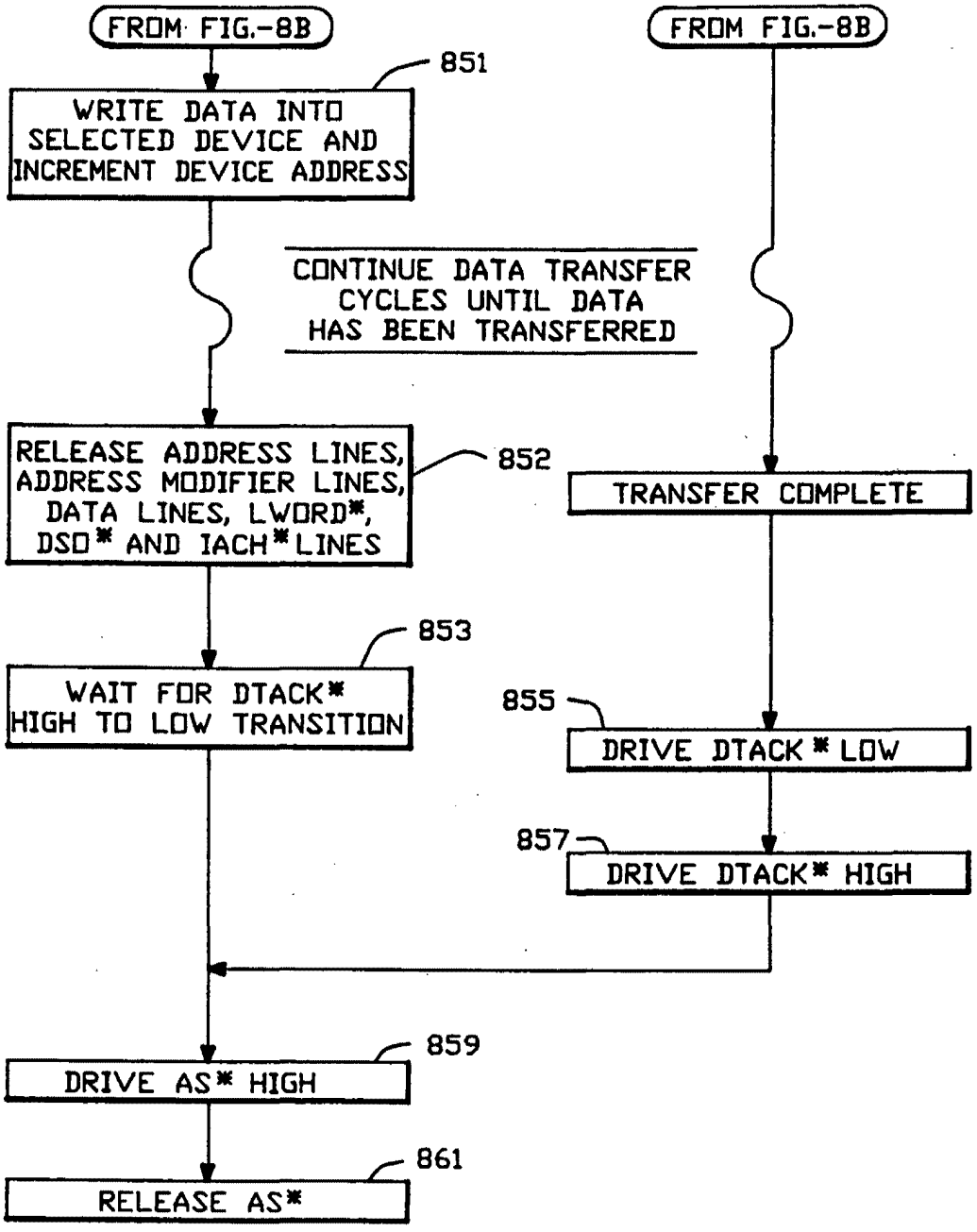
FROM FIG.-8B
FROM FIG.-8B
851
WRITE DATA INTO SELECTED DEVICE AND INCREMENT DEVICE ADDRESS
CONTINUE DATA TRANSFER CYCLES UNTIL DATA HAS BEEN TRANSFERRED
RELEASE ADDRESS LINES, ADDRESS MODIFIER LINES, DATA LINES, LWORD*, DSO* AND IACH* LINES
852
TRANSFER COMPLETE
853
WAIT FOR DTACK* HIGH TO LOW TRANSITION
855
DRIVE DTACK* LOW
857
DRIVE DTACK* HIGH
859
DRIVE AS* HIGH
861
RELEASE AS*

FIG.-8C

INFORMATION DISCLOSURE STATEMENT				Application Number	12/690,592
				Filing or 371 (c) Date:	January 20, 2010
				First Named Inventor	Geoffrey B. Hoese
				Group Art Unit	2182
				Examiner Name	Unknown
Sheet	1	of	1	Atty Docket Number	CROSS1120-33

NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published	T^2
	C171	American National Standard for Information Systems: Fibre Channel -- Cross-Point Switch Fabric Topology (FC-XS); X3T11/Project 959D/Rev 1.30. 114 pgs.	6/17/1994

Examiner Signature		Date Considered	

Electronic Acknowledgement Receipt

EFS ID:	7781273
Application Number:	12690592
International Application Number:	
Confirmation Number:	8115
Title of Invention:	STORAGE ROUTER AND METHOD FOR PROVIDING VIRTUAL LOCAL STORAGE
First Named Inventor/Applicant Name:	Geoffrey B. Hoese
Customer Number:	44654
Filer:	John L. Adair/Betty Caldwell
Filer Authorized By:	John L. Adair
Attorney Docket Number:	CROSS1120-33
Receipt Date:	09-JUN-2010
Filing Date:	20-JAN-2010
Time Stamp:	17:18:03
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		CROSS1120-33_IDS_06-09-10.pdf	115678 51aa5fa515cd40221bf9b52d7d5acc2729951a66	yes	3

	Multipart Description/PDF files in .zip description					
	Document Description		Start		End	
	Transmittal Letter		1		2	
	Information Disclosure Statement (IDS) Filed (SB/08)		3		3	
Warnings:						
Information:						
2	NPL Documents	CROSS1120_Ref_C171.pdf	3613973 d445cf43c5f3deb791444e7c7cc7f749b39cb156	no	114	
Warnings:						
Information:						
		Total Files Size (in bytes):	3729651			

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Atty. Docket No. (Opt.) **CROSS1120-33**

Applicant **Geoffrey B. Hoese**	
Application Number **12/690,592**	Filing or 371 (c) Date: **January 20, 2010**
For **STORAGE ROUTER AND METHOD FOR PROVIDING VIRTUAL LOCAL STORAGE**	
Group Art Unit **2182**	Examiner **Unknown**
Confirmation Number: **8115**	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Certification of Transmission Under 37 C.F.R. 1.8

I hereby certify that this correspondence is being transmitted to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22312-1450 via the U.S. Patent and Trademark Office Electronic Filing System (EFS-Web) on June 9 **2010**.

Betty Caldwell
Betty Caldwell

Dear Sir,

Applicant respectfully requests, pursuant to 37 C.F.R. §§ 1.56, 1.97 and 1.98, that the information listed on the attached SB08A/B form(s) be considered and cited in the examination of the above-identified application. A copy of U.S. Patent(s) and U.S. Patent Application Publication(s) listed on the attached SB08A form is not being submitted with this Information Disclosure Statement pursuant to the waiver of 37 C.F.R. § 1.98(a)(2)(i) by the U.S. Patent and Trademark Office. A copy of foreign patent documents as well as the information listed on the attached SB08B form is enclosed for the convenience of the Examiner.

☐ This Information Disclosure Statement is being submitted within three months of the filing date of a national application other than a continued prosecution application under 37 C.F.R. § 1.53(d).

☐ This Information Disclosure Statement is being submitted within three months of the date of entry of the national stage as set forth in 37 C.F.R. § 1.491 in an international application;

☒ This Information Disclosure Statement is being submitted before the mailing of a first Office action on the merits; or

☐ This Information Disclosure Statement is being submitted before the mailing of a first Office action after the filing of a request for continued examination under 37 C.F.R. § 1.114.

☐ This Information Disclosure Statement is being submitted after the period specified in 37 C.F.R. § 1.97(b) and before the mailing date of any of a final action under 37 C.F.R. § 1.113, a notice of allowance under 37 C.F.R. § 1.311, or an action that otherwise closes prosecution in the application, and is accompanied by one of:

- ☐ The statement specified in 37 C.F.R. § 1.97(e); or
- ☐ The fee set forth in 37 C.F.R. § 1.17(p). Applicant hereby authorizes the Commissioner to deduct the amount of $180 from Deposit Account No. 50-3183 of Sprinkle IP Law Group for the filing fee of this Information Disclosure Statement.

☐ This Information Disclosure Statement is being submitted after the period specified in 37 C.F.R. § 1.97(c) and on or before payment of the issue fee and is accompanied by:

- ☐ The statement specified in 37 C.F.R. § 1.97(e); and
- ☐ The fee set forth in 37 C.F.R. § 1.17(p). Applicant hereby authorizes the Commissioner to deduct the amount of $180 from Deposit Account No. 50-3183 of Sprinkle IP Law Group for the filing fee of this Information Disclosure Statement.

Applicant does not believe any fees are due for filing this Information Disclosure Statement; however, if Applicant is in error, the Director is hereby authorized to deduct any and all appropriate fees from Deposit Account 50-3183 of Sprinkle IP Law Group. Applicant respectfully submits that the claims of Applicant's above-referenced patent application are patentably distinguishable from the listed information.

Respectfully submitted,

Sprinkle IP Law Group
Attorneys for Applicant

John L. Adair
Reg. No. 48,828

Dated: June 8

1301 W. 25th Street, Suite 408
Austin, Texas 78705
Tel. (512) 637-9220
Fax. (512) 317-9088

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Atty. Docket No. (Opt.) **CROSS1120-33**

Applicant **Geoffrey B. Hoese**	
Application Number **12/690,592**	Filing or 371 (c) Date: **January 20, 2010**
For **STORAGE ROUTER AND METHOD FOR PROVIDING VIRTUAL LOCAL STORAGE**	
Group Art Unit **2182**	Examiner **Unknown**
Confirmation Number: **8115**	

Certification of Transmission Under 37 C.F.R. 1.8

I hereby certify that this correspondence is being transmitted to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22312-1450 via the U.S. Patent and Trademark Office Electronic Filing System (EFS-Web) on 8/20/ **2010**.

Janice Pampell

Janice Pampell

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir,

Applicant respectfully requests, pursuant to 37 C.F.R. §§ 1.56, 1.97 and 1.98, that the information listed on the attached SB08A/B form(s) be considered and cited in the examination of the above-identified application. A copy of U.S. Patent(s) and U.S. Patent Application Publication(s) listed on the attached SB08A form is not being submitted with this Information Disclosure Statement pursuant to the waiver of 37 C.F.R. § 1.98(a)(2)(i) by the U.S. Patent and Trademark Office. A copy of foreign patent documents as well as the information listed on the attached SB08B form is enclosed for the convenience of the Examiner.

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☒ This Information Disclosure Statement is being submitted before the mailing of a first Office action on the merits; or

☐ This Information Disclosure Statement is being submitted before the mailing of a first Office action after the filing of a request for continued examination under 37 C.F.R. § 1.114.

☐ This Information Disclosure Statement is being submitted after the period specified in 37 C.F.R. § 1.97(b) and before the mailing date of any of a final action under 37 C.F.R. § 1.113, a notice of allowance under 37 C.F.R. § 1.311, or an action that otherwise closes prosecution in the application, and is accompanied by one of:

- ☐ The statement specified in 37 C.F.R. § 1.97(e); or
- ☐ The fee set forth in 37 C.F.R. § 1.17(p). Applicant hereby authorizes the Commissioner to deduct the amount of $180 from Deposit Account No. 50-3183 of Sprinkle IP Law Group for the filing fee of this Information Disclosure Statement.

☐ This Information Disclosure Statement is being submitted after the period specified in 37 C.F.R. § 1.97(c) and on or before payment of the issue fee and is accompanied by:

- ☐ The statement specified in 37 C.F.R. § 1.97(e); and
- ☐ The fee set forth in 37 C.F.R. § 1.17(p). Applicant hereby authorizes the Commissioner to deduct the amount of $180 from Deposit Account No. 50-3183 of Sprinkle IP Law Group for the filing fee of this Information Disclosure Statement.

Applicant does not believe any fees are due for filing this Information Disclosure Statement; however, if Applicant is in error, the Director is hereby authorized to deduct any and all appropriate fees from Deposit Account 50-3183 of Sprinkle IP Law Group. Applicant respectfully submits that the claims of Applicant's above-referenced patent application are patentably distinguishable from the listed information.

Respectfully submitted,

Sprinkle IP Law Group
Attorneys for Applicant

John L. Adair
Reg. No. 48,828

Dated: Aug 20, 2010

1301 W. 25th Street, Suite 408
Austin, Texas 78705
Tel. (512) 637-9220
Fax. (512) 317-9088

INFORMATION DISCLOSURE STATEMENT				Application Number	12/690,592
				Filing or 371 (c) Date:	January 20, 2010
				First Named Inventor	Geoffrey B. Hoese
				Group Art Unit	2182
				Examiner Name	Unknown
Sheet	1	of	1	Atty Docket Number	CROSS1120-33

NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published	T^2
	C172	QUESTIONING Mailed 06/08/2010 from JP Patent Application 526873/2000. 8 pages	06/08/10
	C173	Office Action Mailed 08/17/2010 in U.S. Serial No. 11/947,499 to Hoese. 6 pgs.	08/17/10

Examiner Signature		Date Considered	

Electronic Acknowledgement Receipt

EFS ID:	8262176
Application Number:	12690592
International Application Number:	
Confirmation Number:	8115
Title of Invention:	STORAGE ROUTER AND METHOD FOR PROVIDING VIRTUAL LOCAL STORAGE
First Named Inventor/Applicant Name:	Geoffrey B. Hoese
Customer Number:	44654
Filer:	John L. Adair/Janice Pampell
Filer Authorized By:	John L. Adair
Attorney Docket Number:	CROSS1120-33
Receipt Date:	20-AUG-2010
Filing Date:	20-JAN-2010
Time Stamp:	17:26:49
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Filed (SB/08)	CROSS1120-33_IDS_Filed_08-20-10.pdf	78419 ca3556359c8fac70e9f21e47262198ec9535b507	no	3

Warnings:	
Information:	

This is not an USPTO supplied IDS fillable form					
2	NPL Documents	CROSS1120_Ref_C172.pdf	197554 f69f3813c29e318b796ff0f186ce0dd9b5f3b5d4	no	8
Warnings:					
Information:					
3	NPL Documents	CROSS1120_Ref_C173.pdf	175870 2f518144450f3e34d8d4f7cabc7ea31971be6085	no	7
Warnings:					
Information:					
			Total Files Size (in bytes):	451843	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/690,592	01/20/2010	Geoffrey B. Hoese	CROSS1120-33	8115

44654 7590 09/10/2010

SPRINKLE IP LAW GROUP
1301 W. 25TH STREET
SUITE 408
AUSTIN, TX 78705

EXAMINER	
SHIN, CHRISTOPHER B	

ART UNIT	PAPER NUMBER
2181	

MAIL DATE	DELIVERY MODE
09/10/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Interview Summary	Application No.	Applicant(s)	
	12/690,592	HOESE ET AL.	
	Examiner	Art Unit	
	Christopher B. Shin	2181	

All participants (applicant, applicant's representative, PTO personnel):

(1) *Christopher B. Shin*. (3)_____.

(2) *John L. Adair*. (4)_____.

Date of Interview: *30 August 2010*.

Type: a)☒ Telephonic b)☐ Video Conference
c)☐ Personal [copy given to: 1)☐ applicant 2)☐ applicant's representative]

Exhibit shown or demonstration conducted: d)☐ Yes e)☐ No.
If Yes, brief description: _____.

Claim(s) discussed: *1-53*.

Identification of prior art discussed: _____.

Agreement with respect to the claims f)☒ was reached. g)☐ was not reached. h)☐ N/A.

Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: *In order to move the case in condition for allowance & to be consistent with the all of the related/parent cases/specification, the applicant agreed to amend the claims to clearly recite that the claimed mediums (i.e., the first and second medims) are not the same mediums, but the protocols used on such mediums can be the same or different protocol types. Therefore,the native low level block protocols are used between different mediums that may use the same or different protocol types is consistent with the related cases and specification. In other words, one of the medium is remote, separate & different from the other medium.. The applicant also agreed to amend & update the RELATED APPLICATIONS of the specification; & the applicant agreed to file Terminal Disclaimer against all of the Related Applications* .

(A fuller description, if necessary, and a copy of the amendments which the examiner agreed would render the claims allowable, if available, must be attached. Also, where no copy of the amendments that would render the claims allowable is available, a summary thereof must be attached.)

THE FORMAL WRITTEN REPLY TO THE LAST OFFICE ACTION MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW. (See MPEP Section 713.04). If a reply to the last Office action has already been filed, APPLICANT IS GIVEN A NON-EXTENDABLE PERIOD OF THE LONGER OF ONE MONTH OR THIRTY DAYS FROM THIS INTERVIEW DATE, OR THE MAILING DATE OF THIS INTERVIEW SUMMARY FORM, WHICHEVER IS LATER, TO FILE A STATEMENT OF THE SUBSTANCE OF THE INTERVIEW. See Summary of Record of Interview requirements on reverse side or on attached sheet.

/Christopher B Shin/
Primary Examiner, Art Unit 2181

Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record
A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews
Paragraph (b)

In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.
All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

———

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:
- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:

1) A brief description of the nature of any exhibit shown or any demonstration conducted,
2) an identification of the claims discussed,
3) an identification of the specific prior art discussed,
4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
5) a brief identification of the general thrust of the principal arguments presented to the examiner,
   (The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
6) a general indication of any other pertinent matters discussed, and
7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/690,592	01/20/2010	Geoffrey B. Hoese	CROSS1120-33	8115

44654 7590 09/10/2010

SPRINKLE IP LAW GROUP
1301 W. 25TH STREET
SUITE 408
AUSTIN, TX 78705

EXAMINER	
SHIN, CHRISTOPHER B	

ART UNIT	PAPER NUMBER
2181	

MAIL DATE	DELIVERY MODE
09/10/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	12/690,592	HOESE ET AL.	
	Examiner	Art Unit	
	Christopher B. Shin	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *Multiple Sheets*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Interview with agreement reached

1. An Agreement was reached during the interview conducted with John L. Adair on august 30, 2010 (See the interview Record). The examiner thanks the applicant for very helpful discussions & cooperation to make the case in condition for allowance. As can be seen from the plurality of related cases, the allowable subject matter over the prior art of record was identified and reached. In order to move the case in condition for allowance & to be consistent with the all of the related/parent cases/specification, the applicant agreed to amend the claims to clearly recite that the claimed mediums (i.e., the first and second medims) are not the same mediums, but the protocols used on such mediums can be the same or different protocol types. Therefore,the native low level block protocols are used between different mediums that may use the same or different protocol types is consistent with the related cases and specification. In other words, one of the medium is remote, separate & different from the other medium. The applicant also agreed to amend & update the RELATED APPLICATIONS of the specification; & the applicant agreed to file Terminal Disclaimer against all of the Related Applications. For the above reasons, the examiner implicitly gives rejection as follows.

Double Patenting/Allowable Subject Matter

2. After careful consideration of the present claims and in relation to all of the parent and/or related application, the examiner finds the claimed invention allowable over the

prior art of records (i.e., prior art of records of the parent & related cases). However, the present claimed invention does not overcome the Double patenting rejections against the parent and related patent/applications. The following interview was conducted with the applicant and the agreement was reached.

Interview/Double Patenting Rejection

3. On August 30, 2010, a telephonic interview was conducted and the applicant agreed to file additional Terminal Disclaimer against all of the remaining related pending applications and allowed applications. During the interview, the examiner kindly asks the applicant to make sure that the present and pending applications to be consistent with the related reexamination applications.

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,*418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

a. Since the applicant agreed with the examiner regarding the Double Patenting rejection, the details of the rejection will be omitted.

b. The examiner kindly asks the applicant for help on identifying all of the related applications, if the examiner inadvertently makes a mistake.

5. Claims 1-53 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims of all of the related Patent/Applications as follows. Although the conflicting claims are not identical, they are not patentably distinct from each other because the related applications claim subject matter that are substantially identical to the present claimed invention. The following are the list of the related cases:

6. Claims 1-53 are rejected on the ground of nonstatutory double patenting over claims of U. S. Patent/Applications of all the related cases, since the claims, if allowed, would improperly extend the "right to exclude" already granted in the patent.

The subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent since the patent and the application are claiming common subject matter.

Furthermore, there is no apparent reason why applicant was prevented from presenting claims corresponding to those of the instant application during prosecution of the application which matured into a patent. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

7. Examiner kindly asks applicant's help for identifying all the related cases (i.e., all the parent and child cases) and submitting T.D. to make the case in condition for

allowance. Further more, the applicant should also submit IDS with all the related prior art of record.

Specification

8. The disclosure is objected to because of the following informalities:

As agreed by the applicant, the RELATED APPLICATIONS sections should be updated.

Appropriate correction is required.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher B. Shin whose telephone number is 571-272-4159. The examiner can normally be reached on Monday Thruogh Friday 6:30AM to 3:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kindred Alford can be reached on 571-272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Christopher B Shin/
Primary Examiner, Art Unit 2181

cs

Search Notes

Application/Control No.	Applicant(s)/Patent under Reexamination
12/690,592	HOESE ET AL.
Examiner	**Art Unit**
Christopher B. Shin	2181

SEARCHED			
Class	Subclass	Date	Examiner
710	1-5,8-13,36-38,126-131	8/30/2010	CS
710	250, 305-	8/30/2010	CS
709	258	8/30/2010	CS
714	42	8/30/2010	CS
711	110-113	8/30/2010	CS

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner
710	**305,11**		
709	258		

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
PLUS from the parent cases	8/30/2010	CS
PALM- for double patenting	8/30/2010	CS
EAST (See notes for parent)	8/30/2010	CS
PARETN & RELATED CASES REVIEWED FOR THE ALOWANCE	8/30/2010	CS
Reviewed IDS	8/30/2010	CS

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Application Number	12/690,592
Filing Date	01/20/2010
First Named Inventor	Geoffrey B. Hoese
Group Art Unit	2111
Examiner Name	Unknown
Attorney Docket Number	CROSS1120-33

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U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number Number-Kind Code *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	A1	3,082,406	3/19/1963	L.D. Stevens	
	A2	4,092,732	5/30/1978	Ouchi	
	A3	4,170,415	10/9/1979	Lemeshewsky, et al.	
	A4	4,415,970	11/15/1983	Swenson, et al.	
	A5	4,455,605	6/19/1984	Cormier, et al.	
	A6	4,504,927	3/12/1985	Callan	
	A7	4,533,996	8/6/1985	Gartung, et al.	
	A8	4,573,152	2/25/1986	Greene, et al.	
	A9	4,603,380	7/29/1986	Easton, et al.	
	A10	4,620,295	10/28/1986	Aiden, Jr.	
	A11	4,644,462	2/17/1987	Matsubara, et al.	
	A12	4,695,948	9/22/1987	Blevins, et al.	
	A13	4,697,232	9/29/1987	Brunelle, et al.	
	A14	4,715,030	12/22/1987	Koch, et al.	
	A15	4,751,635	6/14/1988	Kret	
	A16	4,787,028	11/22/1988	Finforck, et al.	
	A17	4,807,180	2/21/1989	Takeuchi, et al.	
	A18	4,811,278	3/7/1989	Bean, et al.	
	A19	4,821,179	4/11/1989	Jensen, et al.	
	A20	4,825,406	4/25/1989	Bean, et al.	
	A21	4,827,411	5/2/1989	Arrowood, et al.	
	A22	4,835,674	5/30/1989	Collins, et al.	
	A23	4,845,722	7/4/1989	Kent et al.	
	A24	4,864,532	9/5/1989	Reeve, et al.	
	A25	4,897,874	1/30/1990	Lidensky, et al.	
	A26	4,947,367	8/7/1990	Chang, et al.	
	A27	4,961,224	10/2/1990	Yung	
	A28	5,072,378	12/10/1991	Manka	
	A29	5,077,732	12/31/1991	Fischer, et al.	
	A30	5,077,736	12/31/1991	Dunphy, Jr., et al.	
	A31	5,124,987	6/23/1992	Milligan, et al.	
	A32	5,155,845	10/13/1992	Beal, et al.	
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	A34	5,185,876	2/9/1993	Nguyen, et al.	
	A35	5,193,168	3/9/1993	Corrigan, et al.	
	A36	5,193,184	3/9/1993	Belsan, et al.	
	A37	5,202,856	4/13/1993	Glider, et al.	
	A38	5,210,866	5/11/1993	Milligan, et al.	

Examiner Signature	/Christopher Shin/	Date Considered	08/26/2010

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /C.S./

INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	12/690,592
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				Group Art Unit	2111
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	A39	5,212,785	5/18/1993	Powers, et al.	
	A40	5,214,778	5/25/1993	Glider, et al.	
	A41	5,226,143	7/6/1993	Baird, et al.	
	A42	5,239,632	8/24/1993	Larner	
	A43	5,239,643	8/24/1993	Blount, et al.	
	A44	5,239,654	8/24/1993	Ing-Simmons, et al.	
	A45	5,247,638	9/21/1993	O'Brien, et al.	
	A46	5,247,692	9/21/1993	Fujimura	
	A47	5,257,386	10/26/1993	Saito	
	A48	5,297,262	3/22/1994	Cox, et al.	
	A49	5,301,290	4/5/1994	Tetzlaff, et al.	
	A50	5,315,657	5/24/1994	Abadi, et al.	
	A51	5,317,693	5/31/1994	Elko, et al.	
	A52	5,331,673	7/19/1994	Elko, et al.	
	A53	5,347,384	9/13/1994	McReynolds, et al.	
	A54	5,355,453	10/11/1994	Glider, et al.	
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	A56	5,367,646	11/22/1994	Pardillos, et al.	
	A57	5,379,385	1/3/1995	Shomler	
	A58	5,379,398	1/3/1995	Cohn, et al.	
	A59	5,388,243	2/7/1995	Glider, et al.	
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	A61	5,394,402	2/28/1995	Ross, et al.	
	A62	5,394,526	2/28/1995	Crouse et al.	
	A63	5,396,596	3/7/1995	Hashemi, et al.	
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	A66	5,410,697	4/25/1995	Baird, et al.	
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	A68	5,416,915	5/16/1995	Mattson, et al.	

Examiner Signature	/Christopher Shin/	Date Considered	08/26/2010

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /C.S./

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				Group Art Unit	2111
				Examiner Name	Unknown
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U.S. PATENT DOCUMENTS

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	A71	5,423,026	6/6/1995	Cook, et al.	
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	A73	5,426,637	6/20/1995	Derby, et al	
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	A76	5,452,421	9/19/1995	Beardsley, et al.	
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	A89	5,519,695	5/21/1996	Purohit, et al.	
	A90	5,530,845	6/25/1996	Hiatt, et al.	
	A91	5,535,352	7/9/1996	Bridges, et al.	
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	A95	5,564,019	10/8/1996	Beausoleil, et al	
	A96	5,568,648	10/22/1996	Coscarella, et al.	
	A97	5,581,709	12/3/1996	Ito, et al.	
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Examiner Signature	/Christopher Shin/	Date Considered	08/26/2010

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				Examiner Name	Unknown
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Examiner Initials	Cite No.	Document Number Number-Kind Code *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Passages or Figures Appear
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	A100	5,596,562	6/21/1997	Chen	
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	A102	5,598,541	1/28/1997	Malladi	
	A103	5,613,082	3/18/1997	Brewer, et al.	
	A104	5,621,902	4/15/1997	Cases, et al.	
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	A120	5,751,975	5/12/1998	Gillespie, et al.	
	A121	5,764,931	6/9/1998	Schmahl, et al.	
	A122	5,768,623	6/16/1998	Judd, et al.	
	A123	5,774,683	6/30/1998	Gulick	
	A124	5,778,411	7/7/1998	DeMoss	
	A125	5,781,715	7/14/1998	Sheu	
	A126	5,802,278	9/1/1998	Isfeld, et al.	
	A127	5,805,816	9/8/1998	Picazo, Jr., et al.	
	A128	5,805,920	9/8/1998	Sprenkle, et al.	

Examiner Signature	/Christopher Shin/	Date Considered	08/26/2010

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				Examiner Name	Unknown
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U.S. PATENT DOCUMENTS

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	A132	5,825,772	10/20/1998	Dobbins, et al.	
	A133	5,835,496	11/10/1998	Yeung, et al.	
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	A143	5,923,557	7/13/1999	Eidson	
	A144	5,933,824	8/3/1999	DeKoning, et al.	
	A145	5,935,205	8/10/1999	Murayama, et al.	
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	A155	5,978,875	11/2/1999	Asano, et al.	
	A156	5,991,797	11/23/1999	Futral, et al.	
	A157	6,000,020	12/7/1999	Chin, et al.	
	A158	6,041,058	3/21/2000	Flanders, et al.	

Examiner Signature	/Christopher Shin/	Date Considered	08/26/2010

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /C.S./

INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	12/690,592
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U.S. PATENT DOCUMENTS

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	A160	6,029,168	2/22/2000	Frey	
	A161	6,032,269	2/29/2000	Renner, Jr.	
	A162	6,041,381	3/21/2000	Hoese	
	A163	6,055,603	4/25/2000	Ofer, et al.	
	A164	6,065,087	5/16/2000	Keaveny, et al.	
	A165	6,070,253	5/30/2000	Tavallaei, et al.	
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				First Named Inventor	Geoffrey B. Hoese
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	C66	Plaintiff's Revised Trial Exhibit List, Crossroads Systems, Inc. v. Pathlight Technology, Inc., C.A. No. A-00CA-248-SS (W.D. Tex. 2001). **(CD-Rom)**	
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	C75	OEM Datasheet on the 3701 Controller (Engelbrecht 13 (LSI 01837-38)) (**CD-ROM** Chaparral Exhibits D017)	6/17/1905
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	C77	Organizational Presentation on the External Storage Group (Lavan Ex 1 (CNS 182242-255)) (**CD-ROM** Chaparral Exhibits D021)	4/11/1996
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	C79	Bridge. C, Bridge Between SCSI-2 and SCSI-3 FCP (Fibre Channel Protocol) (**CD-ROM** Chaparral Exhibits P214)	
	C80	Attendees/Action Items from 4/12/96 Meeting at BTC (Lavan Ex 3 (CNS 182241)) (**CD-ROM** Chaparral Exhibits D023)	4/12/1996
	C81	Brooklyn Hardware Engineering Requirements Documents, Revision 1.4 (Lavan Ex 4 (CNS 178188-211)) (**CD-ROM** Chaparral Exhibits D024) by Pecone	5/26/1996
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	C87	Bill of Material (Lavan Ex 14 (CNS 177211-214)) (**CD-ROM** Chaparral Exhibits D034)	7/24/1997
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	C90	AEC-4412B, AEC7412/3B External RAID Controller Hardware OEM Manual, Revision 3.0. (Lavan Ex 17 (CNS 177124-165)) (**CD-ROM** Chaparral Exhibits D037)	8/25/1997
	C91	Memo Dated 8/15/97 to AEC-7312A Evaluation Unit Customers re: B001 Release Notes (Lavan Ex 18 (CNS 182878-879)) (**CD-ROM** Chaparral Exhibits D038)	8/15/1997
	C92	Brooklyn Main Board (AES-0302) MES Schedule (Lavan Ex I9 (CNS 177759-763)) (**CD-ROM** Chaparral Exhibits D039)	2/11/1997
	C93	News Release-Adaptec Adds Fibre Channel Option to its External RAID Controller Family (Lavan Ex 20 (CNS 182932-934)) (**CD-ROM** Chaparral Exhibits D040)	5/6/1997
	C94	AEC-4412B/7412B User's Guide, Rev. A (Lavan Ex 21) (**CD-ROM** Chaparral Exhibits D041)	6/19/1905
	C95	Data Book- AIC-7895 PCI Bus Master Single Chip SCSI Host Adapter (Davies Ex 1 (CNS 182944-64)) (**CD-ROM** Chaparral Exhibits D046)	5/21/1996
	C96	Data Book- AIC-1160 Fibre Channel Host Adapter ASIC (Davies Ex 2 (CNS 181800-825)) (**CD-ROM** Chaparral Exhibits D047)	6/18/1905
	C97	Viking RAID Software (Davies Ex 3 (CNS 180969-181026)) (**CD-ROM** Chaparral Exhibits D048)	6/18/1905
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	C100	Header File Data Structure (Davies Ex 6 (CNS 179997-180008)) (**CD-ROM** Chaparral Exhibits D051)	1/2/1997
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	C102	Coronado: Fibre Channel to SCSI Intelligent RAID Controller Product Brief (Kalwitz Ex I (CNS 182804-805)) (**CD-ROM** Chaparral Exhibits D053)	
	C103	Bill of Material (Kalwitz Ex 2 (CNS 181632-633)) (**CD-ROM** Chaparral Exhibits D054)	3/17/1997
	C104	Emails Dated 1/13-3/31/97 from P. Collins to Mo re: Status Reports (Kalwitz Ex 3 (CNS 182501-511)) (**CD-ROM** Chaparral Exhibits D055)	
	C105	Hardware Schematics for the Fibre Channel Daughtercard Coronado (Kalwitz Ex 4 (CNS 181639-648)) (**CD-ROM** Chaparral Exhibits D056)	

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	C106	Adaptec Schematics re AAC-340 (Kalwitz Ex 14 CNS 177215-251)) (**CD-ROM** Chaparral Exhibits D057)	
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	C108	AEC Bridge Series Products-Adaptec External Controller RAID Products Pre-Release Draft, v.6 (Manzanares Ex 4 (CNS 174632-653)). (**CD-ROM** Chaparral Exhibits D059)	10/28/1997
	C109	Hewlett-Packard Roseville Site Property Pass for Brian Smith (Dunning Ex 14 (HP 489) (**CD-ROM** Chaparral Exhibits D078)	11/7/1996
	C110	Distribution Agreement Between Hewlett-Packard and Crossroads (Dunning Ex 15 (HP 326-33) (**CD-ROM** Chaparral Exhibits D079)	
	C111	HPFC-5000 Tachyon User's Manuel, First Edition (PTI 172419-839) (**CD-ROM** Chaparral Exhibits D084)	5/1/1996
	C112	X3T10 994D - (Draft) Information Technology: SCSI-3 Architecture Model, Rev. 1.8 (PTI 165977) (**CD-ROM** Chaparral Exhibits D087)	
	C113	X3T10 Project 1047D: Information Technology- SCSI-3 Controller Commands (SCC), Rev, 6c (PTI 166400-546) (**CD-ROM** Chaparral Exhibits D088)	9/3/1996
	C114	X3T10 995D- (Draft) SCSI-3 Primary Commands, Rev. 11 (Wanamaker Ex 5 (PTI 166050-229)) (**CD-ROM** Chaparral Exhibits D089)	11/13/1996
	C115	VBAR Volume Backup and Restore (CRDS 12200-202) (**CD-ROM** Chaparral Exhibits D099)	
	C116	Preliminary Product Literature for Infinity Commstor's Fibre Channel to SCSI Protocol Bridge (Smith Ex 11; Quisenberry Ex 31 (SPLO 428-30) (**CD-ROM** Chaparral Exhibits D143)	8/19/1996
	C117	Letter dated 7/12/96 from J. Boykin to B. Smith re: Purchase Order for Evaluation Units from Crossroads (Smith Ex 24) CRDS 8556-57) (**CD-ROM** Chaparral Exhibits D144)	7/12/1996
	C118	CrossPoint 4100 Fibre Channel to SCSI Router Preliminary Datasheet (Hulsey Ex 9 (CRDS 16129-130)) (**CD-ROM** Chaparral Exhibits D145)	11/1/1996
	C119	CrossPoint 4400 Fibre Channel to SCSI Router Preliminary Datasheet (Bardach Ex. 9, Quisenberry Ex 33 (CRDS 25606-607)) (**CD-ROM** Chaparral Exhibits D153)	11/1/1996
	C120	Fax Dated 07/22/96 from L. Petti to B. Smith re: Purchase Order from Data General for FC2S Fibre to Channel SCSI Protocol Bridge Model 11 (Smith Ex 25; Quisenberry Ex 23; Bardach Ex 11 (CRDS 8552-55; 8558) (**CD-ROM** Chaparral Exhibits D155)	7/22/1996
	C121	Email Dated 12/20/96 from J. Boykin to B. Smith re: Purchase Order for Betas in February and March (Hoese Ex 16, Quisenberry Ex 25; Bardach Ex 12 (CRDS 13644-650) (**CD-ROM** Chaparral Exhibits D156)	12/20/1996
	C122	Infinity Commstor Fibre Channel Demo for Fall Comdex, 1996 (Hoese Ex 15, Bardach Ex 13 (CRDS 27415) (**CD-ROM** Chaparral Exhibits D157)	

Examiner Signature	/Christopher Shin/	Date Considered	08/26/2010

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /C.S./

INFORMATION DISCLOSURE STATEMENT				Application Number	12/690,592
				Filing Date	01/20/2010
				First Named Inventor	Geoffrey B. Hoese
				Group Art Unit	2111
				Examiner Name	Unknown
Sheet	7	of	9	Atty Docket Number	CROSS1120-33

Examiner Initials	Cite No.	OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS	Date
	C123	Fax Dated 12/19/96 from B. Bardach to T. Rarich re: Purchase Order Information (Bardach Ex. 14; Smith Ex 16 (CRDS 4460)) (**CD-ROM** Chaparral Exhibits D158)	12/19/1996
	C124	Miscellaneous Documents Regarding Comdex (Quisenberry Ex 2 (CRDS 27415-465)) (**CD-ROM** Chaparral Exhibits D165)	
	C125	CrossPoint 4100 Fibre Channel to SCSI Router Preliminary Datasheet (Quisenberry) Ex 3 (CRDS 4933-34) (**CD-ROM** Chaparral Exhibits D166) (CD-ROM Chaparral Exhibits D166)	
	C126	CrossPoint 4400 Fibre to Channel to SCSI Router Preliminary Datasheet; Crossroads Company and Product Overview (Quisenberry Ex 4 (CRDS 25606; 16136)) (**CD-ROM** Chaparral Exhibits D167)	
	C127	Crossroads Purchase Order Log (Quisenberry Ex 9 (CRDS 14061-062)) (**CD-ROM** Chaparral Exhibits D172)	
	C128	RAID Manager 5 with RDAC 5 for UNIX V.4 User's Guide (LSI-01854) (**CD-ROM** Chaparral Exhibits P062)	9/1/1996
	C129	Letter dated May 12, 1997 from Alan G. Leal to Barbara Bardach enclosing the original OEM License and Purchase Agreement between Hewlett-Package Company and Crossroads Systems, Inc. (CRDS 02057) (**CD-ROM** Chaparral Exhibits P130)	
	C130	CR4x00 Product Specification (CRDS 43929) (**CD-ROM** Chaparral Exhibits P267)	6/1/1998
	C131	Symbios Logic – Hardware Functional Specification for the Symbios Logic Series 3 Fibre Channel Disk Array Controller Model 3701 (Engelbrecht Ex 3 (LSI-1659-1733) (**CD-ROM** Pathlight Exhibits D074)	
	C132	Report of the Working Group on Storage I/O for Large Scale Computing; Department of Computer Science Duke University: CS-1996-21 (PTI 173330-347). (**CD-ROM** Pathlight Exhibits D098)	
	C133	Brian Allison's 1999 Third Quarter Sales Plan (PDX 38)CNS 022120-132)) (**CD-ROM** Pathlight Exhibits D201)	6/5/2001
	C134	Brooklyn SCSI-SCSI Intelligent External RAID Bridge Definition Phase External Documentation ((**CD-ROM** Pathlight Exhibits D129)	
	C135	StorageWorks HSx70 System Specification by Steve Sicola dated 6/11/96 4:57pm, Revision 4.	6/11/1996
	C136	ANSI TR X3.xxx-199x, Revision 9 of X3-991D. Draft Proposed X3 Technical Report - Small Computer System Interface - 3 Generic Packetized Protocol (SCSI-GPP). Computer and Business Equipment Manufacturers Assoc.	
	C137	Enterprise Systems Connection (ESON) Implementation Guide, July 1996, IBM International Technical Support Organization, Poughkeepsie Center	7/1/1996

Examiner Signature	/Christopher Shin/	Date Considered	08/26/2010

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /C.S./

INFORMATION DISCLOSURE STATEMENT

Application Number	12/690,592
Filing Date	01/20/2010
First Named Inventor	Geoffrey B. Hoese
Group Art Unit	2111
Examiner Name	Unknown
Atty Docket Number	CROSS1120-33

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Examiner Initials	Cite No.	OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS	Date
	C138	Digital Delivers Industry-Leading Enterprise-Class Storage Solutions. StorageWorks Family Provides Easiest Path to Fibre Channel. Three pages by Company News Oncall dated 09/09/04	9/9/2004
	C139	American National Standard for Information Technology – Fibre Channel Protocol for SCSI. ANSI X3.269-1996	6/18/1905
	C140	F1710A File Control Unit and F6493 Array Disk Subsystem by Hitoshi Matsushima, Shojiro Okada and Tetsuro Kudo.	2/3/1995
	C141	The Legend of AMDAHL by Jeffrey L. Rodengen (5 pages)	
	C142	Office Action dated February 6, 2007 from the Japanese Patent Office regarding related application No. 526873/2000.	2/6/2007
	C143	InfoServer 100 System Operation Guide, Order Number EK-DIS1K-UG-001	
	C144	iNFOsERVER 100 Installation and Owner's Guide, Order Number EK-DIS1K-IN-001	
	C145	Software Product Description: Product Name: InfoServer 100 Software, Version 1.1 SPD 38.59.00	11/1/1991
	C146	Software Product Description: Product Name: InfoServer Client for ULTRIX, Version 1.1, SPD 40.78.01	4/1/1993
	C147	Draft Proposed American National Standard. X3.269-199X, Revision 012. Information System - dpANS Fibre Channel Protocol fo SCSI.	12/4/1995
	C148	Impactdata Launches Breakthrough Architecture for Network Storage.	11/13/1996
	C149	Impactdata..News Release: Impactdata Introduces New Storage Architecture for High Performance Computing. 2 Pages.	11/12/1996
	C150	Impactdata..News Release: Impactdata's Network Peripheral Adapter (NPA) Pushes Technology Envelope of Data Storage Management in High-Speed Computing Environments. 2 Pages.	11/12/1996
	C151	Impactdata..News Release: Impactdata and Storage Concepts Announce Integration of FibreRAID II Storage Solution with Impactdata's Distributed Storage Node Architecture (DSNA). 2 pages.	11/18/1996
	C152	Impactdata..News Release: Breece Hill Libraries Now Able to Attach Directly to High Speed Networks Peripheral Adapter from Impactdata. 2 Pages.	11/20/1996
	C153	Impactdata - DSNA Questions and Answers. 22 Pages.	
	C154	Impactdata - Network Storage Solutions. 4 pages.	
	C155	Network Storage Building Blocks. 2 Pages.	
	C156	Impactdata - NPA (Network Peripheral Interface). 4 Pages	
	C157	Impactdata - CPI (Common Peripheral Interfae). 2 Pages	
	C158	Impactdata - SNC (Storage Node Controller). 2 Pages	
	C159	Impactdata - DSNA (Distributed Storage Node Architecture) Protocol. 2 Pages	
	C160	Impactdata - DS-50. 2 Pages	
	C161	Impactdata - Corporate Fact Sheet. 1 Page	

Examiner Signature	/Christopher Shin/	Date Considered	08/26/2010

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /C.S./

INFORMATION DISCLOSURE STATEMENT				Application Number	12/690,592
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				First Named Inventor	Geoffrey B. Hoese
				Group Art Unit	2111
				Examiner Name	Unknown
Sheet	9	of	9	Atty Docket Number	CROSS1120-33

Examiner Initials	Cite No.	OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS	Date
	C162	Raider-5 "Disk Array Manual for the UltraSCSI Controller". Part No. 261-0013-002. 191 Pages	
	C163	Impactdata - White Paper: Distributed Storage Node Architecture (DSNA). January, 1997	01/97
	C164	Impactdata - DSNA Distributed Storage Node Architecture "Reference Guide". 44 Pages	
	C165	F1710 Logic Specification	
	C166	Translation of Final Office Action issued in JP 526873/2000 mailed 05/14/08. 4 Pages.	5/14/2008
	C167	Office Action issued in USPA 11/851,837 dated 12/22/08, Hoese, 7 pages	12/22/2008
	C168	English Translation of Japanese Laid-Open Publication No. 5-181609. 9 pgs.	7/23/1993
	C169	English Translation of Japanese Laid-Open Publication No. 7-20994. 57 pgs	1/24/1995
	C170	F1710 File Control Unit (FCU) Logical Specifications. 11 Pages	12/9/1997

Examiner Signature	/Christopher Shin/	Date Considered	08/26/2010

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /C.S./

	Type	Hits	Search Text	DBs
1	IS&R	6	(("7340549") or ("7051147") or ("6789152") or ("6421753") or ("5941972") or ("20080307444")).PN.	US-PGPUB; USPAT
2	BRS	175	crossroads.as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
3	BRS	21357	geoffrey.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
4	BRS	119	storage and S2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
5	BRS	84	router and S5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
6	BRS	176	crossroads.as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
7	BRS	21454	geoffrey.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
8	BRS	24	S7 and S8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
9	IS&R	3	(("7051147") or ("6738854") or ("6425035")).PN.	US-PGPUB; USPAT

	Time Stamp	Comments	Error Definition	Errors	Ref #
1	2010/07/22 15:13				S1
2	2010/07/22 15:14				S2
3	2010/07/22 15:15				S3
4	2010/07/22 15:15				S5
5	2010/07/22 15:15				S6
6	2010/08/25 15:35				S7
7	2010/08/25 15:35				S8
8	2010/08/25 15:35				S9
9	2010/09/08 12:21				S10

INFORMATION DISCLOSURE STATEMENT				Application Number	12/690,592
				Filing or 371 (c) Date:	January 20, 2010
				First Named Inventor	Geoffrey B. Hoese
				Group Art Unit	2182
				Examiner Name	Unknown
Sheet	1	of	1	Atty Docket Number	CROSS1120-33

NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published	T^2
	C172	QUESTIONING Mailed 06/08/2010 from JP Patent Application 526873/2000. 8 pages	06/08/10
	C173	Office Action Mailed 08/17/2010 in U.S. Serial No. 11/947,499 to Hoese. 6 pgs.	08/17/10

Examiner Signature	/Christopher Shin/	Date Considered	09/09/2010

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /C.S./

INFORMATION DISCLOSURE STATEMENT

Application Number	12/690,592
Filing or 371 (c) Date:	January 20, 2010
First Named Inventor	Geoffrey B. Hoese
Group Art Unit	2182
Examiner Name	Unknown
Atty Docket Number	CROSS1120-33

Sheet 1 of 1

NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published	T^2
	C171	American National Standard for Information Systems: Fibre Channel -- Cross-Point Switch Fabric Topology (FC-XS); X3T11/Project 959D/Rev 1.30. 114 pgs.	6/17/1994

Examiner Signature	/Christopher Shin/	Date Considered	08/26/2010

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /C.S./

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BIB DATA SHEET

CONFIRMATION NO. 8115

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
12/690,592	01/20/2010 RULE	710	2181	CROSS1120-33

APPLICANTS

Geoffrey B. Hoese, Austin, TX;
Jeffry T. Russell, Cibolo, TX;

**** CONTINUING DATA ***************************

This application is a CON of 12/552,885 09/02/2009
which is a CON of 11/851,724 09/07/2007 PAT 7,689,754
which is a CON of 11/442,878 05/30/2006 ABN *
which is a CON of 11/353,826 02/14/2006 PAT 7,340,549
which is a CON of 10/658,163 09/09/2003 PAT 7,051,147
which is a CON of 10/081,110 02/22/2002 PAT 6,789,152
which is a CON of 09/354,682 07/15/1999 PAT 6,421,753
which is a CON of 09/001,799 12/31/1997 PAT 5,941,972
(*)Data provided by applicant is not consistent with PTO records.

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

02/02/2010

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /CHRISTOPHER B SHIN/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		TX	2	53	3

ADDRESS

SPRINKLE IP LAW GROUP
1301 W. 25TH STREET
SUITE 408
AUSTIN, TX 78705
UNITED STATES

TITLE

STORAGE ROUTER AND METHOD FOR PROVIDING VIRTUAL LOCAL STORAGE

FILING FEE RECEIVED		
2806	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE	
REPLY TO OFFICE ACTION DATED 09/10/2010	Atty. Docket No. **CROSS1120-33**

Applicant **Geoffrey B. Hoese**	
Application Number **12/690,592**	Date Filed **01/20/10**
Title **Storage Router and Method for Providing Virtual Local Storage**	
Group Art Unit **2181**	Examiner **Shin, Christopher**
Confirmation Number: **8115**	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Certificate of Transmission Under 37 C.F.R. § 1.8

I hereby certify that this correspondence is being deposited electronically with the U.S. Patent and Trademark Office using the United States Patent and Trademark Office's EFS-Web system on **December 10, 2010.**

Delia Narvaiz

Dear Sir:

In response to the Official Action mailed September 10, 2010, Applicant respectfully requests the Examiner reconsider the rejections of the Claims in view of this reply.

IN THE SPECIFICATION:

Please replace paragraph [0001] with the following paragraph.

[0001] This application is a continuation of, and claims a benefit of priority under 35 U.S.C. 120 of the filing date of U.S. Patent Application Serial No. 12/552,885 entitled "Storage Router and Method for Providing Virtual Local Storage" filed 09/02/2009, which is a continuation of and claims the benefit of priority of U.S. Application Serial No. 11/851,724 entitled "Storage Router and Method for Providing Virtual Local Storage" filed 09/07/2007, now U.S. Patent No. 7,689,754 issued 03/30/2010, which is a continuation of and claims the benefit of priority of U.S. Patent Application Serial No. 11/442,878 entitled "Storage Router and Method for Providing Virtual Local Storage" filed 09/07/2007, now abandoned, which is a continuation of and claims the benefit of priority of U.S. Patent Application Serial No. 11/353,826 entitled "Storage Router and Method for Providing Virtual Local Storage" filed on 02/14/2006, now U.S. Patent No. 7,340,549 issued 03/04/2008, which is a continuation of and claims the benefit of priority of U.S. Patent Application Serial No. 10/658,163 entitled "Storage Router and Method for Providing Virtual Local Storage" filed on 09/09/2003 now U.S. Patent No. 7,051,147 issued 05/23/2006, which is a continuation of and claims the benefit of benefit of priority of U.S. Patent Application Serial No. 10/081,110 by inventors Geoffrey B. Hoese and Jeffery T. Russell, entitled "Storage Router and Method for Providing Virtual Local Storage" filed on 02/22/2002, now U.S. Patent No. 6,789,152 issued on 09/07/2004, which in turn is a continuation of and claims benefit of priority of U.S. Application No. 09/354,682 by inventors Geoffrey B. Hoese and Jeffrey T. Russell, entitled "Storage Router and Method for Providing Virtual Local Storage" filed on 07/15/1999, now U.S. Patent No. 6,421,753 issued on 07/16/2002, which in turn is a continuation of and claims benefit of priority of U.S. Patent Application Serial No. 09/001,799, filed on 12/31/1997, now U.S. Patent No. 5,941,972 issued on 08/24/1999, and hereby incorporates these applications and patents by reference in their entireties as if they had been fully set forth herein.

IN THE CLAIMS:

Please amend the claims as follows:

1. (Original) A storage router for providing virtual local storage on remote storage devices, comprising:

a first controller operable to interface with a first transport medium, wherein the first medium is a serial transport media; and

a processing device coupled to the first controller, wherein the processing device is configured to:

maintain a map to allocate storage space on the remote storage devices to devices connected to the first transport medium by associating representations of the devices connected to the first transport medium with representations of storage space on the remote storage devices, wherein each representation of a device connected to the first transport medium is associated with one or more representations of storage space on the remote storage devices;

control access from the devices connected to the first transport medium to the storage space on the remote storage devices in accordance with the map; and

allow access from devices connected to the first transport medium to the remote storage devices using native low level block protocol.

2. (Original)The storage router of Claim 1, wherein the map associates a representation of storage space on the remote storage devices with multiple devices connected to the first transport medium.

3. (Original)The storage router of Claim 1, wherein the storage space on the remote storage devices comprises storage space on multiple remote storage devices.

4. (Original)The storage router of Claim 1, wherein the map associates a representation of a device connected to the first transport medium with a representation of an entire storage space of at least one remote storage device.

5. (Original)The storage router of Claim 1, wherein the map resides at the storage router and is maintained at the storage router.

6. (Original)The storage router of Claim 1, wherein the native low level block protocol is received at the storage router via the first transport medium and the processing device uses the received native low level block protocol to allow the devices connected to the first transport medium access to storage space specifically allocated to them in the map.

7. (Original)The storage router of Claim 1, wherein the storage router is configured to receive commands according to a first low level block protocol from the device connected to the first transport medium and forward commands according to a second low level block protocol to the remote storage devices.

8. (Original)The storage router of Claim 7, wherein the first low level block protocol is an FCP protocol and the second low level block protocol is a protocol other than FCP.

9. (Original)The storage router of Claim 1, wherein the map comprises one or more tables.

10. (Original)The storage router of Claim 1, wherein the virtual local storage is provided to the devices connected to the first transport medium in a manner that is transparent to the devices and wherein the storage space allocated to the devices connected to the first transport medium appears to the devices as local storage.

11. (Original)The storage router of Claim 1, wherein the storage router provides centralized control of what the devices connected to the first transport medium see as local storage.

12. (Original)The storage router of Claim 1, wherein the representations of storage space comprise logical unit numbers that represent a subset of storage on the remote storage devices.

13. (Original)The storage router of Claim 12, wherein the storage router is operable to route requests to the same logical unit number from different devices connected to the first transport medium to different subsets of storage space on the remote storage devices.

14. (Original)The storage router of Claim 1, wherein the representations of devices connected to the first transport medium are unique identifiers.

15. (Original)The storage router of Claim 14, wherein the unique identifiers are world wide names.

16. (Original)The storage router of Claim 1, wherein the storage router is configured to allow modification of the map in a manner transparent to and without involvement of the devices connected to the first transport medium.

17. (Original)The storage router of Claim 1, wherein the processing device is a microprocessor.

18. (Original)The storage router of Claim 1, wherein the processing device is a microprocessor and associated logic to implement a stand-alone processing system.

19. (Original)The storage router of Claim 1, wherein the first transport medium is a fibre channel transport medium and further comprising a second transport medium connected to the remote storage devices that is a fibre channel transport medium.

20. (Original)A storage network comprising:

a set of devices connected a first transport medium, wherein the first transport medium;

a set of remote storage devices connected to a second transport medium;

a storage router connected to the serial transport medium;

a storage router connected to the first transport medium and second transport medium to provide virtual local storage on the remote storage devices, the storage router configured to:

maintain a map to allocate storage space on the remote storage devices to devices connected to the first transport medium by associating representations of the devices connected to the first transport medium with representations of storage space on the remote

storage devices, wherein each representation of a device connected to the first transport medium is associated with one or more representations of storage space on the remote storage devices;

control access from the devices connected to the first transport medium to the storage space on the remote storage devices in accordance with the map; and

allow access from devices connected to the first transport medium to the remote storage devices using native low level block protocol.

21. (Original)The storage network of Claim 20, wherein the map associates a representation of storage space on the remote storage devices with multiple devices connected to the first transport medium.

22. (Original)The storage network of Claim 20, wherein the storage space on the remote storage devices comprises storage space on multiple remote storage devices.

23. (Original)The storage network of Claim 20, wherein the map associates a representation of a device connected to the first transport medium with a representation of an entire storage space of at least one remote storage device.

24. (Original)The storage network of Claim 20, wherein the map resides at the storage router and is maintained at the storage router.

25. (Original)The storage network of Claim 20, wherein the native low level block protocol is received at the storage router via the first transport medium and the storage router uses the received native low level block protocol to allow the devices connected to the first transport medium access to storage space specifically allocated to them in the map.

26. (Original)The storage router of Claim 20, wherein the storage router is configured to receive commands according to a first low level block protocol from the device connected to the first transport medium and forward commands according to a second low level block protocol to the remote storage devices.

27. (Original)The storage network of Claim 20, wherein the first low level block protocol is an FCP protocol and the second low level block protocol is a protocol other than FCP.

28. (Original)The storage network of Claim 20, wherein the map comprises one or more tables.

29. (Original)The storage network of Claim 20, wherein the virtual local storage is provided to the devices connected to the first transport medium in a manner that is transparent to the devices and wherein the storage space allocated to the devices connected to the first transport medium appears to the devices as local storage.

30. (Original)The storage network of Claim 20, wherein the storage router provides centralized control of what the devices connected to the first transport medium see as local storage.

31. (Original)The storage network of Claim 20, wherein the representations of storage space comprise logical unit numbers that represent a subset of storage on the remote storage devices.

32. (Original)The storage network of Claim 31, wherein the storage router is operable to route requests to the same logical unit number from different devices connected to the first transport medium to different subsets of storage space on the remote storage devices.

33. (Original)The storage network of Claim 20, wherein the representations of devices connected to the first transport medium are unique identifiers.

34. (Original)The storage network of Claim 33, wherein the unique identifiers are world wide names.

35. (Original)The storage network of Claim 20, wherein the storage router is configured to allow modification of the map in a manner transparent to and without involvement of the devices connected to the first transport medium.

36. (Original)The storage network of Claim 20, wherein the first transport medium is a fibre channel transport medium and the second transport medium is a fibre channel transport medium.

37. (Original)A method for providing virtual local storage on remote storage devices comprising:

connecting a storage router between a set of devices connected to a first transport medium and a set of remote storage devices, wherein the first transport medium is a serial transport medium;

maintaining a map at the storage router to allocate storage space on the remote storage devices to devices connected to the first transport medium by associating representations of the devices connected to the first transport medium with representations of storage space on the remote storage devices, wherein each representation of a device connected to the first transport medium is associated with one or more representations of storage space on the remote storage devices;

controlling access from the devices connected to the first transport medium to the storage space on the remote storage devices in accordance with the map; and

allowing access from devices connected to the first transport medium to the remote storage devices using native low level block protocol.

38. (Original)The method of Claim 37, wherein the map associates a representation of storage space on the remote storage devices with multiple devices connected to the first transport medium.

39. (Original)The method of Claim 37, wherein the storage space on the remote storage devices comprises storage space on multiple remote storage devices.

40. (Original)The method of Claim 37, wherein the map associates a representation of a device connected to the first transport medium with a representation of an entire storage space of at least one remote storage device.

41. (Original)The method of Claim 37, wherein the map resides at the storage router and is maintained at the storage router.

42. (Original)The method of Claim 37, further comprising:

receiving the native low level block protocol at the storage router via the first transport medium;

using the received native low level block protocol at the storage router to allow the devices connected to the first transport medium access to storage space specifically allocated to them in the map.

43. (Original)The method of Claim 37, further comprising receiving commands at the storage router according to a first low level block protocol from the device connected to the first transport medium and forwarding commands according to a second low level block protocol to the remote storage devices.

44. (Original)The method of Claim 43, wherein the first low level block protocol is an FCP protocol and the second low level block protocol is a protocol other than FCP.

45. (Original)The method of Claim 37, wherein the map comprises one or more tables.

46. (Original)The method of Claim 37, wherein the virtual local storage is provided to the devices connected to the first transport medium in a manner that is transparent to the devices and wherein the storage space allocated to the devices connected to the first transport medium appears to the devices as local storage.

47. (Original)The method of Claim 37, wherein the storage router provides centralized control of what the devices connected to the first transport medium see as local storage.

48. (Original)The method of Claim 37, wherein the representations of storage space comprise logical unit numbers that represent a subset of storage on the remote storage devices.

49. (Original)The method of Claim 48, wherein the storage router is operable to route requests to the same logical unit number from different devices connected to the first transport medium to different subsets of storage space on the remote storage devices.

50. (Original)The method of Claim 37, wherein the representations of devices connected to the first transport medium are unique identifiers.

51. (Original)The method of Claim 50, wherein the unique identifiers are world wide names.

52. (Original)The method of Claim 51, wherein the storage router is configured to allow modification of the map in a manner transparent to and without involvement of the devices connected to the first transport medium.

53. (Original)The method of Claim 1 wherein connecting the storage router between a set of devices connected to a first transport medium and a set of remote storage devices further comprises connecting the storage router between a first fibre channel transport medium and a second fibre channel transport medium.

INTERVIEW SUMMARY

On August 30, 2010, John L. Adair and Examiner Shin held a telephonic interview regarding United States Patent Application Serial No. 11/947,499 (the "'499 Application"), United States Patent Application Serial No. 11/980,909 (the "'909 Application"), United States Patent Application Serial No. 12/552,885 and United States Patent Application Serial No. 12/552,913 and United States Patent Application No. 12/690,592 (the '592 Application). Applicant pointed out the transport mediums could be the same or different types of transport mediums and, for example, that i) the specification describes a Fibre Channel-to-Fibre Channel mode of operation and ii) issued United States Patent No. 7,051,147 claims a Fibre Channel-to-Fibre Channel system. Applicant also pointed out that other patents have issued that recite first and second transport mediums without requiring that the transport mediums use different protocols. The Examiner agreed that in the various cases, while the transport mediums may be different (e.g., separated by a storage router in the case of Claim 1 of the '499 Application), the transport mediums can use the same or different protocols and the 'low level block protocol' in the same medium types is consistent with the parent patents/specifications.

Furthermore, in the August 30, 2010 interview, Applicant pointed out that the term "remote" was construed to mean "indirectly connected through at least one serial network transport medium" (emphasis added). Crossroads v. Dot Hill Systems Corporation, Western District of Texas, Civil Action No. A-03-CA-754-SS. Therefore, the recitation of "remote" in various claims of the related applications addresses the fact that the transport mediums are different so that storage is indirectly connected to hosts (e.g., through a storage router in the case of Claim 1 of the '499 Application). Applicant agreed to review the claims of the related applications and specifically to amend the claims of the '909 Application to clarify that the storage devices are remote from the hosts. While Applicant and the Examiner discussed the other related cases generally, they did not discuss specific claims.

To the extent the Examiner's statement that one transport medium is "remote, separate and different" may be interpreted to mean anything different than that the transport mediums are different/separate so that storage is indirectly connected to hosts (e.g., through a storage router in the case of Claim 1 of the '499 Application) and that at least one of the transport mediums is a serial transport medium, Applicant disagrees with such an interpretation. As pointed out in the interview, the transport mediums can be the same type of transport mediums or different types of transport mediums.

Applicant agreed to file an updated terminal disclaimer and amend the Related Applications section as needed.

REMARKS

Applicant appreciates the time taken by the Examiner to review Applicant's present application. This application has been carefully reviewed in light of the Official Action mailed September 10, 2010. Applicant respectfully requests reconsideration and favorable action in this case.

Double Patenting Rejection

Claims 1-53 were rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims of U.S. Patent Nos. 7,051,147, 5,941,972, 7,340,549, 7,689,754, 7,552,266, 7,694,058, 6,421,753, 6,425,036, 6,425,035, 6,789,152, 6,738,854 and 6,763,419 and were provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over U.S. Patent Application Nos. 11/980,909, 11/947,499, 12/220,431, 12/552,807, 12/552,885, 12/552,913, 12/910,431, 12/910,375, 12/910,476 and 12/910,515. Applicant is including with this reply a timely filed terminal disclaimer in compliance with 37 C.F.R. § 1.321(c). U.S. Patent Nos. 7,051,147, 5,941,972, 7,340,549, 7,689,754, 7,552,266, 7,694,058, 6,421,753, 6,425,036, 6,425,035, 6,789,152, 6,738,854 and 6,763,419 and U.S. Patent Application Nos. 11/980,909, 11/947,499, 12/220,431, 12/552,807, 12/552,885, 12/552,913, 12/910,431, 12/910,375, 12/910,476 and 12/910,515 and the current Application are commonly owned. Accordingly, withdrawal of this rejection is respectfully requested.

Specification

The specification was objected to for informalities. An amended paragraph [0001] is submitted to update the related applications. Accordingly, withdrawal of this objection is requested.

IDS REFERENCES

Applicant filed information disclosure statements (IDS) citing the related art of record in the present application on May 21, 2010, June 9, 2010 and August 20, 2010. The Applicant notes that the Office Action mailed September 10, 2010 was accompanied by a copy of the listing of references, with an indication by the Examiner to indicate what references cited therein were considered.

Conclusion

Applicant has now made an earnest attempt to place this case in condition for allowance. Other than as explicitly set forth above, this reply does not include an acquiescence to statements, assertions, assumptions, conclusions, or any combination thereof in the Office Action. For the foregoing reasons and for other reasons clearly apparent, Applicant respectfully requests full allowance of Claims 1-53. The Examiner is invited to telephone the undersigned at the number listed below for prompt action in the event any issues remain.

The Director of the U.S. Patent and Trademark Office is hereby authorized to charge any fees or credit any overpayments to Deposit Account No. 50-3183 of Sprinkle IP Law Group.

Respectfully submitted,

Sprinkle IP Law Group
Attorneys for Applicant

John L. Adair
Reg. No. 48,828

Date: December 10, 2010

1301 W. 25th Street, Suite 408
Austin, TX 78705
Tel. (512) 637-9220
Fax. (512) 371-9088

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE	
Terminal Disclaimer	Atty. Docket No. **CROSS1120-33**

Applicant **Geoffrey B. Hoese, et al.**	
Application Number **12/690,592**	Date Filed **09/02/2009**
Title **STORAGE ROUTER AND METHOD FOR PROVIDING VIRTUAL LOCAL STORAGE**	
Group Art Unit **2181**	Examiner **SHIN, Christopher B.**
Confirmation Number: **5330**	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Certificate of Mailing

I hereby certify that this correspondence is being filed via electronically using the U.S. Patent Office EFS-Web system on December 10, 2010.

Delia Narvaez
Signature

Delia Narvaez
Printed Name

Crossroads Systems, Inc., the owner of one hundred percent (100%) interest in the instant application, except as provided below:

i) The terminal part of the statutory term of any patent granted on the instant application, which would extend beyond the expiration date of the full statutory term defined in 35 U.S.C. § 154 and 173 of U.S. Patent No. 5,941,972. In making the above disclaimer, the owner does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full statutory term as defined in 35 U.S.C. § 154 and 173 of U.S. Patent No. 5,941,972, in the event that it later: expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 C.F.R. 1.321, has all claims canceled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term.

ii) The terminal part of the statutory term of any patent granted on the instant application, which would extend beyond the expiration date of the full statutory term defined in 35 U.S.C. § 154 and 173 of U.S. Patent No. 6,421,753 as presently shortened by terminal disclaimer. In making the above disclaimer, the owner does not disclaim the terminal part of any patent

granted on the instant application that would extend to the expiration date of the full statutory term as defined in 35 U.S.C. § 154 and 173 of U.S. Patent No. 6,421,753, as presently shortened by terminal disclaimer, in the event that it later: expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 C.F.R. 1.321, has all claims canceled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term as presently shortened by terminal disclaimer.

iii) The terminal part of the statutory term of any patent granted on the instant application, which would extend beyond the expiration date of the full statutory term defined in 35 U.S.C. § 154 and 173, as presently shortened by terminal disclaimer, of U.S. Patent No. 6,425,036. In making the above disclaimer, the owner does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full statutory term as defined in 35 U.S.C. § 154 and 173 of U.S. Patent No. 6,425,036, as presently shorted by terminal disclaimer, in the event that it later: expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 C.F.R. 1.321, has all claims canceled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term, as presently shortened by any terminal disclaimer.

iv) The terminal part of the statutory term of any patent granted on the instant application, which would extend beyond the expiration date of the full statutory term defined in 35 U.S.C. § 154 and 173, as presently shortened by terminal disclaimer, of U.S. Patent No. 6,425,035. In making the above disclaimer, the owner does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full statutory term as defined in 35 U.S.C. § 154 and 173 of U.S. Patent No. 6,425,035, as presently shorted by terminal disclaimer, in the event that it later: expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 C.F.R. 1.321, has all claims canceled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term, as presently shortened by any terminal disclaimer.

v) The terminal part of the statutory term of any patent granted on the instant application, which would extend beyond the expiration date of the full statutory term defined in 35 U.S.C. § 154 and 173, as presently shortened by terminal disclaimer, of U.S. Patent No. 6,789,152. In making the above disclaimer, the owner does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full statutory term as defined in 35 U.S.C. § 154 and 173 of U.S. Patent No. 6,789,152, as presently shorted by terminal disclaimer, in the event that it later: expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 C.F.R. 1.321, has all claims canceled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term, as presently shortened by any terminal disclaimer.

vi) The terminal part of the statutory term of any patent granted on the instant application, which would extend beyond the expiration date of the full statutory term defined in 35 U.S.C. § 154 and 173, as presently shortened by terminal disclaimer, of U.S. Patent No. 6,738,854. In making the above disclaimer, the owner does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full statutory term as defined in 35 U.S.C. § 154 and 173 of U.S. Patent No. 6,738,854, as presently shorted by terminal disclaimer, in the event that it later: expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 C.F.R. 1.321, has all claims canceled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term, as presently shortened by any terminal disclaimer.

vii) The terminal part of the statutory term of any patent granted on the instant application, which would extend beyond the expiration date of the full statutory term defined in 35 U.S.C. § 154 and 173, as presently shortened by terminal disclaimer, of U.S. Patent No. 6,763,419. In making the above disclaimer, the owner does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full statutory term as defined in 35 U.S.C. § 154 and 173 of U.S. Patent No. 6,763,419, as presently shorted by terminal disclaimer, in the event that it later: expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 C.F.R. 1.321, has all claims canceled by

a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term, as presently shortened by any terminal disclaimer.

viii) The terminal part of the statutory term of any patent granted on the instant application, which would extend beyond the expiration date of the full statutory term defined in 35 U.S.C. § 154 and 173, as presently shortened by terminal disclaimer, of U.S. Patent No. 7,051,147. In making the above disclaimer, the owner does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full statutory term as defined in 35 U.S.C. § 154 and 173 of U.S. Patent No. 7,051,147, as presently shorted by terminal disclaimer, in the event that it later: expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 C.F.R. 1.321, has all claims canceled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term, as presently shortened by any terminal disclaimer.

ix) The terminal part of the statutory term of any patent granted on the instant application, which would extend beyond the expiration date of the full statutory term defined in 35 U.S.C. § 154 and 173, as presently shortened by terminal disclaimer, of U.S. Patent No. 7,340,549. In making the above disclaimer, the owner does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full statutory term as defined in 35 U.S.C. § 154 and 173 of U.S. Patent No. 7,340,549, as presently shorted by terminal disclaimer, in the event that it later: expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 C.F.R. 1.321, has all claims canceled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term, as presently shortened by any terminal disclaimer.

x) The terminal part of the statutory term of any patent granted on the instant application, which would extend beyond the expiration date of the full statutory term defined in 35 U.S.C. § 154 and 173, as presently shortened by terminal disclaimer, of U.S. Patent No. 7,689,754. In making the above disclaimer, the owner does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full statutory term as defined in 35 U.S.C. § 154 and 173 of U.S. Patent No. 7,689,754, as presently

shorted by terminal disclaimer, in the event that it later: expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 C.F.R. 1.321, has all claims canceled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term, as presently shortened by any terminal disclaimer.

xi) The terminal part of the statutory term of any patent granted on the instant application, which would extend beyond the expiration date of the full statutory term defined in 35 U.S.C. § 154 and 173, as presently shortened by terminal disclaimer, of U.S. Patent No. 7,552,266. In making the above disclaimer, the owner does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full statutory term as defined in 35 U.S.C. § 154 and 173 of U.S. Patent No. 7,552,266, as presently shorted by terminal disclaimer, in the event that it later: expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 C.F.R. 1.321, has all claims canceled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term, as presently shortened by any terminal disclaimer.

xii) The terminal part of the statutory term of any patent granted on the instant application, which would extend beyond the expiration date of the full statutory term defined in 35 U.S.C. § 154 and 173, as presently shortened by terminal disclaimer, of U.S. Patent No. 7,694,058. In making the above disclaimer, the owner does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full statutory term as defined in 35 U.S.C. § 154 and 173 of U.S. Patent No. 7,694,058, as presently shorted by terminal disclaimer, in the event that it later: expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 C.F.R. 1.321, has all claims canceled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term, as presently shortened by any terminal disclaimer.

xiii) The terminal part of the statutory term of any patent granted on the instant application, which would extend beyond the expiration date of the full statutory term of any patent granted on United States Patent Application No. 11/947,499 as defined in 35 U.S.C.

§ 154 and 173 as shortened by any terminal disclaimer filed prior to the grant of any patent on United States Patent Application No. 11/947,499. In making the above disclaimer, the owner does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full term as defined in 35 U.S.C. § 154 and 173 as shortened by any terminal disclaimer filed prior to the grant of any patent on United States Patent Application No. 11/947,499, in the event that any such patent granted on the co-pending application: expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 C.F.R. 1.321, has all claims canceled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term as shortened by any terminal disclaimer filed prior to its grant.

xiv) The terminal part of the statutory term of any patent granted on the instant application, which would extend beyond the expiration date of the full statutory term of any patent granted on United States Patent Application No. 12/220,431 as defined in 35 U.S.C. § 154 and 173 as shortened by any terminal disclaimer filed prior to the grant of any patent on United States Patent Application No. 12/220,431. In making the above disclaimer, the owner does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full term as defined in 35 U.S.C. § 154 and 173 as shortened by any terminal disclaimer filed prior to the grant of any patent on United States Patent Application No. 12/220,431, in the event that any such patent granted on the co-pending application: expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 C.F.R. 1.321, has all claims canceled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term as shortened by any terminal disclaimer filed prior to its grant.

xv) The terminal part of the statutory term of any patent granted on the instant application, which would extend beyond the expiration date of the full statutory term of any patent granted on United States Patent Application No. 11/980,909 as defined in 35 U.S.C. § 154 and 173 as shortened by any terminal disclaimer filed prior to the grant of any patent on United States Patent Application No. 11/980,909. In making the above disclaimer, the owner does not disclaim the terminal part of any patent granted on the instant application that would

extend to the expiration date of the full term as defined in 35 U.S.C. § 154 and 173 as shortened by any terminal disclaimer filed prior to the grant of any patent on United States Patent Application No. 11/980,909, in the event that any such patent granted on the co-pending application: expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 C.F.R. 1.321, has all claims canceled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term as shortened by any terminal disclaimer filed prior to its grant.

xvi) The terminal part of the statutory term of any patent granted on the instant application, which would extend beyond the expiration date of the full statutory term of any patent granted on United States Patent Application No. 12/552,885 as defined in 35 U.S.C. § 154 and 173 as shortened by any terminal disclaimer filed prior to the grant of any patent on United States Patent Application No. 12/552,885. In making the above disclaimer, the owner does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full term as defined in 35 U.S.C. § 154 and 173 as shortened by any terminal disclaimer filed prior to the grant of any patent on United States Patent Application No. 12/552,885, in the event that any such patent granted on the co-pending application: expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 C.F.R. 1.321, has all claims canceled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term as shortened by any terminal disclaimer filed prior to its grant.

xvii) The terminal part of the statutory term of any patent granted on the instant application, which would extend beyond the expiration date of the full statutory term of any patent granted on United States Patent Application No. 12/552,913 as defined in 35 U.S.C. § 154 and 173 as shortened by any terminal disclaimer filed prior to the grant of any patent on United States Patent Application No. 12/552,913. In making the above disclaimer, the owner does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full term as defined in 35 U.S.C. § 154 and 173 as shortened by any terminal disclaimer filed prior to the grant of any patent on United States Patent Application No. 12/552,913, in the event that any such patent granted on the co-pending

application: expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 C.F.R. 1.321, has all claims canceled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term as shortened by any terminal disclaimer filed prior to its grant.

xviii) The terminal part of the statutory term of any patent granted on the instant application, which would extend beyond the expiration date of the full statutory term of any patent granted on United States Patent Application No. 12/552,807 as defined in 35 U.S.C. § 154 and 173 as shortened by any terminal disclaimer filed prior to the grant of any patent on United States Patent Application No. 12/552,807. In making the above disclaimer, the owner does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full term as defined in 35 U.S.C. § 154 and 173 as shortened by any terminal disclaimer filed prior to the grant of any patent on United States Patent Application No. 12/552,807, in the event that any such patent granted on the co-pending application: expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 C.F.R. 1.321, has all claims canceled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term as shortened by any terminal disclaimer filed prior to its grant.

xix) The terminal part of the statutory term of any patent granted on the instant application, which would extend beyond the expiration date of the full statutory term of any patent granted on United States Patent Application No. 12/910,375 as defined in 35 U.S.C. § 154 and 173 as shortened by any terminal disclaimer filed prior to the grant of any patent on United States Patent Application No. 12/910,375. In making the above disclaimer, the owner does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full term as defined in 35 U.S.C. § 154 and 173 as shortened by any terminal disclaimer filed prior to the grant of any patent on United States Patent Application No. 12/910,375, in the event that any such patent granted on the co-pending application: expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 C.F.R. 1.321, has all claims canceled by a reexamination certificate, is reissued, or is

in any manner terminated prior to the expiration of its full statutory term as shortened by any terminal disclaimer filed prior to its grant

xx) The terminal part of the statutory term of any patent granted on the instant application, which would extend beyond the expiration date of the full statutory term of any patent granted on United States Patent Application No. 12/910,431 as defined in 35 U.S.C. § 154 and 173 as shortened by any terminal disclaimer filed prior to the grant of any patent on United States Patent Application No. 12/910,431. In making the above disclaimer, the owner does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full term as defined in 35 U.S.C. § 154 and 173 as shortened by any terminal disclaimer filed prior to the grant of any patent on United States Patent Application No. 12/910,431, in the event that any such patent granted on the co-pending application: expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 C.F.R. 1.321, has all claims canceled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term as shortened by any terminal disclaimer filed prior to its grant.

xxi) The terminal part of the statutory term of any patent granted on the instant application, which would extend beyond the expiration date of the full statutory term of any patent granted on United States Patent Application No. 12/910,476 as defined in 35 U.S.C. § 154 and 173 as shortened by any terminal disclaimer filed prior to the grant of any patent on United States Patent Application No. 12/910,476. In making the above disclaimer, the owner does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full term as defined in 35 U.S.C. § 154 and 173 as shortened by any terminal disclaimer filed prior to the grant of any patent on United States Patent Application No. 12/910,476, in the event that any such patent granted on the co-pending application: expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 C.F.R. 1.321, has all claims canceled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term as shortened by any terminal disclaimer filed prior to its grant

xxii) The terminal part of the statutory term of any patent granted on the instant application, which would extend beyond the expiration date of the full statutory term of any patent granted on United States Patent Application No. 12/910,515 as defined in 35 U.S.C. § 154 and 173 as shortened by any terminal disclaimer filed prior to the grant of any patent on United States Patent Application No. 12/910,515. In making the above disclaimer, the owner does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full term as defined in 35 U.S.C. § 154 and 173 as shortened by any terminal disclaimer filed prior to the grant of any patent on United States Patent Application No. 12/910,515, in the event that any such patent granted on the co-pending application: expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 C.F.R. 1.321, has all claims canceled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term as shortened by any terminal disclaimer filed prior to its grant

The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it, the above-referenced patents and the above-referenced co-pending applications are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

Check box 1, 2, 3, or 4 as appropriate.

1. ☐ For submission on behalf of an organization (e.g., corporation, partnership, university, government agency, etc.), the undersigned is empowered to act on behalf of the organization.

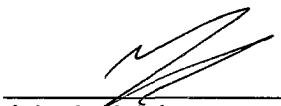
I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

* Statement under 37 C.R.F. 3.73(b) is required if terminal disclaimer is signed by the assignee (owner). Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

2. ☒ The undersigned is an attorney or agent of record.

3. ☐ Terminal disclaimer fee under 37 C.F.R. 1.20(d) included.

4. ☒ Terminal disclaimer fee under 37 C.F.R. 1.20(d). The Commissioner is hereby authorized to deduct $130.00 representing the above-noted filing fee from Deposit Account. No. 50-3183 of Sprinkle IP Law Group. The Commissioner is hereby further authorized to deduct any deficiencies or credit any overpayments regarding this application from the same account.



12-10-10

John L. Adair
Reg. No. 48,828

Dated

Electronic Patent Application Fee Transmittal

Application Number:	12690592
Filing Date:	20-Jan-2010
Title of Invention:	STORAGE ROUTER AND METHOD FOR PROVIDING VIRTUAL LOCAL STORAGE
First Named Inventor/Applicant Name:	Geoffrey B. Hoese
Filer:	John L. Adair/Delia Narvaiz
Attorney Docket Number:	CROSS1120-33

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Statutory or terminal disclaimer	1814	1	140	140
		Total in USD ($)		**140**

Electronic Acknowledgement Receipt

EFS ID:	9010738
Application Number:	12690592
International Application Number:	
Confirmation Number:	8115
Title of Invention:	STORAGE ROUTER AND METHOD FOR PROVIDING VIRTUAL LOCAL STORAGE
First Named Inventor/Applicant Name:	Geoffrey B. Hoese
Customer Number:	44654
Filer:	John L. Adair/Delia Narvaiz
Filer Authorized By:	John L. Adair
Attorney Docket Number:	CROSS1120-33
Receipt Date:	10-DEC-2010
Filing Date:	20-JAN-2010
Time Stamp:	15:14:59
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$140
RAM confirmation Number	1520
Deposit Account	503183
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		CROSS1120-33_ROA_121010.pdf	537418 6e59822f22b7f7497f1f7d6964bbad6891b63029	yes	14

Multipart Description/PDF files in .zip description

Document Description	Start	End
Amendment/Req. Reconsideration-After Non-Final Reject	1	1
Specification	2	2
Claims	3	10
Applicant summary of interview with examiner	11	12
Applicant Arguments/Remarks Made in an Amendment	13	14

Warnings:

Information:

2	Terminal Disclaimer Filed	CROSS1120-33_TD.pdf	616456 66a9e07300ed52edbfd6d6c196cff077829d7245	no	11

Warnings:

Information:

3	Fee Worksheet (PTO-875)	fee-info.pdf	30397 2ccb2d240efe13efa583b68a4c5d6a2d45cfcd56	no	2

Warnings:

Information:

Total Files Size (in bytes):	1184271

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT				Application Number	12/690,592
				Filing or 371 (c) Date:	January 20, 2010
				First Named Inventor	Geoffrey B. Hoese
				Group Art Unit	2182
				Examiner Name	Unknown
Sheet	1	of	1	Atty Docket Number	CROSS1120-33

NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published	T^2
	C174	Office Action Mailed 09/13/10 in U.S. Serial No. 11/980,909	09/13/10
	C175	Office Action Mailed 09/13/10 in U.S. Serial No. 12/552,807	09/13/10
	C176	Office Action Mailed 09/15/10 in U.S. Serial No. 12/552,885	09/15/10
	C177	Office Action Mailed 09/23/10 in U.S. Serial No. 12/552,913	09/23/10

Examiner Signature		Date Considered	

Electronic Patent Application Fee Transmittal

Application Number:	12690592
Filing Date:	20-Jan-2010
Title of Invention:	STORAGE ROUTER AND METHOD FOR PROVIDING VIRTUAL LOCAL STORAGE
First Named Inventor/Applicant Name:	Geoffrey B. Hoese
Filer:	John L. Adair/Delia Narvaiz
Attorney Docket Number:	CROSS1120-33

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
		Total in USD ($)		**180**

Electronic Acknowledgement Receipt

EFS ID:	9013238
Application Number:	12690592
International Application Number:	
Confirmation Number:	8115
Title of Invention:	STORAGE ROUTER AND METHOD FOR PROVIDING VIRTUAL LOCAL STORAGE
First Named Inventor/Applicant Name:	Geoffrey B. Hoese
Customer Number:	44654
Filer:	John L. Adair/Delia Narvaiz
Filer Authorized By:	John L. Adair
Attorney Docket Number:	CROSS1120-33
Receipt Date:	10-DEC-2010
Filing Date:	20-JAN-2010
Time Stamp:	16:54:55
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$180
RAM confirmation Number	3549
Deposit Account	503183
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		CROSS1120-33_IDS_121010.pdf	118713 b9af1228e38ca950f0fd60b2fb2fcf207db61d73	yes	3

Multipart Description/PDF files in .zip description

Document Description	Start	End
Transmittal Letter	1	2
Information Disclosure Statement (IDS) Filed (SB/08)	3	3

Warnings:

Information:

2	NPL Documents	CROSS1120_Ref_C174.pdf	164812 5039095bedf7274716acdd9b4726e1ccedccb4ca	no	7

Warnings:

Information:

3	NPL Documents	CROSS1120_Ref_C175.pdf	163965 8fcd974da4623a8ebce94e62a091e0e52cc0c2cd	no	7

Warnings:

Information:

4	NPL Documents	CROSS1120_Ref_C176.pdf	165757 21708767ba58acd885ba4bd417d71084f4dc1459	no	7

Warnings:

Information:

5	NPL Documents	CROSS1120_Ref_C177.pdf	166395 aaf9f5ef1eb835af156987ab4f354f6f0a206ba1	no	7

Warnings:

Information:

6	Fee Worksheet (PTO-875)	fee-info.pdf	30513 8e4cf3ec5a4643d4172cc328ca8997c2447b57d1	no	2

Warnings:

Information:

Total Files Size (in bytes):	810155

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

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New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Atty. Docket No. (Opt.) **CROSS1120-33**

Applicant **Geoffrey B. Hoese**	
Application Number **12/690,592**	Filing or 371 (c) Date: **January 20, 2010**
For **STORAGE ROUTER AND METHOD FOR PROVIDING VIRTUAL LOCAL STORAGE**	
Group Art Unit **2181**	Examiner **Shin, Christopher**
Confirmation Number: **8115**	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Certification of Transmission Under 37 C.F.R. 1.8

I hereby certify that this correspondence is being transmitted to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22312-1450 via the U.S. Patent and Trademark Office Electronic Filing System (EFS-Web) on **December 10, 2010.**

Delia Narvaiz

Dear Sir,

Applicant respectfully requests, pursuant to 37 C.F.R. §§ 1.56, 1.97 and 1.98, that the information listed on the attached SB08A/B form(s) be considered and cited in the examination of the above-identified application. A copy of U.S. Patent(s) and U.S. Patent Application Publication(s) listed on the attached SB08A form is not being submitted with this Information Disclosure Statement pursuant to the waiver of 37 C.F.R. § 1.98(a)(2)(i) by the U.S. Patent and Trademark Office. A copy of foreign patent documents as well as the information listed on the attached SB08B form is enclosed for the convenience of the Examiner.

☐ This Information Disclosure Statement is being submitted within three months of the filing date of a national application other than a continued prosecution application under 37 C.F.R. § 1.53(d).

☐ This Information Disclosure Statement is being submitted within three months of the date of entry of the national stage as set forth in 37 C.F.R. § 1.491 in an international application;

☐ This Information Disclosure Statement is being submitted before the mailing of a first Office action on the merits; or

☐ This Information Disclosure Statement is being submitted before the mailing of a first Office action after the filing of a request for continued examination under 37 C.F.R. § 1.114.

☒ This Information Disclosure Statement is being submitted after the period specified in 37 C.F.R. § 1.97(b) and before the mailing date of any of a final action under 37 C.F.R. § 1.113, a notice of allowance under 37 C.F.R. § 1.311, or an action that otherwise closes prosecution in the application, and is accompanied by one of:

- ☐ The statement specified in 37 C.F.R. § 1.97(e); or
- ☒ The fee set forth in 37 C.F.R. § 1.17(p). Applicant hereby authorizes the Commissioner to deduct the amount of $180 from Deposit Account No. 50-3183 of Sprinkle IP Law Group for the filing fee of this Information Disclosure Statement.

☐ This Information Disclosure Statement is being submitted after the period specified in 37 C.F.R. § 1.97(c) and on or before payment of the issue fee and is accompanied by:

- ☐ The statement specified in 37 C.F.R. § 1.97(e); and
- ☐ The fee set forth in 37 C.F.R. § 1.17(p). Applicant hereby authorizes the Commissioner to deduct the amount of $180 from Deposit Account No. 50-3183 of Sprinkle IP Law Group for the filing fee of this Information Disclosure Statement.

Applicant does not believe any fees are due for filing this Information Disclosure Statement; however, if Applicant is in error, the Director is hereby authorized to deduct any and all appropriate fees from Deposit Account 50-3183 of Sprinkle IP Law Group. Applicant respectfully submits that the claims of Applicant's above-referenced patent application are patentably distinguishable from the listed information.

Respectfully submitted,

Sprinkle IP Law Group
Attorneys for Applicant

John L. Adair
Reg. No. 48,828

Dated: December 10, 2010

1301 W. 25th Street, Suite 408
Austin, Texas 78705
Tel. (512) 637-9220
Fax. (512) 317-9088

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
12/690,592	01/20/2010	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 12/10/2010

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 53	Minus	** 53	= 0	X $ =		OR	X $52=	0
Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $ =		OR	X $220=	0
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/MARQUITA D. JONES/

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Atty. Docket No. (Opt.) **CROSS1120-33**

Applicant **Geoffrey B. Hoese**	
Application Number **12/690,592**	Filing or 371 (c) Date: **01/20/2010**
For **Storage Router and Method for Providing Virtual Local Storage**	
Group Art Unit **2181**	Examiner **Shin, Christopher**
Confirmation Number: **8115**	

Certification of Transmission Under 37 C.F.R. 1.8

I hereby certify that this correspondence is being transmitted to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22312-1450 via the U.S. Patent and Trademark Office Electronic Filing System (EFS-Web) on **December 17 2010**.

Janice Pampell

Janice Pampell

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir,

Applicant respectfully requests, pursuant to 37 C.F.R. §§ 1.56, 1.97 and 1.98, that the information listed on the attached SB08B form be considered and cited in the examination of the above-identified application. A copy of the information listed on the attached SB08B form is enclosed for the convenience of the Examiner.

☐ This Information Disclosure Statement is being submitted within three months of the filing date of a national application other than a continued prosecution application under 37 C.F.R. § 1.53(d).

☐ This Information Disclosure Statement is being submitted within three months of the date of entry of the national stage as set forth in 37 C.F.R. § 1.491 in an international application;

☐ This Information Disclosure Statement is being submitted before the mailing of a first Office action on the merits; or

☐ This Information Disclosure Statement is being submitted before the mailing of a first Office action after the filing of a request for continued examination under 37 C.F.R. § 1.114.

☒ This Information Disclosure Statement is being submitted after the period specified in 37 C.F.R. § 1.97(b) and before the mailing date of any of a final action under 37 C.F.R. § 1.113, a notice of allowance under 37 C.F.R. § 1.311, or an action that otherwise closes prosecution in the application, and is accompanied by one of:

☐ The statement specified in 37 C.F.R. § 1.97(e); or

☒ The fee set forth in 37 C.F.R. § 1.17(p). Applicant hereby authorizes the Commissioner to deduct the amount of $180 from Deposit Account No. 50-3183 of Sprinkle IP Law Group for the filing fee of this Information Disclosure Statement.

☐ This Information Disclosure Statement is being submitted after the period specified in 37 C.F.R. § 1.97(c) and on or before payment of the issue fee and is accompanied by:

☐ The statement specified in 37 C.F.R. § 1.97(e); and

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Applicant does not believe any fees are due for filing this Information Disclosure Statement; however, if Applicant is in error, the Director is hereby authorized to deduct any and all appropriate fees from Deposit Account 50-3183 of Sprinkle IP Law Group. Applicant respectfully submits that the claims of Applicant's above-referenced patent application are patentably distinguishable from the listed information.

Respectfully submitted,

Sprinkle IP Law Group
Attorneys for Applicant

John L. Adair
Reg. No. 48,828

Dated: Dec. 15, 2010

1301 W. 25th Street, Suite 408
Austin, Texas 78705
Tel. (512) 637-9220
Fax. (512) 317-9088

INFORMATION DISCLOSURE STATEMENT				Application Number	12/690,592
				Filing or 371 (c) Date:	January 20, 2010
				First Named Inventor	Geoffrey B. Hoese
				Group Art Unit	2181
				Examiner Name	Shin, Christopher
Sheet	1	of	1	Atty Docket Number	CROSS1120-33

NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published	T^2
	C179	Office Action Mailed 12/02/10 in U.S. Serial No. 12/910,375	12/2/2010
	C180	Office Action Mailed 12/03/10 in U.S. Serial No. 12/910,431	12/3/2010
	C181	Office Action Mailed 12/03/10 in U.S. Serial No. 12/910,515	12/3/2010

Examiner Signature		Date Considered	

Electronic Patent Application Fee Transmittal

Application Number:	12690592
Filing Date:	20-Jan-2010
Title of Invention:	STORAGE ROUTER AND METHOD FOR PROVIDING VIRTUAL LOCAL STORAGE
First Named Inventor/Applicant Name:	Geoffrey B. Hoese
Filer:	John L. Adair/Janice Pampell
Attorney Docket Number:	CROSS1120-33

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
		Total in USD ($)		**180**

Electronic Acknowledgement Receipt

EFS ID:	9062027
Application Number:	12690592
International Application Number:	
Confirmation Number:	8115
Title of Invention:	STORAGE ROUTER AND METHOD FOR PROVIDING VIRTUAL LOCAL STORAGE
First Named Inventor/Applicant Name:	Geoffrey B. Hoese
Customer Number:	44654
Filer:	John L. Adair/Janice Pampell
Filer Authorized By:	John L. Adair
Attorney Docket Number:	CROSS1120-33
Receipt Date:	17-DEC-2010
Filing Date:	20-JAN-2010
Time Stamp:	14:07:18
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$180
RAM confirmation Number	322
Deposit Account	503183
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)					
File Listing:					
Document Number	**Document Description**	**File Name**	**File Size(Bytes)/ Message Digest**	**Multi Part /.zip**	**Pages (if appl.)**
1	Information Disclosure Statement (IDS) Filed (SB/08)	CROSS1120-33_IDS_Filed_12-17-10.pdf	109107 80a5654afdcd449d01308e69e23ef5e486995055	no	3
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
2	NPL Documents	CROSS1120_Ref_C179.pdf	252415 ec33ebb937f62aea15cec67f0d4e7d15e2959906	no	7
Warnings:					
Information:					
3	NPL Documents	CROSS1120_Ref_C180.pdf	254399 845fbb723c26af4bb2f4aece8f061856a612c5a2	no	7
Warnings:					
Information:					
4	NPL Documents	CROSS1120_Ref_C181.pdf	218169 5781d9e2b8edee132dd11ed8d451ded236d11aa8	no	6
Warnings:					
Information:					
5	Fee Worksheet (PTO-875)	fee-info.pdf	30500 614355e9e496790e3524127de0acdbeaecdfc165	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	864590		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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NOTICE OF ALLOWANCE AND FEE(S) DUE

44654 7590 01/10/2011

Sprinkle IP Law Group
1301 W. 25th Street
Site 408
Austin, TX 78705

EXAMINER	
SHIN, CHRISTOPHER B	
ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 01/10/2011

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/690,592	01/20/2010	Geoffrey B. Hoese	CROSS1120-33	8115

TITLE OF INVENTION: STORAGE ROUTER AND METHOD FOR PROVIDING VIRTUAL LOCAL STORAGE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	04/11/2011

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

44654 7590 01/10/2011

Sprinkle IP Law Group
1301 W. 25th Street
Site 408
Austin, TX 78705

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/690,592	01/20/2010	Geoffrey B. Hoese	CROSS1120-33	8115

TITLE OF INVENTION: STORAGE ROUTER AND METHOD FOR PROVIDING VIRTUAL LOCAL STORAGE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	04/11/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
SHIN, CHRISTOPHER B	2181	710-305000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1_____

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2_____ 3_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/690,592	01/20/2010	Geoffrey B. Hoese	CROSS1120-33	8115

44654 7590 01/10/2011

Sprinkle IP Law Group
1301 W. 25th Street
Site 408
Austin, TX 78705

EXAMINER	
SHIN, CHRISTOPHER B	
ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 01/10/2011

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No.	Applicant(s)	
	12/690,592	HOESE ET AL.	
	Examiner	Art Unit	
	Christopher B. Shin	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the Amendment received December 10, 2010*.

2. ☒ The allowed claim(s) is/are *1-53*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date Multiple Pages filed
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Christopher B Shin/
Primary Examiner, Art Unit 2181

Search Notes

Application/Control No.	Applicant(s)/Patent under Reexamination
12/690,592	HOESE ET AL.
Examiner	**Art Unit**
Christopher B. Shin	2181

SEARCHED			
Class	Subclass	Date	Examiner
710	1-5,8-13,36-38,126-131	8/30/2010	CS
710	250, 305-	8/30/2010	CS
709	258	8/30/2010	CS
714	42	8/30/2010	CS
711	110-113	8/30/2010	CS

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner
710	**305,11**	12/15/2010	**CS**
709	258	12/15/2010	CS

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
PLUS from the parent cases	8/30/2010	CS
PALM- for double patenting	8/30/2010	CS
EAST (See notes for parent)	8/30/2010	CS
PARETN & RELATED CASES REVIEWED FOR THE ALOWANCE	8/30/2010	CS
Reviewed IDS	8/30/2010	CS

INFORMATION DISCLOSURE STATEMENT

Application Number	12/690,592
Filing or 371 (c) Date:	January 20, 2010
First Named Inventor	Geoffrey B. Hoese
Group Art Unit	2181
Examiner Name	Shin, Christopher
Atty Docket Number	CROSS1120-33

Sheet 1 of 1

NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published	T^2
	C179	Office Action Mailed 12/02/10 in U.S. Serial No. 12/910,375	12/2/2010
	C180	Office Action Mailed 12/03/10 in U.S. Serial No. 12/910,431	12/3/2010
	C181	Office Action Mailed 12/03/10 in U.S. Serial No. 12/910,515	12/3/2010

Examiner Signature	/Christopher Shin/	Date Considered	12/17/2010

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /C.S./

Issue Classification	Application/Control No. 12/690,592	Applicant(s)/Patent under Reexamination HOESE ET AL.
	Examiner Christopher B. Shin	Art Unit 2181

ISSUE CLASSIFICATION

ORIGINAL		INTERNATIONAL CLASSIFICATION									
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED				
710	305	G	06	F	13	/00	G	06	F	3	/0

CROSS REFERENCES															
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)														
710	11														
709	258														

---------- (Assistant Examiner) (Date)	/Christopher B Shin/ PRIMARY EXAMINER OF 2181 (Primary Examiner) (Date)	**Total Claims Allowed: 53**
(Legal Instruments Examiner) (Date)		O.G. Print Claim(s): 1 / O.G. Print Fig.: 3

☒ **Claims renumbered in the same order as presented by applicant** ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		31		61		91		121		151		181
	2		32		62		92		122		152		182
	3		33		63		93		123		153		183
	4		34		64		94		124		154		184
	5		35		65		95		125		155		185
	6		36		66		96		126		156		186
	7		37		67		97		127		157		187
	8		38		68		98		128		158		188
	9		39		69		99		129		159		189
	10		40		70		100		130		160		190
	11		41		71		101		131		161		191
	12		42		72		102		132		162		192
	13		43		73		103		133		163		193
	14		44		74		104		134		164		194
	15		45		75		105		135		165		195
	16		46		76		106		136		166		196
	17		47		77		107		137		167		197
	18		48		78		108		138		168		198
	19		49		79		109		139		169		199
	20		50		80		110		140		170		200
	21		51		81		111		141		171		201
	22		52		82		112		142		172		202
	23		53		83		113		143		173		203
	24		54		84		114		144		174		204
	25		55		85		115		145		175		205
	26		56		86		116		146		176		206
	27		57		87		117		147		177		207
	28		58		88		118		148		178		208
	29		59		89		119		149		179		209
	30		60		90		120		150		180		210

	Type	Hits	Search Text	DBs
1	IS&R	6	(("7340549") or ("7051147") or ("6789152") or ("6421753") or ("5941972") or ("20080307444")).PN.	US-PGPUB; USPAT

	Time Stamp	Comments	Error Definition	Errors	Ref #
1	2010/07/22 15:13				S1

INFORMATION DISCLOSURE STATEMENT				Application Number	12/690,592
				Filing or 371 (c) Date:	January 20, 2010
				First Named Inventor	Geoffrey B. Hoese
				Group Art Unit	2182
				Examiner Name	Unknown
Sheet	1	of	1	Atty Docket Number	CROSS1120-33

NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published	T^2
	C174	Office Action Mailed 09/13/10 in U.S. Serial No. 11/980,909	09/13/10
	C175	Office Action Mailed 09/13/10 in U.S. Serial No. 12/552,807	09/13/10
	C176	Office Action Mailed 09/15/10 in U.S. Serial No. 12/552,885	09/15/10
	C177	Office Action Mailed 09/23/10 in U.S. Serial No. 12/552,913	09/23/10

Examiner Signature	/Christopher Shin/	Date Considered	12/17/2010

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /C.S./

INFORMATION DISCLOSURE STATEMENT

Application Number	12/690,592
Filing or 371 (c) Date:	January 20, 2010
First Named Inventor	Geoffrey B. Hoese
Group Art Unit	2181
Examiner Name	Shin, Christopher
Atty Docket Number	CROSS1120-33

Sheet 1 of 1

NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published	T^2
	C179	Office Action Mailed 12/02/10 in U.S. Serial No. 12/910,375	12/2/2010
	C180	Office Action Mailed 12/03/10 in U.S. Serial No. 12/910,431	12/3/2010
	C181	Office Action Mailed 12/03/10 in U.S. Serial No. 12/910,515	12/3/2010

Examiner Signature	/Christopher Shin/	Date Considered	01/02/2011

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /C.S./

Application Number	Application/Control No.	Applicant(s)/Patent under Reexamination	
	12/690,592	HOESE ET AL.	

Document Code - DISQ	Internal Document – DO NOT MAIL

TERMINAL DISCLAIMER	☐ APPROVED	☒ DISAPPROVED
Date Filed : 12/10/10	This patent is subject to a Terminal Disclaimer	

Approved/Disapproved by:

Td has wrong filling date it should be 1/20/10 not 9/2/09.
Jean Proctor

U.S. Patent and Trademark Office

INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	12/690,592
				Filing Date	01/20/2010
				First Named Inventor	Geoffrey B. Hoese
				Group Art Unit	2111
				Examiner Name	Unknown
Sheet	7	of	9	Attorney Docket Number	CROSS1120-33

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number Number-Kind Code *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	A189	6,260,120	7/10/2001	Blumenau, et al.	
	A190	6,268,789	7/31/2001	Diamant, et al.	
	A191	6,308,247	10/23/2001	Ackerman	
	A192	6,330,629	12/11/2001	Kondo, et al.	
	A193	6,330,687	12/11/2001	Griffith	
	A194	6,341,315	1/22/2002	Arroyo, et al.	
	A195	6,343,324	1/29/2002	Hubis, et al.	
	A196	6,363,462	3/26/2002	Bergsten	
	A197	6,401,170	6/4/2002	Griffith, et al.	
	A198	6,421,753	7/16/2002	Hoese, et al.	
	A199	6,425,035	7/23/2002	Hoese, et al.	
	A200	6,425,036	7/23/2002	Hoese, et al.	
	A201	6,425,052	07/23/2002	Hashemi	
	A202	6,453,345	9/17/2002	Trcka, et al.	
	A203	6,484,245	11/19/2002	Sanada, et al.	
	A204	6,529,996	3/4/2003	Nguyen, et al.	
	A205	6,547,576	4/15/2003	Peng, et al.	
	A206	6,560,750	5/6/2003	Chien, et al.	
	A207	6,563,701	5/13/2003	Peng, et al.	
	A208	6,775,693	8/10/2004	Adams	
	A209	6,792,602	9/14/2004	Lin, et al.	
	A210	6,820,212	11/16/2004	Duchesne, et al.	
	A211	6,854,027	2/8/2005	Hsu, et al.	
	A212	6,862,637	3/1/2005	Stupar	
	A213	6,874,043	3/29/2005	Treggiden	
	A214	6,874,100	3/29/2005	Rauscher	
	A215	6,910,083	6/21/2005	Hsu, et al.	
	A216	7,065,076	6/20/2006	Nemazie	
	A217	7,127,668	10/24/2006	McBryde, et al.	
	A218	7,133,965	11/7/2006	Chien	

Change(s) applied to document, /A.E.M./ 3/17/2011

Examiner Signature	/Christopher Shin/	Date Considered	08/26/2010

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /C.S./

INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	12/690,592
				Filing Date	01/20/2010
				First Named Inventor	Geoffrey B. Hoese
				Group Art Unit	2111
				Examiner Name	Unknown
Sheet	4	of	9	Attorney Docket Number	CROSS1120-33

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number Number-Kind Code *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	A99	5,581,724	12/3/1996	Belsan et al.	
	A100	5,596,562	016/21/1997	Chen	
	A101	5,596,736	1/21/1997	Kerns	
	A102	5,598,541	1/28/1997	Malladi	
	A103	5,613,082	3/18/1997	Brewer, et al.	
	A104	5,621,902	4/15/1997	Cases, et al.	
	A105	5,632,012	5/20/1997	Belsan, et al.	
	A106	5,634,111	5/27/1997	Oeda, et al.	
	A107	5,638,518	6/10/1997	Malladi	
Change(s) applied to document, /A.E.M./ 3/17/2011	A108	5,642,515	6/24/1997	Jones, et al.	
	A109	5,659,756	8/19/1997	Hefferon, et al.	
	A110	5,664,107	9/2/1997	Chatwanni, et al.	
	A111	5,680,556	10/21/1997	Begun, et al.	
	A112	5,684,800	11/4/1997	Dobbins, et al.	
	A113	5,701,491	12/23/1997	Dunn, et al.	
	A114	5,712,976	1/27/1998	Falcon, et al.	
	A115	5,727,218	3/10/1998	Hotchkin	
	A116	5,729,705	3/17/1998	Weber	
	A117	5,743,847	4/28/1998	Nakamura, et al.	
	A118	5,748,924	5/5/1998	Llorens, et al.	
	A119	~~5,571,971~~ 5,751,971	5/12/1998	Dobbins, et al.	
	A120	5,751,975	5/12/1998	Gillespie, et al.	
	A121	5,764,931	6/9/1998	Schmahl, et al.	
	A122	5,768,623	6/16/1998	Judd, et al.	
	A123	5,774,683	6/30/1998	Gulick	
	A124	5,778,411	7/7/1998	DeMoss	
	A125	5,781,715	7/14/1998	Sheu	
	A126	5,802,278	9/1/1998	Isfeld, et al.	
	A127	5,805,816	9/8/1998	Picazo, Jr., et al.	
	A128	5,805,920	9/8/1998	Sprenkle, et al.	

Examiner Signature	/Christopher Shin/	Date Considered	08/26/2010

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /C.S./

INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	12/690,592
				Filing Date	01/20/2010
				First Named Inventor	Geoffrey B. Hoese
				Group Art Unit	2111
				Examiner Name	Unknown
Sheet	2	of	9	Attorney Docket Number	CROSS1120-33

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number Number-Kind Code *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	A39	5,212,785	5/18/1993	Powers, et al.	
	A40	5,214,778	5/25/1993	Glider, et al.	
	A41	5,226,143	7/6/1993	Baird, et al.	
	A42	5,239,632	8/24/1993	Larner	
	A43	5,239,643	8/24/1993	Blount, et al.	
	A44	5,239,654	8/24/1993	Ing-Simmons, et al.	
	A45	5,247,638	9/21/1993	O'Brien, et al.	
	A46	5,247,692	9/21/1993	Fujimura	
	A47	5,257,386	10/26/1993	Saito	
	A48	5,297,262	3/22/1994	Cox, et al.	
	A49	5,301,290	4/5/1994	Tetzlaff, et al.	
	A50	5,315,657	5/24/1994	Abadi, et al.	
	A51	5,317,693	5/31/1994	Elko, et al.	
	A52	5,331,673	7/19/1994	Elko, et al.	
	A53	5,347,384	9/13/1994	McReynolds, et al.	
	A54	5,355,453	10/11/1994	Glider, et al.	
	A55	5,361,347	11/1/1994	Glider, et al.	
	A56	5,367,646	11/22/1994	Pardillos, et al.	
	A57	5,379,385	1/3/1995	Shomler	
	A58	5,379,398	1/3/1995	Cohn, et al.	
	A59	5,388,243	2/7/1995	Glider, et al.	
	A60	5,388,246	2/7/1995	Kasi	
	A61	5,394,402	2/28/1995	Ross, et al.	
	A62	5,394,526	2/28/1995	Crouse et al.	
	A63	5,396,596	3/7/1995	Hashemi, et al.	
	A64	5,403,639	4/4/1995	Belsan, et al.	
Change(s) applied	A65	5,410,667	4/25/1995	Belsan, et al.	
to document,	A66	5,410,697	4/25/1995	Baird, et al.	
/A.E.M./	A67	5,414,820	05/9/1995	McFarland, et al.	
3/17/2011	A68	5,416,915	5/16/1995	Mattson, et al.	

Examiner Signature	/Christopher Shin/	Date Considered	08/26/2010

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /C.S./

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

44654 7590 01/10/2011

Sprinkle IP Law Group
1301 W. 25th Street
Site 408
Austin, TX 78705

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Janice Pampell	(Depositor's name)
Janice Pampell	(Signature)
March 21, 2011	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/690,592	01/20/2010	Geoffrey B. Hoese	CROSS1120-33	8115

TITLE OF INVENTION: STORAGE ROUTER AND METHOD FOR PROVIDING VIRTUAL LOCAL STORAGE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	04/11/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
SHIN, CHRISTOPHER B	2181	710-305000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Sprinkle IP Law
2 Group
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Crossroads Systems, Inc. Austin, TX

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 50-3183 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date 3/21/11

Typed or printed name Ari G. Akmal Registration No. 51,388

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE	
AMENDMENT UNDER 37 CFR 1.312	Atty. Docket No. (Opt.) **CROSS1120-33**

Applicants: **Geoffrey B. Hoese**	
Application Number **12/690,592**	Filed **01/20/2010**
For: **Storage Router and Method for Providing Virtual Local Storage**	
Group Art Unit **2181**	Confirmation Number: **8115**

Mail Stop: Issue Fee

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

Dear Sir:

Certification Under 37 C.F.R. §1.10

I hereby certify that this correspondence is being deposited electronically with the U.S. Patent and Trademark Office using the United States Patent and Trademark Office's EFS-Web system on 3/2/11

Janice Pampell

A Notice of Allowance and Fee(s) Due was issued by the Examiner on January 10, 2011. The Applicant therefore respectfully requests that the Examiner enter the following amendment under 37 CFR 1.312. While Applicant understands that entry of an Amendment after the notice of allowance is a matter of discretion and not of right, Applicant respectfully requests that the Examiner consider and enter the following changes to the specification.

Please amend the application as follows:

IN THE SPECIFICATION

Following the title, please replace the first paragraph of page one the following paragraph:

[0001] [0001] This application is a continuation of, and claims a benefit of priority under 35 U.S.C. 120 of the filing date of U.S. Patent Application Serial No. 12/552,885 entitled "Storage Router and Method for Providing Virtual Local Storage" filed 09/02/2009, which is a continuation of and claims the benefit of priority of U.S. Application Serial No. 11/851,724 entitled "Storage Router and Method for Providing Virtual Local Storage" filed 09/07/2007, now U.S. Patent No. 7,689,754 issued 03/30/2010, which is a continuation of and claims the benefit of priority of U.S. Patent Application Serial No. 11/442,878 entitled "Storage Router and Method for Providing Virtual Local Storage" filed 05/30/2006, now abandoned, which is a continuation of and claims the benefit of priority of U.S. Patent Application Serial No. 11/353,826 entitled "Storage Router and Method for Providing Virtual Local Storage" filed on 02/14/2006, now U.S. Patent No. 7,340,549 issued 03/04/2008, which is a continuation of and claims the benefit of priority of U.S. Patent Application Serial No. 10/658,163 entitled "Storage Router and Method for Providing Virtual Local Storage" filed on 09/09/2003 now U.S. Patent No. 7,051,147 issued 05/23/2006, which is a continuation of and claims the benefit of benefit of priority of U.S. Patent Application Serial No. 10/081,110 by inventors Geoffrey B. Hoese and Jeffery T. Russell, entitled "Storage Router and Method for Providing Virtual Local Storage" filed on 02/22/2002, now U.S. Patent No. 6,789,152 issued on 09/07/2004, which in turn is a continuation of and claims benefit of priority of U.S. Application No. 09/354,682 by inventors Geoffrey B. Hoese and Jeffrey T. Russell, entitled "Storage Router and Method for Providing Virtual Local Storage" filed on 07/15/1999, now U.S. Patent No. 6,421,753 issued on 07/16/2002, which in turn is a continuation of and claims benefit of priority of U.S. Patent Application Serial No. 09/001,799, filed on 12/31/1997, now U.S. Patent No. 5,941,972 issued on 08/24/1999, and hereby incorporates these applications and patents by reference in their entireties as if they had been fully set forth herein.

REMARKS

Applicants appreciate the time taken by the Examiner to review the present amendment.

Applicant submits that the priority information in the new paragraph above was recognized by the United States Patent and Trademark office as shown by its inclusion in the official filing receipt. It is respectfully submitted that the amendment does not affect the merits of the application and is proper subject matter for an Amendment Under 37 CFR 1.312. The Applicant therefore respectfully requests entry of the amendment.

The Commissioner is hereby authorized to charge any deficiencies or credit any overpayment to Deposit Account No. 50-3183.

Respectfully submitted,

Sprinkle IP Law Group

Ari G. Akmal
Reg. No. 51,388

Dated: March 21, 2011

1301 W. 25th Street, Suite 408
Austin, Texas 78705
Tel. 512-637-9220
Fax. 512-371-9088

Electronic Patent Application Fee Transmittal

Application Number:	12690592
Filing Date:	20-Jan-2010
Title of Invention:	STORAGE ROUTER AND METHOD FOR PROVIDING VIRTUAL LOCAL STORAGE
First Named Inventor/Applicant Name:	Geoffrey B. Hoese
Filer:	Ari G. Akmal/Janice Pampell
Attorney Docket Number:	CROSS1120-33

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1510	1510
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1810**

Electronic Acknowledgement Receipt

EFS ID:	9696893
Application Number:	12690592
International Application Number:	
Confirmation Number:	8115
Title of Invention:	STORAGE ROUTER AND METHOD FOR PROVIDING VIRTUAL LOCAL STORAGE
First Named Inventor/Applicant Name:	Geoffrey B. Hoese
Customer Number:	44654
Filer:	Ari G. Akmal/Janice Pampell
Filer Authorized By:	Ari G. Akmal
Attorney Docket Number:	CROSS1120-33
Receipt Date:	21-MAR-2011
Filing Date:	20-JAN-2010
Time Stamp:	11:47:44
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$1810
RAM confirmation Number	8781
Deposit Account	503183
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	CROSS1120-33_Transmittal_of_Payment_of_Issue_Fee.pdf	38692 0ed3d30a44ed45ee1cf37580d97b0bbad11eb3ba	no	1
Warnings:					
Information:					
2	Issue Fee Payment (PTO-85B)	CROSS1120-33_PTOL-85.pdf	96691 2081e8bddfd0c06c1b420644747322b881b52ec5	no	1
Warnings:					
Information:					
3	Amendment after Notice of Allowance (Rule 312)	CROSS1120-33_Amendment_Under_312.pdf	104947 3146295b48db3e23309885ba8408b8a8cf7cd713	no	3
Warnings:					
Information:					
4	Fee Worksheet (PTO-875)	fee-info.pdf	31982 35c157186b5d2bc9d857dba7280faf1357b9fdc8	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	272312		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

TRANSMITTAL OF PAYMENT OF ISSUE FEE (LARGE Entity) 37 C.F.R. 1.311)	Docket No. CROSS1120-33

Applicant(s) Geoffrey B. Hoese				
Application No.	Filing Date	Examiner	Group Art Unit	Confirmation No.
12/690,592	01/20/2010	SHIN, Christopher B.	2181	8115

Title:
STORAGE ROUTER AND METHOD FOR PROVIDING VIRTUAL LOCAL STORAGE

Mail Stop: Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Transmitted herewith are the following items in reference to the above-identified application:

- ☒ Issue Fee Transmittal Form PTOL-85
- ☒ Issue Fee: $1,510.00
- ☒ Publication Fee $300.00
- ☒ Amendment Under 1.312
- ☒ The Director is hereby authorized to charge Deposit Account No. 50-3183 of Sprinkle IP Law Group.
- ☒ The Director is hereby authorized to charge any deficiencies or credit any overpayments to Deposit Account No. 50-3183 of Sprinkle IP Law Group.

Ari G. Akmal
Reg. No. 48,828

Customer No. 44654
Sprinkle IP Law Group
1301 W. 25th Street, Suite 408
Austin, Texas 78705
Tel. (512) 637-9220
Fax. (512) 371-9088

Certificate of Transmission Under 37 C.F.R. § 1.8

I hereby certify that this correspondence is being deposited electronically with the U.S. Patent and Trademark Office using the United States Patent and Trademark Office's EFS-Web system on 3/21/11

Janice Pampell

Janice Pampell

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/690,592	01/20/2010	Geoffrey B. Hoese	CROSS1120-33	8115

44654 7590 03/23/2011

Sprinkle IP Law Group
1301 W. 25th Street
Suite 408
Austin, TX 78705

EXAMINER	
SHIN, CHRISTOPHER B	
ART UNIT	**PAPER NUMBER**
2181	

MAIL DATE	DELIVERY MODE
03/23/2011	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Response to Rule 312 Communication	Application No.	Applicant(s)
	12/690,592	HOESE ET AL.
	Examiner	Art Unit

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

1. ☒ The amendment filed on *21 March 2011* under 37 CFR 1.312 has been considered, and has been:

   a) ☒ entered.

   b) ☐ entered as directed to matters of form not affecting the scope of the invention.

   c) ☐ disapproved because the amendment was filed after the payment of the issue fee.
   Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.

   d) ☐ disapproved. See explanation below.

   e) ☐ entered in part. See explanation below.

Timothy Caldwell
Publishing Division

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/690,592	04/26/2011	7934041	CROSS1120-33	8115

44654 7590 04/06/2011

Sprinkle IP Law Group
1301 W. 25th Street
Suite 408
Austin, TX 78705

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Geoffrey B. Hoese, Austin, TX;
Jeffry T. Russell, Cibolo, TX;

PTO/SB/44 (09/07)
Approved for use through 08/31/2013. OMB 0651-0033
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. **7,934,041**

APPLICATION NO.: **12/690,592**

ISSUE DATE: **04/26/2011**

INVENTOR(S): **Geoffrey B. Hoese, et al.**

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Claim 20:

A set of devices connected --to-- a first transport medium, wherein the first transport medium --is a serial transport medium--;

MAILING ADDRESS OF SENDER:

Customer No. 44654
Sprinkle IP Law Group
1301 W. 25th Street, Suite 408
Austin, Texas 78705
Tel. (512) 637-9220
Fax. (512) 371-9088

Electronic Patent Application Fee Transmittal

Application Number:	12690592
Filing Date:	20-Jan-2010
Title of Invention:	STORAGE ROUTER AND METHOD FOR PROVIDING VIRTUAL LOCAL STORAGE
First Named Inventor/Applicant Name:	Geoffrey B. Hoese
Filer:	John L. Adair/Janice Pampell
Attorney Docket Number:	CROSS1120-33

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Certificate of correction	1811	1	100	100
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
			Total in USD ($)	**100**

Electronic Acknowledgement Receipt

EFS ID:	10490129
Application Number:	12690592
International Application Number:	
Confirmation Number:	8115
Title of Invention:	STORAGE ROUTER AND METHOD FOR PROVIDING VIRTUAL LOCAL STORAGE
First Named Inventor/Applicant Name:	Geoffrey B. Hoese
Customer Number:	44654
Filer:	John L. Adair/Janice Pampell
Filer Authorized By:	John L. Adair
Attorney Docket Number:	CROSS1120-33
Receipt Date:	11-JUL-2011
Filing Date:	20-JAN-2010
Time Stamp:	15:20:53
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$100
RAM confirmation Number	1837
Deposit Account	503183
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	CROSS1120-33_Transmittal_Letter.pdf	34484 225180843b7e05f6c5ae82d25f3193d2f695dd6d	no	1
Warnings:					
Information:					
2	Request for Certificate of Correction	CROSS1120-33_Certificate_of_Correction.pdf	31604 39defa7b887e73ea1a92b03836649154ba03f765	no	1
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30191 d67fb2524cf07f864b91d8088e775d1e1c54d8dc	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	96279		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE	
TRANSMITTAL LETTER	Atty. Docket No. **CROSS1120-33**

Applicant **Geoffrey B. Hoese, et al.**	
Application No. **12/690,592**	Filing Date **01/20/2010**
Patent Number **7,934,041**	Issue Date **04/26/2011**
For **Storage Router and Method for Providing Virtual Local Storage**	
Confirmation No. **8115**	

Attention: Certificate of Correction Branch
Office of Patent Publication
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Certificate of Mailing Under 37 C.F.R. 1.8

I hereby certify that this correspondence is being deposited with the U.S. Patent Office using the United States Patent and Trademark Office's EFS-Web system on 7-11-11

Janice Pampell
Janice Pampell

Transmitted herewith for filing in the above-identified Patent is a Certificate of Correction. The error noted on the Certificate of Correction is on the part of the Applicant. The Commissioner is hereby authorized to charge the appropriate fee against Deposit Account No. 50-3183 of Sprinkle IP Law Group.

Respectfully submitted,
SPRINKLE IP LAW GROUP

John L. Adair
Reg. No. 48,828

Date: 7-8, 2011

Sprinkle IP Law Group
1301 W. 25th Street
Suite 408
Austin, Texas 78705
Tel. (512) 637-9225
Fax. (512) 371-9088

SPE RESPONSE FOR CERTIFICATE OF CORRECTION

DATE : 7/19/2011

TO SPE OF : ART UNIT 2181

SUBJECT : Request for Certificate of Correction for Appl. No.: 12/690592 Patent No.: 7934041 B2

CofC mailroom date: 7/11/2011

Please respond to this request for a certificate of correction within 7 days.

FOR IFW FILES:

Please review the requested changes/corrections as shown in the **COCIN** document(s) in the IFW application image. No new matter should be introduced, nor should the scope or meaning of the claims be changed.

Please complete the response (see below) and forward the completed response to scanning using document code **COCX**.

FOR PAPER FILES:

Please review the requested changes/corrections as shown in the attached certificate of correction. Please complete this form (see below) and forward it with the file to:

Certificates of Correction Branch (CofC)
Randolph Square – 9D10-A
Palm Location 7580

Note: _____

_____

Virginia Tolbert

Certificates of Correction Branch

(571) 272-0460

Thank You For Your Assistance

The request for issuing the above-identified correction(s) is hereby:
Note your decision on the appropriate box.

- ☐ **Approved** — **All** changes apply.
- ☐ **Approved in Part** — Specify below which changes **do not** apply.
- ☐ **Denied** — State the reasons for denial below.

Comments: _____

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_____ _____

SPE **Art Unit**

SPE RESPONSE FOR CERTIFICATE OF CORRECTION

DATE : 7/19/2011

TO SPE OF : ART UNIT 2181

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Please complete the response (see below) and forward the completed response to scanning using document code **COCX**.

FOR PAPER FILES:

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Certificates of Correction Branch (CofC)
Randolph Square – 9D10-A
Palm Location 7580

Note: _____

_____

Virginia Tolbert

Certificates of Correction Branch

(571) 272-0460

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The request for issuing the above-identified correction(s) is hereby:
Note your decision on the appropriate box.

- ☒ **Approved** — **All** changes apply.
- ☐ **Approved in Part** — Specify below which changes **do not** apply.
- ☐ **Denied** — State the reasons for denial below.

Comments: _____

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Clifford W. [illegible] 2181

SPE **Art Unit**

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.	: 7,934,041 B2
APPLICATION NO.	: 12/690592
DATED	: April 26, 2011
INVENTOR(S)	: Geoffrey B. Hoese et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Claim 20: Col. 10 line 56 should read -

A set of devices connected --to-- a first transport medium, wherein the first transport medium --is a serial transport medium--;

Signed and Sealed this
Thirteenth Day of September, 2011

David J. Kappos

David J. Kappos
Director of the United States Patent and Trademark Office

AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Western District of Texas, Austin Division on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
1:12-CV-104 SS	2/1/2012	Western District of Texas, Austin Division

PLAINTIFF	DEFENDANT
Crossroads Systems, Inc.	Infortrend Corporation; Aberdeen LLC; Boost Systems, Inc.; iXsystems, Inc.; and Storageflex, Inc.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	see attached		
2	6,425,035		
3	7,051,147		
4	7,934,041		
5	7,934,040		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 7,987,311		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
William G. Putnicki	Olga Schroed	2/2/2012

Copy 1—Upon initiation of action, mail this copy to Director **Copy 3—Upon termination of action, mail this copy to Director**
Copy 2—Upon filing document adding patent(s), mail this copy to Director **Copy 4—Case file copy**

infringement, by way of actively inducing infringement and/or contributing to the infringement of the '147 Patent by users of Defendant Boost products, such as EonStor Fibre-to-Fibre RAID Systems by, among other things, making, using, offering for sale, selling, importing into the United States, marketing, supporting, providing product instruction, and/or advertising certain of its products, including the EonStor Fibre-to-Fibre RAID Systems.

32. Further, Defendant Storageflex has been and now is indirectly infringing the '147 Patent, with knowledge of the patent and knowledge that its induced acts constitute patent infringement, by way of actively inducing infringement and/or contributing to the infringement of the '147 Patent by users of Defendant Storageflex's products, such as the FF1124 by, among other things, making, using, offering for sale, selling, importing into the United States, marketing, supporting, promoting, providing product instruction, and/or advertising certain of its products and/or certain components for use with Storageflex's products, including the FF1124 and/or components for use with same.

33. Defendants Infortrend, Boost and Storageflex have been on notice of the '147 Patent since before this lawsuit through notification by letter (Boost, Storageflex), prior involvement in litigation involving the '147 Patent (Infortrend), and/or purchase of a marked product (Storageflex), and have not ceased their infringing activities. The infringement of the '147 Patent by Defendants Infortrend, Boost and Storageflex has been and continues to be willful and deliberate.

34. Crossroads has been irreparably harmed by each of Defendant Infortrend's, Boost's and Storageflex's acts of infringement of the '147 Patent and will continue to be harmed unless and until each of Defendant Infortrend's, Boost's and Storageflex's acts of infringement are enjoined and restrained by order of this Court.

35. As a result of the acts of infringement of the '147 Patent by Defendants Infortrend, Boost and Storageflex, Crossroads has suffered and will continue to suffer damages in an amount to be proven at trial.

COUNT 3: INFRINGEMENT OF U.S. PATENT NO. 7,934,041

36. Crossroads incorporates by reference the allegations set forth in the preceding paragraphs.

37. On April 26, 2011, United States Patent No. 7,934,041 (the "'041 Patent") was duly and legally issued. A true and correct copy of the '041 Patent is attached hereto as Exhibit C. Crossroads is the assignee and the owner of all right, title, and interest in and to the '041 Patent. The '041 Patent is entitled to a presumption of validity.

38. Defendants Infortrend, Aberdeen, Boost, iXsystems and Storageflex have directly infringed the '041 Patent. On information and belief, the Defendants continue to directly infringe the '041 Patent.

39. Specifically, each of the Defendants has directly infringed the '041 Patent by making, using, offering for sale, selling and/or importing into the United States certain of their products including at least the following: EonStor RAID Systems with Fibre Host Interface and/or iSCSI Host Interface, EonStor DS RAID Systems with Fibre Host Interface and/or iSCSI Host Interface, ESVA iSCSI Host Series and ESVA Fibre Host Series (Infortrend); XDAS D-Series RAID Systems with FC and/or iSCSI Host, XDAS iSCSI Series RAID Systems, XDAS F8 Series RAID Systems and Aberdeen P8 XDAS with Fibre Host Interface (Aberdeen); EonStor RAID Systems with Fibre Host Interface and/or iSCSI Host Interface, EonStor DS RAID Systems with Fibre Host Interface and/or iSCSI Host Interface, ESVA iSCSI Host Series and ESVA Fibre Host Series (Boost); Titan 316F, Titan 424F, ESVA iSCSI Host Series and

ESVA Fibre Host Series (iXsystems); and FF1124 and HA3969 with FC or iSCSI Host Interfaces (Storageflex).

40. Further, Defendant Aberdeen has been and now is indirectly infringing the '041 Patent, with knowledge of the patent and knowledge that its induced acts constitute patent infringement, by way of actively inducing infringement and/or contributing to the infringement of the '041 Patent by users of Defendant Aberdeen's products, such as XDAS D-Series RAID Systems with FC and/or iSCSI Host, XDAS iSCSI Series RAID Systems, XDAS F8 Series RAID Systems and Aberdeen P8 XDAS with Fibre Host Interface by among other things, making, using, offering for sale, selling, importing into the United States, marketing, supporting, providing product instruction, and/or advertising certain of Defendant Aberdeen's products, including XDAS D-Series RAID Systems with FC and/or iSCSI Host, XDAS iSCSI Series RAID Systems, XDAS F8 Series RAID Systems and Aberdeen P8 XDAS with Fibre Host Interface.

41. Further, Defendant Boost has been and now is indirectly infringing the '041 Patent, with knowledge of the patent and knowledge that its induced acts constitute patent infringement, by way of actively inducing infringement and/or contributing to the infringement of the '041 Patent by users of Defendant Boost's products, such as EonStor RAID Systems with Fibre Host Interface and/or iSCSI Host Interface, EonStor DS RAID Systems with Fibre Host Interface and/or iSCSI Host Interface, ESVA iSCSI Host Series, and ESVA Fibre Host Series by among other things, making, using, offering for sale, selling, importing into the United States, marketing, supporting, providing product instruction, and/or advertising certain of Defendant Boost's products, including the EonStor RAID Systems with Fibre Host Interface and/or iSCSI

Host Interface, EonStor DS RAID Systems with Fibre Host Interface and/or iSCSI Host Interface, ESVA iSCSI Host Series, and ESVA Fibre Host Series.

42. Further, Defendant iXsystems has been and now is indirectly infringing the '041 Patent, with knowledge of the patent, by way of contributing to the infringement of the '041 Patent by users of Defendant iXsystems' products, such as Titan 316F, Titan 424F, ESVA iSCSI Host Series, and ESVA Fibre Host Series by among other things, offering for sale, selling, and/or importing into the United States certain of Defendant iXsystems' products, including Titan 316F, Titan 424F, ESVA iSCSI Host Series, and/or ESVA Fibre Host Series.

43. Further, Defendant Storageflex has been and now is indirectly infringing the '041 Patent, with knowledge of the patent and knowledge that its induced acts constitute patent infringement, by way of actively inducing infringement and/or contributing to the infringement of the '041 Patent by users of Defendant Storageflex's products, such as the FF1124 and HA3969 with FC or iSCSI Host Interfaces by among other things, making, using, offering for sale, selling, importing into the United States, marketing, supporting, promoting, providing product instruction, and/or advertising certain of Defendant Storageflex's products and/or components for use with same, including, without limitation, the FF1124 and HA3969 with FC or iSCSI Host Interfaces and/or components for use with same.

44. Defendants Aberdeen, Boost, iXsystems and Storageflex have been on notice of the '041 Patent since before this lawsuit through notification by letter that their products, including, but not limited to, the infringing products listed herein, have infringed and continue to infringe the '041 Patent, and have not ceased their infringing activities. The infringement of the '041 Patent by Defendants Aberdeen, Boost, iXsystems and Storageflex has been and continues to be willful and deliberate.

45. Crossroads has been irreparably harmed by each of Defendant Infortrend's, Boost's, Aberdeen's, iXsystems' and Storageflex's acts of infringement of the '041 Patent, and will continue to be harmed unless and until of Defendant Infortrend's, Boost's, Aberdeen's, iXsystems' and Storageflex's acts of infringement are enjoined and restrained by order of this Court.

46. As a result of the acts of infringement of the '041 Patent by Defendants, Crossroads has suffered and will continue to suffer damages in an amount to be proven at trial.

COUNT 4: INFRINGEMENT OF U.S. PATENT NO. 7,934,040

47. Crossroads incorporates by reference the allegations set forth in the preceding paragraphs.

48. On April 26, 2011, United States Patent No. 7,934,040 (the "'040 Patent") was duly and legally issued. A true and correct copy of the '040 Patent is attached hereto as Exhibit D. Crossroads is the assignee and the owner of all right, title, and interest in and to the '040 Patent. The '040 Patent is entitled to a presumption of validity.

49. Defendants Infortrend, Aberdeen, Boost, iXsystems and Storageflex have each directly infringed the '040 Patent. On information and belief, each Defendant continues to directly infringe the '040 Patent.

50. Specifically, each of the Defendants has directly infringed the '040 Patent by making, using, offering for sale, selling and/or importing into the United States certain of their products including at least the following: EonStor RAID Systems with Fibre Host Interface and/or iSCSI Host Interface, EonStor DS RAID Systems with Fibre Host Interface and/or iSCSI Host Interface, ESVA iSCSI Host Series and ESVA Fibre Host Series (Infortrend); XDAS D-Series RAID Systems with FC and/or iSCSI Host, XDAS iSCSI Series RAID Systems, XDAS

F8 Series RAID Systems and Aberdeen P8 XDAS with Fibre Host Interface (Aberdeen); EonStor RAID Systems with Fibre Host Interface and/or iSCSI Host Interface, EonStor DS RAID Systems with Fibre Host Interface and/or iSCSI Host Interface, ESVA iSCSI Host Series and ESVA Fibre Host Series (Boost); Titan 316F, Titan 424F, ESVA iSCSI Host Series and ESVA Fibre Host Series (iXsystems); and FF1124 and HA3969 FC or iSCSI Host Interfaces (Storageflex).

51. Further, Defendant Aberdeen has been and now is indirectly infringing the '040 Patent, with knowledge of the patent and knowledge that its induced acts constitute patent infringement, by way of actively inducing infringement and/or contributing to the infringement of the '040 Patent by users of Defendant Aberdeen's products, such as XDAS D-Series RAID Systems with FC and/or iSCSI Host, XDAS iSCSI Series RAID Systems, XDAS F8 Series RAID Systems and Aberdeen P8 XDAS with Fibre Host Interface by among other things, making, using, offering for sale, selling, importing into the United States, marketing, supporting, providing product instruction, and/or advertising certain of Defendant Aberdeen's products, including XDAS D-Series RAID Systems with FC and/or iSCSI Host, XDAS iSCSI Series RAID Systems, XDAS F8 Series RAID Systems and Aberdeen P8 XDAS with Fibre Host Interface.

52. Further, Defendant Boost has been and now is indirectly infringing the '040 Patent, with knowledge of the patent and knowledge that its induced acts constitute patent infringement, by way of actively inducing infringement and/or contributing to the infringement of the '040 Patent by users of Defendant Boost's products, such as EonStor RAID Systems with Fibre Host Interface and/or iSCSI Host Interface, EonStor DS RAID Systems with Fibre Host Interface and/or iSCSI Host Interface, ESVA iSCSI Host Series, and ESVA Fibre Host Series by

among other things, making, using, offering for sale, selling, importing into the United States, marketing, supporting, providing product instruction, and/or advertising certain of Defendant Boost's products, including the EonStor RAID Systems with Fibre Host Interface and/or iSCSI Host Interface, EonStor DS RAID Systems with Fibre Host Interface and/or iSCSI Host Interface, ESVA iSCSI Host Series, and ESVA Fibre Host Series.

53. Further, Defendant iXsystems has been and now is indirectly infringing the '040 Patent, with knowledge of the patent, by way of contributing to the infringement of the '040 Patent by users of Defendant iXsystems' products, such as the Titan 316F, Titan 424F, ESVA iSCSI Host Series and ESVA Fibre Host Series by among other things, offering for sale, selling, and/or importing into the United States certain of Defendant iXsystems' products, including the Titan 316F, Titan 424F, ESVA iSCSI Host Series and ESVA Fibre Host Series.

54. Further, Defendant Storageflex has been and now is indirectly infringing the '040 Patent, with knowledge of the patent and knowledge that its induced acts constitute patent infringement, by way of actively inducing infringement and/or contributing to the infringement of the '040 Patent by users of Defendant Storageflex's products, such as the FF1124 and HA3969 with FC or iSCSI Host Interfaces by among other things, making, using, offering for sale, selling, importing into the United States, marketing, supporting, promoting, providing product instruction, and/or advertising certain of Defendant Storageflex's products and/or components for use with same, including, without limitation, the FF1124 and HA3969 with FC or iSCSI Host Interfaces and/or components for use with same.

55. Defendants Aberdeen, Boost, iXsystems and Storageflex have been on notice of the '040 Patent since before this lawsuit through notification by letter that their products, including, but not limited to, the infringing products listed herein, have infringed and continued

to infringe, and have not ceased their infringing activities. The infringement of the '040 Patent by Defendants Aberdeen, Boost, iXsystems and Storageflex has been and continues to be willful and deliberate.

56. Crossroads has been irreparably harmed by each of Defendant Storageflex's, Aberdeen's, iXsystems', Boost's and Infortrend's acts of infringement of the '040 Patent, and will continue to be harmed unless and until each of Defendant Storageflex's, Aberdeen's, iXsystems', Boost's and Infortrend's acts of infringement are enjoined and restrained by order of this Court.

57. As a result of the acts of infringement of the '040 Patent by Defendants, Crossroads has suffered and will continue to suffer damages in an amount to be proven at trial.

COUNT 5: INFRINGEMENT OF U.S. PATENT NO. 7,987,311

58. Crossroads incorporates by reference the allegations set forth in the preceding paragraphs.

59. On July 26, 2011, United States Patent No. 7,987,311 (the "'311 Patent") was duly and legally issued. A true and correct copy of the '311 Patent is attached hereto as Exhibit E. Crossroads is the assignee and the owner of all right, title, and interest in and to the '311 Patent. The '311 Patent is entitled to a presumption of validity.

60. Defendants Infortrend, Aberdeen, Boost, iXsystems and Storageflex have each directly infringed the '311 Patent. On information and belief, each Defendant continues to directly infringe the '311 Patent.

61. Specifically, each of the Defendants has directly infringed the '311 Patent by making, using, offering for sale, selling and/or importing into the United States certain of their products including at least the following: EonStor RAID Systems with Fibre Host Interface

and/or iSCSI Host Interface, EonStor DS RAID Systems with Fibre Host Interface and/or iSCSI Host Interface, ESVA iSCSI Host Series and ESVA Fibre Host Series (Infortrend); XDAS D-Series RAID Systems with FC and/or iSCSI Host, XDAS iSCSI Series RAID Systems, XDAS F8 Series RAID Systems and Aberdeen P8 XDAS with Fibre Host Interface (Aberdeen); EonStor RAID Systems with Fibre Host Interface and/or iSCSI Host Interface, EonStor DS RAID Systems with Fibre Host Interface and/or iSCSI Host Interface, ESVA iSCSI Host Series and ESVA Fibre Host Series (Boost); Titan 316F, Titan 424F, ESVA iSCSI Host Series and ESVA Fibre Host Series (iXsystems); and FF1124 and HA3969 FC or iSCSI Host Interfaces (Storageflex).

62. Further, Defendant Boost has been and now is indirectly infringing the '311 Patent, with knowledge of the patent and knowledge that its induced acts constitute patent infringement, by way of actively inducing infringement and/or contributing to the infringement of the '311 Patent by users of Defendant Boost's products, such as EonStor RAID Systems with Fibre Host Interface and/or iSCSI Host Interface, EonStor DS RAID Systems with Fibre Host Interface and/or iSCSI Host Interface, ESVA iSCSI Host Series, and ESVA Fibre Host Series by among other things, making, using, offering for sale, selling, importing into the United States, marketing, supporting, providing product instruction, and/or advertising certain of Defendant Boost's products, including the EonStor RAID Systems with Fibre Host Interface and/or iSCSI Host Interface, EonStor DS RAID Systems with Fibre Host Interface and/or iSCSI Host Interface, ESVA iSCSI Host Series, and ESVA Fibre Host Series.

63. Further, Defendant Storageflex has been and now is indirectly infringing the '311 Patent, with knowledge of the patent and knowledge that its induced acts constitute patent infringement, by way of actively inducing infringement and/or contributing to the infringement

of the '311 Patent by users of Defendant Storageflex's products, such as the FF1124 and HA3969 with FC or iSCSI Host Interfaces by among other things, making, using, offering for sale, selling, importing into the United States, marketing, supporting, promoting, providing product instruction, and/or advertising certain of Defendant Storageflex's products and/or components for use with same, including, without limitation, the FF1124 and HA3969 with FC or iSCSI Host Interfaces and/or components for use with same.

64. Defendants Boost and Storageflex have been on notice of the '311 Patent since before this lawsuit through notification by letter that their products, including, but not limited to, the infringing products listed herein, have infringed and continued to infringe, and have not ceased their infringing activities. The infringement of the '311 Patent by Defendants Boost and Storageflex has been and continues to be willful and deliberate.

65. Crossroads has been irreparably harmed by each of Defendant Storageflex's, Aberdeen's, iXsystems', Boost's and Infortrend's acts of infringement of the '311 Patent, and will continue to be harmed unless and until each of Defendant Storageflex's, Aberdeen's, iXsystems', Boost's and Infortrend's acts of infringement are enjoined and restrained by order of this Court.

66. As a result of the acts of infringement of the '311 Patent by Defendants, Crossroads has suffered and will continue to suffer damages in an amount to be proven at trial.

PRAYER FOR RELIEF

WHEREFORE, Crossroads requests this Court enter judgment as follows:

A. That each of the Defendants has infringed the '035 Patent;

B. That such infringement of the '035 Patent by Defendants has been willful;

IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
AUSTIN DIVISION

CROSSROADS SYSTEMS, INC.,	§	
	§	
Plaintiff,	§	
	§	CIVIL ACTION NO. 1:12-CV-104
v.	§	
	§	JURY DEMANDED
(1) INFORTREND CORPORATION,	§	
(2) ABERDEEN LLC,	§	
(3) BOOST SYSTEMS, INC.,	§	
(4) IXSYSTEMS, INC., and	§	
(5) STORAGEFLEX, INC.,	§	
	§	
Defendants.	§	

PLAINTIFF CROSSROADS SYSTEMS, INC.'S COMPLAINT FOR PATENT INFRINGEMENT

THE PARTIES

1. Plaintiff Crossroads Systems, Inc. ("Crossroads") is a corporation incorporated under the laws of the State of Delaware and has its principal place of business at 11000 North MoPac Expressway, Austin, Texas 78759.

2. Upon information and belief, Defendant Infortrend Corporation ("Infortrend") is a California corporation with a principal place of business of 2200 Zanker Road, Suite 130, San Jose, CA 95131.

3. Upon information and belief, Defendant Aberdeen LLC ("Aberdeen") is a California company with a principal place of business of 10420 Pioneer Boulevard, Santa Fe Springs, CA 90670.

4. Upon information and belief, Defendant Boost Systems, Inc. ("Boost") is a California corporation with a principal place of business of 11391 Sunrise Gold Circle, Suite 300, Rancho Cordova, CA 95742.

C. That Defendants account for and pay to Crossroads all damages caused by the infringement of the '035 Patent;

D. That Crossroads receive enhanced damages from Defendants in the form of treble damages, pursuant to 35 U.S.C. § 284 based on Defendants' willful infringement of the '035 Patent;

E. That Crossroads be granted pre-judgment and post-judgment interest on the damages caused to it by reason of Defendants' infringement of the '035 Patent, including pre-judgment and post-judgment interest on any enhanced damages or attorneys' fees award;

F. That Defendants Infortrend, Boost and Storageflex have infringed the '147 Patent;

G. That such infringement of the '147 Patent by Defendants Infortrend, Boost and Storageflex has been willful;

H. That Defendants Infortrend, Boost and Storageflex account for and pay to Crossroads all damages caused by the infringement of the '147 Patent;

I. That Crossroads receive enhanced damages from Defendants Infortrend, Boost and Storageflex in the form of treble damages, pursuant to 35 U.S.C. § 284 based on Defendants Infortrend, Boost and Storageflex's willful infringement of the '147 Patent;

J. That Crossroads be granted pre-judgment and post-judgment interest on the damages caused to it by reason of Defendants Infortrend, Boost and Storageflex's infringement of the '147 Patent, including pre-judgment and post-judgment interest on any enhanced damages or attorneys' fees award;

K. That each of the Defendants has infringed the '041 Patent;

L. That such infringement of the '041 Patent by Defendants Aberdeen, Boost, iXsystems and Storageflex has been willful;

M. That Defendants account for and pay to Crossroads all damages caused by the infringement of the '041 Patent;

N. That Crossroads receive enhanced damages from Defendants in the form of treble damages, pursuant to 35 U.S.C. § 284 based on each of Defendants Aberdeen's, Boost's, iXsystems' and Storageflex's willful infringement of the '041 Patent;

O. That Crossroads be granted pre-judgment and post-judgment interest on the damages caused to it by reason of Defendants' infringement of the '041 Patent, including pre-judgment and post-judgment interest on any enhanced damages or attorneys' fees award;

P. That each of the Defendants has infringed the '040 Patent;

Q. That such infringement of the '040 Patent by Defendants Aberdeen, Boost, iXsystems and Storageflex has been willful;

R. That Defendants account for and pay to Crossroads all damages caused by the infringement of the '040 Patent;

S. That Crossroads receive enhanced damages from Defendants in the form of treble damages, pursuant to 35 U.S.C. § 284 based on each of Defendants Aberdeen's, Boost's, iXsystems' and Storageflex's willful infringement of the '040 Patent;

T. That Crossroads be granted pre-judgment and post-judgment interest on the damages caused to it by reason of Defendants' infringement of the '040 Patent, including pre-judgment and post-judgment interest on any enhanced damages or attorneys' fees award;

U. That each of the Defendants has infringed the '311 Patent;

V. That such infringement of the '311 Patent by Defendants Boost and Storageflex has been willful;

W. That Defendants account for and pay to Crossroads all damages caused by the infringement of the '311 Patent;

X. That Crossroads receive enhanced damages from Defendants Boost and Storageflex in the form of treble damages, pursuant to 35 U.S.C. § 284 based on each of Defendants Boost's and Storageflex's willful infringement of the '311 Patent;

Y. That Crossroads be granted pre-judgment and post-judgment interest on the damages caused to it by reason of Defendants' infringement of the '311 Patent, including pre-judgment and post-judgment interest on any enhanced damages or attorneys' fees award;

Z. That Defendants pay Crossroads all of Crossroads' reasonable attorneys' fees and expenses;

AA. That costs be awarded to Crossroads;

BB. That Defendants, their agents, employees, representatives, successors and assigns, and those acting in privity or in concert with them, be preliminary and permanently enjoined from further infringement of the '035 Patent;

CC. That Defendants Infortrend, Boost and Storageflex, their agents, employees, representatives, successors and assigns, and those acting in privity or in concert with them, be preliminary and permanently enjoined from further infringement of the '147 Patent;

DD. That Defendants, their agents, employees, representatives, successors and assigns, and those acting in privity or in concert with them, be preliminary and permanently enjoined from further infringement of the '041 Patent;

EE. That Defendants, their agents, employees, representatives, successors and assigns, and those acting in privity or in concert with them, be preliminary and permanently enjoined from further infringement of the '040 Patent;

FF. That Defendants, their agents, employees, representatives, successors and assigns, and those acting in privity or in concert with them, be preliminary and permanently enjoined from further infringement of the '311 Patent;

GG. That this is an exceptional case under 35 U.S.C. § 285; and

HH. That Crossroads be granted such other and further relief as the Court may deem just and proper under the circumstances.

DEMAND FOR JURY TRIAL

Crossroads hereby demands a trial by jury on all issues.

Dated: February 1, 2012

Respectfully submitted,

By: */s/ Elizabeth J. Brown Fore*

Steven Sprinkle
State Bar No. 00794962
Elizabeth J. Brown Fore
State Bar No. 24001795
Sprinkle IP Law Group, PC

1301 W. 25th Street, Suite 408
Austin, Texas 78705
Tel: (512) 637-9220
Fax: (512) 371-9088
ssprinkle@sprinklelaw.com
ebrownfore@sprinklelaw.com

5. Upon information and belief, Defendant iXsystems, Inc. ("iXsystems") is a Delaware corporation with a principal place of business of 2490 Kruse Drive, San Jose, CA 95131.

6. Upon information and belief, Defendant Storageflex, Inc. ("Storageflex") is an Ontario corporation with a principal place of business of 3601 Highway 7, Suite 400, Markham, Ontario L3R 0M3 Canada.

JURISDICTION AND VENUE

7. This action arises under the laws of the United States, more specifically under 35 U.S.C. § 100, *et seq.* Subject matter jurisdiction is proper in this Court pursuant to 28 U.S.C. §§ 1331 and 1338.

8. Personal jurisdiction and venue are proper in this district under 28 U.S.C. §§ 1391(c) and 1400. Upon information and belief, each Defendant has established minimum contacts with this forum such that the exercise of jurisdiction over each defendant would not offend traditional notions of fair play and substantial justice.

9. This Court has personal jurisdiction over Infortrend. Upon information and belief, Infortrend regularly conducts business in the State of Texas and in this judicial district and is subject to the jurisdiction of this Court. Upon information and belief, Infortrend has been doing business in Texas and this judicial district by distributing, marketing, selling and/or offering for sale its products, including, but not limited to, products that practice the subject matter claimed in the Patents-In-Suit, and/or regularly doing or soliciting business and/or engaging in other persistent courses of conduct in and/or directed to Texas and this judicial district.

10. This Court has personal jurisdiction over Aberdeen. Upon information and belief, Aberdeen regularly conducts business in the State of Texas and in this judicial district and is

subject to the jurisdiction of this Court. Upon information and belief, Aberdeen has been doing business in Texas and this judicial district by distributing, marketing, selling and/or offering for sale its products, and/or regularly doing or soliciting business and/or engaging in other persistent courses of conduct in and/or directed to Texas and this judicial district.

11. This Court has personal jurisdiction over Boost. Upon information and belief, Boost regularly conducts business in the State of Texas and in this judicial district and is subject to the jurisdiction of this Court. Upon information and belief, Boost has been doing business in Texas and this judicial district by distributing, marketing, selling and/or offering for sale its products, and/or regularly doing or soliciting business and/or engaging in other persistent courses of conduct in and/or directed to Texas and this judicial district.

12. This Court has personal jurisdiction over iXsystems. Upon information and belief, iXsystems regularly conducts business in the State of Texas and in this judicial district and is subject to the jurisdiction of this Court. Upon information and belief, iXsystems has been doing business in Texas and this judicial district by distributing, marketing, selling and/or offering for sale its products, and/or regularly doing or soliciting business and/or engaging in other persistent courses of conduct in and/or directed to Texas and this judicial district.

13. This Court has personal jurisdiction over Storageflex. Upon information and belief, Storageflex regularly conducts business in the State of Texas and in this judicial district and is subject to the jurisdiction of this Court. Upon information and belief, Storageflex has been doing business in Texas and this judicial district by distributing, marketing, selling and/or offering for sale its products, and/or regularly doing or soliciting business and/or engaging in other persistent courses of conduct in and/or directed to Texas and this judicial district. Further, Storageflex has engaged in activities in this judicial district relating to one or more products that

practice the subject matter claimed by at least one of the Patents-In-Suit by purchasing one or more products from this judicial district that were marked with at least one of the patents-in-suit.

COUNT 1: INFRINGEMENT OF U.S. PATENT NO. 6,425,035

14. Crossroads incorporates by reference the allegations set forth in the preceding paragraphs.

15. On July 23, 2002, United States Patent No. 6,425,035 (the "'035 Patent") was duly and legally issued. A true and correct copy of the '035 Patent is attached hereto as Exhibit A. Crossroads is the assignee and the owner of all right, title, and interest in and to the '035 Patent. The '035 Patent is entitled to a presumption of validity.

16. Defendants Infortrend, Aberdeen, Boost, iXsystems and Storageflex have each directly infringed the '035 Patent. On information and belief, each Defendant continues to directly infringe the '035 Patent.

17. Specifically, each of the Defendants has directly infringed the '035 Patent by making, using, offering for sale, selling and/or importing into the United States certain of their products including at least the following: EonStor RAID Systems with Fibre Host Interface and/or iSCSI Host Interface, EonStor DS RAID Systems with Fibre Host Interface and/or iSCSI Host Interface, ESVA iSCSI Host Series and ESVA Fibre Host Series (Infortrend); XDAS D-Series RAID Systems with FC and/or iSCSI Host, XDAS iSCSI Series RAID Systems, XDAS F8 Series RAID Systems and Aberdeen P8 XDAS with Fibre Host Interface (Aberdeen); EonStor RAID Systems with Fibre Host Interface and/or iSCSI Host Interface, EonStor DS RAID Systems with Fibre Host Interface and/or iSCSI Host Interface, ESVA iSCSI Host Series and ESVA Fibre Host Series (Boost); Titan 316F, Titan 424F, ESVA iSCSI Host Series, and

ESVA Fibre Host Series (iXsystems); and FF1124 and HA3969 with FC or iSCSI Host Interfaces (Storageflex).

18. Further, Defendant Infortrend has been and now is indirectly infringing the '035 Patent, with knowledge of the patent and knowledge that its induced acts constitute patent infringement, by way of actively inducing infringement and/or contributing to the infringement of the '035 Patent by users of Defendant Infortrend's products, such as EonStor RAID Systems with Fibre Host Interface and/or iSCSI Host Interface, EonStor DS RAID Systems with Fibre Host Interface and/or iSCSI Host Interface, ESVA iSCSI Host Series and ESVA Fibre Host Series, by among other things, making, using, offering for sale, selling, importing into the United States, marketing, supporting, promoting, providing product instruction, and/or advertising certain of Defendant Infortrend's products and/or Defendant Infortrend's components for use with same, including EonStor RAID Systems with Fibre Host Interface and/or iSCSI Host Interface, EonStor DS RAID Systems with Fibre Host Interface and/or iSCSI Host Interface, ESVA iSCSI Host Series and ESVA Fibre Host Series and/or components for use with same.

19. Further, Defendant Aberdeen has been and now is indirectly infringing the '035 Patent, with knowledge of the patent and knowledge that its induced acts constitute patent infringement, by way of actively inducing infringement and/or contributing to the infringement of the '035 Patent by users of Defendant Aberdeen's products, such as XDAS D-Series RAID Systems with FC and/or iSCSI Host, XDAS iSCSI Series RAID Systems, XDAS F8 Series RAID Systems and Aberdeen P8 XDAS with Fibre Host Interface by among other things, making, using, offering for sale, selling, importing into the United States, marketing, supporting, providing product instruction, and/or advertising certain of Defendant Aberdeen's products, including XDAS D-Series RAID Systems with FC and/or iSCSI Host, XDAS iSCSI Series

RAID Systems, XDAS F8 Series RAID Systems and Aberdeen P8 XDAS with Fibre Host Interface.

20. Further, Defendant Boost has been and now is indirectly infringing the '035 Patent, with knowledge of the patent and knowledge that its induced acts constitute patent infringement, by way of actively inducing infringement and/or contributing to the infringement of the '035 Patent by users of Defendant Boost's products, such as EonStor RAID Systems with Fibre Host Interface and/or iSCSI Host Interface, EonStor DS RAID Systems with Fibre Host Interface and/or iSCSI Host Interface, ESVA iSCSI Host Series, and ESVA Fibre Host Series by among other things, making, using, offering for sale, selling, importing into the United States, marketing, supporting, providing product instruction, and/or advertising certain of Defendant Boost's products, including the EonStor RAID Systems with Fibre Host Interface and/or iSCSI Host Interface, EonStor DS RAID Systems with Fibre Host Interface and/or iSCSI Host Interface, ESVA iSCSI Host Series, and ESVA Fibre Host Series.

21. Further, Defendant iXsystems has been and now is indirectly infringing the '035 Patent, with knowledge of the patent, by way of contributing to the infringement of the '035 Patent by users of Defendant iXsystems' products, such as the Titan 316F, Titan 424F, ESVA iSCSI Host Series and ESVA Fibre Host Series, by among other things, offering for sale, selling, and/or importing into the United States certain of Defendant iXsystems' products, including Titan 316F, Titan 424F, ESVA iSCSI Host Series, and/or ESVA Fibre Host Series.

22. Further, Defendant Storageflex has been and now is indirectly infringing the '035 Patent, with knowledge of the patent and knowledge that its induced acts constitute patent infringement, by way of actively inducing infringement and/or contributing to the infringement of the '035 Patent by users of Defendant Storageflex's products, such as the FF1124 and

HA3969 with FC or iSCSI Host Interfaces, by among other things, making, using, offering for sale, selling, importing into the United States, marketing, supporting, promoting, providing product instruction, and/or advertising certain of Defendant Storageflex's products and/or components for use with same, including the FF1124 and HA3969 with FC or iSCSI Host Interfaces and/or components for use with same.

23. Each Defendant has been on notice of the '035 Patent since before this lawsuit through prior involvement in litigation involving the '035 Patent (Infortrend), the purchase of a marked product (Storageflex) and/or through notification by letter that its products, including but not limited to the infringing products listed herein, have infringed and continue to infringe (Storageflex, Aberdeen, iXsystems, Boost), and no Defendant has ceased its infringing activities. The infringement of the '035 Patent by each Defendant has been and continues to be willful and deliberate.

24. Crossroads has been irreparably harmed by each of Defendant Infortrend's, Storageflex's, Aberdeen's, Boost's and iXsystems' acts of infringement of the '035 Patent, and will continue to be harmed unless and until each of Defendant Infortrend's, Storageflex's, Aberdeen's, Boost's and iXsystems' acts of infringement are enjoined and restrained by order of this Court.

25. As a result of the acts of infringement of the '035 Patent by Defendants, Crossroads has suffered and will continue to suffer damages in an amount to be proven at trial.

COUNT 2: INFRINGEMENT OF U.S. PATENT NO. 7,051,147

26. Crossroads incorporates by reference the allegations set forth in the preceding paragraphs.

27. On May 23, 2006, United States Patent No. 7,051,147 (the "'147 Patent") was duly and legally issued. A true and correct copy of the '147 Patent is attached hereto as Exhibit B. Crossroads is the assignee and the owner of all right, title, and interest in and to the '147 Patent. The '147 Patent is entitled to a presumption of validity.

28. Defendants Infortrend, Boost and Storageflex have directly infringed the '147 Patent and, on information and belief, Defendants Infortrend, Boost and Storageflex continue to directly infringe the '147 Patent.

29. Specifically, Defendants Infortrend, Boost and Storageflex have directly infringed the '147 Patent by making, using, offering for sale, selling and/or importing into the United States certain of their products including at least the following: EonStor Fibre-to-Fibre RAID Systems and EonStor DS Fibre-to-Fibre RAID Systems (Infortrend); EonStor Fibre-to-Fibre RAID Systems (Boost); and FF1124 (Storageflex).

30. Further, Defendant Infortrend has been and now is indirectly infringing the '147 Patent, with knowledge of the patent and knowledge that its induced acts constitute patent infringement, by way of actively inducing infringement and/or contributing to the infringement of the '147 Patent by users of Defendant Infortrend's products, such as EonStor Fibre-to-Fibre RAID Systems and EonStor DS Fibre-to-Fibre RAID Systems by, among other things, making, using, offering for sale, selling, importing into the United States, marketing, supporting, promoting, providing product instruction, and/or advertising certain of its products and/or Defendant Infortrend's components for use with same, including EonStor Fibre-to-Fibre RAID Systems, EonStor DS Fibre-to-Fibre RAID Systems and/or components for use with same.

31. Further, Defendant Boost has been and now is indirectly infringing the '147 Patent, with knowledge of the patent and knowledge that its induced acts constitute patent

AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Western District of Texas, Austin Division on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
1:12-CV-1090-SS	11/27/2012	Western District of Texas, Austin Division

PLAINTIFF	DEFENDANT
Crossroads Systems, Inc.	Addonics Technologies, Inc.

PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 see attached		
2 6,425,035		
3 7,934,041		
4		
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
William G. Putnicki	Jennifer Williams	11/28/2012

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
AUSTIN DIVISION

CROSSROADS SYSTEMS, INC.,	§	
	§	
Plaintiff,	§	
	§	CIVIL ACTION NO. 1:12-CV-1090
v.	§	
	§	JURY DEMANDED
ADDONICS TECHNOLOGIES, INC.,	§	
	§	
Defendant.	§	

PLAINTIFF CROSSROADS SYSTEMS, INC.'S COMPLAINT FOR PATENT INFRINGEMENT

THE PARTIES

1. Plaintiff Crossroads Systems, Inc. ("Crossroads") is a corporation incorporated under the laws of the State of Delaware and has its principal place of business at 11000 North MoPac Expressway, Austin, Texas 78759.

2. Upon information and belief, Defendant Addonics Technologies, Inc. ("Addonics") is a California corporation with a principal place of business of 1918 Junction Avenue, San Jose, CA 95131.

JURISDICTION AND VENUE

3. This action arises under the laws of the United States, more specifically under 35 U.S.C. § 100, *et seq.* Subject matter jurisdiction is proper in this Court pursuant to 28 U.S.C. §§ 1331 and 1338.

4. Personal jurisdiction and venue are proper in this district under 28 U.S.C. §§ 1391 and 1400. Upon information and belief, Defendant has established minimum contacts with this forum such that the exercise of jurisdiction over Defendant would not offend traditional notions of fair play and substantial justice.

5. Addonics is subject to this Court's specific and general personal jurisdiction pursuant to due process and/or the Texas Long Arm Statute, because, upon information and belief, Addonics has been doing business in Texas and this judicial district by distributing, marketing, selling and/or offering for sale its products, including, but not limited to, products that practice the subject matter claimed in the Patents-In-Suit, and/or regularly doing or soliciting business and/or engaging in other persistent courses of conduct in and/or directed to Texas and this judicial district including, at least by advertising and making available their infringing systems and/or methods through the Internet in such a way as to reach customers in this judicial district.

COUNT 1: INFRINGEMENT OF U.S. PATENT NO. 6,425,035

6. Crossroads incorporates by reference the allegations set forth in the preceding paragraphs.

7. On July 23, 2002, United States Patent No. 6,425,035 (the "'035 Patent") was duly and legally issued. A true and correct copy of the '035 Patent is attached hereto as Exhibit A. Crossroads is the assignee and the owner of all right, title, and interest in and to the '035 Patent. The '035 Patent is entitled to a presumption of validity.

8. Defendant Addonics has directly infringed the '035 Patent. On information and belief, Defendant continues to directly infringe the '035 Patent.

9. Specifically, Defendant has directly infringed the '035 Patent by making, using, offering for sale, selling and/or importing into the United States certain of its products including at least the following: Addonics ISC8P2G-S and ISC16P2G-S iSCSI Subsystems, Addonics iSCSI Rack, Addonics Storage Rack with ISC8P2G, Addonics SAN Tower (also referred to as

Addonics SAN Storage Tower), and Addonics SAN Tower II (also referred to as Addonics SAN Storage Tower II).

10. Further, Defendant has been and now is indirectly infringing by way of inducing infringement of the '035 Patent with knowledge of the '035 Patent by making, offering for sale, selling, importing into the United States, marketing, supporting, providing product instruction and/or advertising certain of its products, including the Addonics ISC8P2G-S and ISC16P2G-S iSCSI Subsystems, Addonics iSCSI Rack, Addonics Storage Rack with ISC8P2G, Addonics SAN Tower (also referred to as Addonics SAN Storage Tower), and Addonics SAN Tower II (also referred to as Addonics SAN Storage Tower II), and Defendant knew that its actions were inducing end users to infringe the '035 Patent.

11. Further, Defendant has been and now is indirectly infringing by way of contributing to the infringement by end users of the '035 Patent by selling, offering to sell and/or importing into the United States components, including the Addonics ISC8P2G-S and ISC16P2G-S iSCSI Subsystems, Addonics iSCSI Rack, Addonics Storage Rack with ISC8P2G, Addonics SAN Tower (also referred to as Addonics SAN Storage Tower), and Addonics SAN Tower II (also referred to as Addonics SAN Storage Tower II), knowing the components to be especially made or especially adapted for use in the infringement of the '035 Patent. Such components are not a staple article or commodity of commerce suitable for substantial non-infringing uses.

12. Defendant has been on constructive and/or actual notice of the '035 Patent since before this lawsuit and Defendant has not ceased its infringing activities. The infringement of the '035 Patent by Defendant has been and continues to be willful and deliberate.

13. Crossroads has been irreparably harmed by Defendant's acts of infringement of the '035 Patent, and will continue to be harmed unless and until Defendant's acts of infringement are enjoined and restrained by order of this Court.

14. As a result of the acts of infringement of the '035 Patent by Defendant, Crossroads has suffered and will continue to suffer damages in an amount to be proven at trial.

COUNT 2: INFRINGEMENT OF U.S. PATENT NO. 7,934,041

15. Crossroads incorporates by reference the allegations set forth in the preceding paragraphs.

16. On April 26, 2011, United States Patent No. 7,934,041 (the "'041 Patent") was duly and legally issued. A true and correct copy of the '041 Patent is attached hereto as Exhibit B. Crossroads is the assignee and the owner of all right, title, and interest in and to the '041 Patent. The '041 Patent is entitled to a presumption of validity.

17. Defendant Addonics has directly infringed the '041 Patent. On information and belief, Defendant continues to directly infringe the '041 Patent.

18. Specifically, Defendant has directly infringed the '041 Patent by making, using, offering for sale, selling and/or importing into the United States certain of its products including at least the following: Addonics ISC8P2G-S and ISC16P2G-S iSCSI Subsystems, Addonics iSCSI Rack, Addonics Storage Rack with ISC8P2G, Addonics SAN Tower (also referred to as Addonics SAN Storage Tower), and Addonics SAN Tower II (also referred to as Addonics SAN Storage Tower II).

19. Further, Defendant has been and now is indirectly infringing by way of inducing infringement of the '041 Patent with knowledge of the '041 Patent by making, offering for sale, selling, importing into the United States, marketing, supporting, providing product instruction

and/or advertising certain of its products, including the Addonics ISC8P2G-S and ISC16P2G-S iSCSI Subsystems, Addonics iSCSI Rack, Addonics Storage Rack with ISC8P2G, Addonics SAN Tower (also referred to as Addonics SAN Storage Tower), and Addonics SAN Tower II (also referred to as Addonics SAN Storage Tower II), and Defendant knew that its actions were inducing end users to infringe the '041 Patent.

20. Further, Defendant has been and now is indirectly infringing by way of contributing to the infringement by end users of the '041 Patent by selling, offering to sell and/or importing into the United States components, including the Addonics ISC8P2G-S and ISC16P2G-S iSCSI Subsystems, Addonics iSCSI Rack, Addonics Storage Rack with ISC8P2G, Addonics SAN Tower (also referred to as Addonics SAN Storage Tower), and Addonics SAN Tower II (also referred to as Addonics SAN Storage Tower II), knowing the components to be especially made or especially adapted for use in the infringement of the '041 Patent. Such components are not a staple article or commodity of commerce suitable for substantial non-infringing uses.

21. Defendant has been on constructive and/or actual notice of the '041 Patent since before this lawsuit and Defendant has not ceased its infringing activities. The infringement of the '041 Patent by Defendant has been and continues to be willful and deliberate.

22. Crossroads has been irreparably harmed by Defendant Addonics' acts of infringement of the '041 Patent, and will continue to be harmed unless and until Defendant Addonics' acts of infringement are enjoined and restrained by order of this Court.

23. As a result of the acts of infringement of the '041 Patent by Defendant, Crossroads has suffered and will continue to suffer damages in an amount to be proven at trial.

PRAYER FOR RELIEF

WHEREFORE, Crossroads requests this Court enter judgment as follows:

A. That Defendant Addonics has infringed the '035 Patent;

B. That such infringement of the '035 Patent by Defendant has been willful;

C. That Defendant accounts for and pays to Crossroads all damages caused by the infringement of the '035 Patent;

D. That Crossroads receive enhanced damages from Defendant in the form of treble damages, pursuant to 35 U.S.C. § 284 based on Defendant's willful infringement of the '035 Patent;

E. That Crossroads be granted pre-judgment and post-judgment interest on the damages caused to it by reason of Defendant's infringement of the '035 Patent, including pre-judgment and post-judgment interest on any enhanced damages or attorneys' fees award;

F. That Defendant Addonics has infringed the '041 Patent;

G. That such infringement of the '041 Patent by Defendant has been willful;

H. That Defendant accounts for and pays to Crossroads all damages caused by the infringement of the '041 Patent;

I. That Crossroads receive enhanced damages from Defendant in the form of treble damages, pursuant to 35 U.S.C. § 284 based on Defendant Addonics' willful infringement of the '041 Patent;

J. That Crossroads be granted pre-judgment and post-judgment interest on the damages caused to it by reason of Defendant's infringement of the

'041 Patent, including pre-judgment and post-judgment interest on any enhanced damages or attorneys' fees award;

K. That Defendant pay Crossroads all of Crossroads' reasonable attorneys' fees and expenses;

L. That costs be awarded to Crossroads;

M. That Defendant, its agents, employees, representatives, successors and assigns, and those acting in privity or in concert with it, be preliminary and permanently enjoined from further infringement of the '035 Patent;

N. That Defendant, its agents, employees, representatives, successors and assigns, and those acting in privity or in concert with it, be preliminary and permanently enjoined from further infringement of the '041 Patent;

O. That this is an exceptional case under 35 U.S.C. § 285; and

P. That Crossroads be granted such other and further relief as the Court may deem just and proper under the circumstances.

DEMAND FOR JURY TRIAL

Crossroads hereby demands a trial by jury on all issues.

Dated: November 27, 2012

Respectfully submitted,

By: */s/ Elizabeth J. Brown Fore*

Steven Sprinkle
State Bar No. 00794962
Elizabeth J. Brown Fore
State Bar No. 24001795
Sprinkle IP Law Group, PC
1301 W. 25th Street, Suite 408
Austin, Texas 78705
Tel: (512) 637-9220
Fax: (512) 371-9088
ssprinkle@sprinklelaw.com
ebrownfore@sprinklelaw.com

ATTORNEYS FOR PLAINTIFF CROSSROADS SYSTEMS, INC.