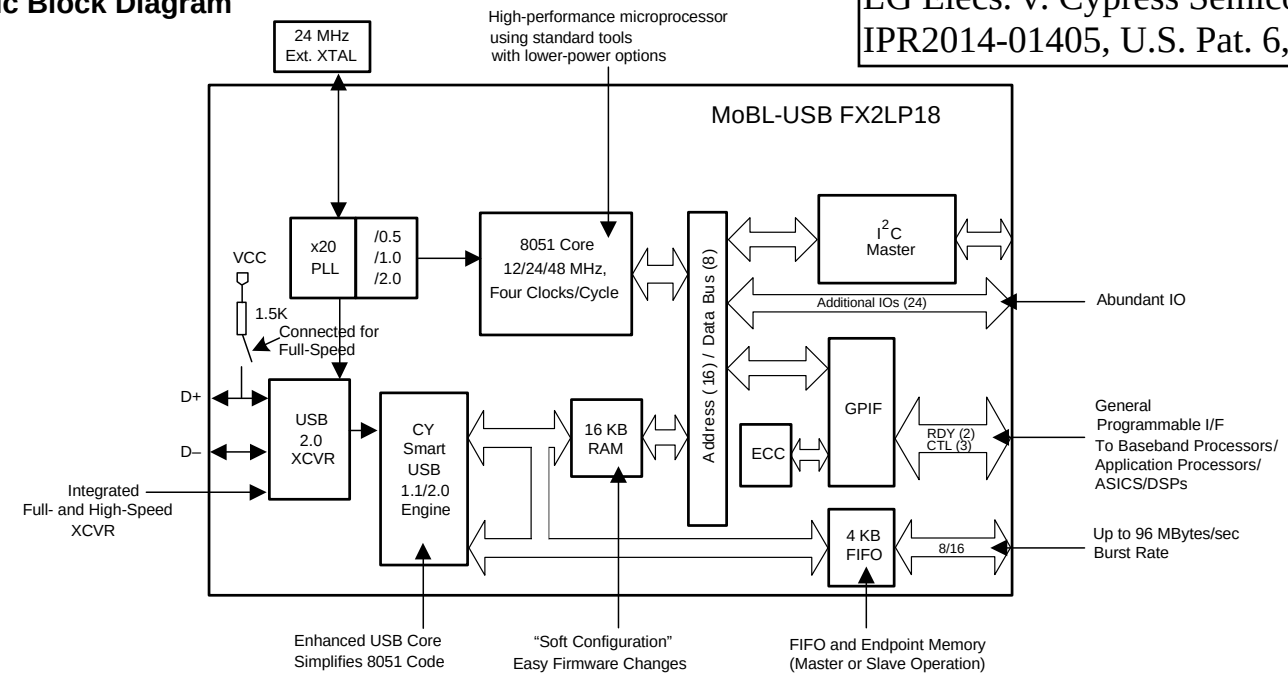
CY7C68053

MoBL-USB™ FX2LP18 USB Microcontroller

1. Features

- USB 2.0 9 V USB-IF high speed and full speed compliant (TID# 40000188)
- Single-chip integrated USB 2.0 transceiver, smart SIE, and enhanced 8051 microprocessor
- Ideal for mobile applications (cell phone, smart phones, PDAs, MP3 players)
  - Ultra low power
  - Suspend current: 20 µA (typical)
- Software: 8051 Code runs from:
  - Internal RAM, which is loaded from EEPROM
- 16 kBytes of on-chip code/data RAM
- Four programmable BULK/INTERRUPT/ISOCHRONOUS endpoints
  - Buffering options: double, triple, and quad
- Additional Programmable (BULK/INTERRUPT) 64-Byte Endpoint
- 8 or 16-Bit External Data Interface
- Smart Media Standard ECC Generation
- GPIF (General Programmable Interface)
  - Allows direct connection to most parallel interface
  - Programmable waveform descriptors and configuration registers to define waveforms
  - Supports multiple Ready and Control outputs
- Integrated, Industry Standard Enhanced 8051
  - 48 MHz, 24 MHz, or 12 MHz CPU operation
  - Four clocks per instruction cycle
  - Three counter/timers
  - Expanded interrupt system
  - Two data pointers
- 1.8 V Core Operation
- 1.8 V to 3.3 V I/O Operation
- Vectored USB Interrupts and GPIF/FIFO Interrupts
- Separate Data Buffers for Setup and Data Portions of a CONTROL Transfer
- Integrated I^2C Controller, runs at 100 or 400 kHz
- Four Integrated FIFOs
  - Integrated glue logic and FIFOs lower system cost
  - Automatic conversion to and from 16-bit buses
  - Master or slave operation
  - Uses external clock or asynchronous strobes
  - Easy interface to ASIC and DSP ICs
- Available in Industrial Temperature Grade
- Available in one Pb-free Package with up to 24 GPIOs
  - 56-pin VFBGA (24 GPIOs)

Logic Block Diagram



Contents

Cypress Semiconductor Corporation's MoBL-USB™ FX2LP18 (CY7C68053) is a low voltage (1.8 V) version of the EZ-USB® FX2LP (CY7C68013A), which is a highly integrated, low power USB 2.0 microcontroller. By integrating the USB 2.0 transceiver, serial interface engine (SIE), enhanced 8051 microcontroller, and a programmable peripheral interface in a single chip, Cypress has created a very cost effective solution that provides superior time-to-market advantages with low power to enable bus powered applications.

The ingenious architecture of MoBL-USB FX2LP18 results in data transfer rates of over 53 Mbytes per second, the maximum allowable USB 2.0 bandwidth, while still using a low cost 8051 microcontroller in a package as small as a 56VFBGA (5 mm x 5 mm). Because it incorporates the USB 2.0 transceiver, the MoBL-USB FX2LP18 is more economical, providing a smaller footprint solution than USB 2.0 SIE or external transceiver implementations. With MoBL-USB FX2LP18, the Cypress Smart SIE handles most of the USB 1.1 and 2.0 protocol in hardware, freeing the embedded microcontroller for application-specific functions and decreasing development time to ensure USB compatibility.

The General Programmable Interface (GPIF) and Master/Slave Endpoint FIFO (8 or 16-bit data bus) provide an easy and glueless interface to popular interfaces such as ATA, UTOPIA, EPP, PCMCIA, and most DSP/processors.

The MoBL-USB FX2LP18 is also referred to as FX2LP18 in this document.

2. Applications

There are a wide variety of applications for the MoBL-USB FX2LP18. It is used in cell phones, smart phones, PDAs, and MP3 players, to name a few.

The 'Reference Designs' section of the Cypress web site provides additional tools for typical USB 2.0 applications. Each reference design comes complete with firmware source and object code, schematics, and documentation. For more information, visit http://www.cypress.com.

3. Functional Overview

The functionality of this chip is described in the sections below.

3.1 USB Signaling Speed

FX2LP18 operates at two of the three rates defined in the USB Specification Revision 2.0, dated April 27, 2000.

- Full speed, with a signaling bit rate of 12 Mbps
- High speed, with a signaling bit rate of 480 Mbps

FX2LP18 does not support the low speed signaling mode of 1.5 Mbps.

3.2 8051 Microprocessor

The 8051 microprocessor embedded in the FX2LP18 family has 256 bytes of register RAM, an expanded interrupt system, and three timer/counters.

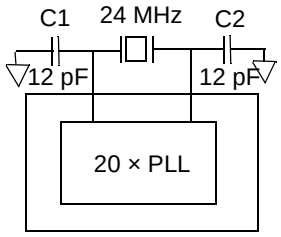
3.2.1 8051 Clock Frequency

FX2LP18 has an on-chip oscillator circuit that uses an external 24 MHz (±100-ppm) crystal with the following characteristics:

- Parallel resonant
- Fundamental mode
- 500 µW drive level
- 12 pF (5% tolerance) load capacitors

An on-chip PLL multiplies the 24 MHz oscillator up to 480 MHz, as required by the transceiver/PHY; internal counters divide it down for use as the 8051 clock. The default 8051 clock frequency is 12 MHz. The clock frequency of the 8051 can be changed by the 8051 through the CPUCS register, dynamically.

Figure 1. Crystal Configuration



12 pF capacitor values assumes a trace capacitance of 3 pF per side on a four-layer FR4 PCA

The CLKOUT pin, which can be tristated and inverted using internal control bits, outputs the 50% duty cycle 8051 clock, at the selected 8051 clock frequency — 48, 24, or 12 MHz.

3.2.2 Special Function Registers

Certain 8051 Special Function Register (SFR) addresses are populated to provide fast access to critical FX2LP18 functions. These SFR additions are shown in Table 1 on page 4. Bold type indicates non standard, enhanced 8051 registers. The two SFR rows that end with '0' and '8' contain bit-addressable registers. The four I/O ports A–D use the SFR addresses used in the standard 8051 for ports 0–3, which are not implemented in FX2LP18. Because of the faster and more efficient SFR addressing, the FX2LP18 I/O ports are not addressable in external RAM space (using the MOVX instruction).

Table 1. Special Function Registers

x	8x	9x	Ax	Bx	Cx	Dx	Ex	Fx
0	**IOA**	**IOB**	**IOC**	**IOD**	SCON1	PSW	ACC	B
1	SP	**EXIF**	**INT2CLR**	**IOE**	SBUF1			
2	DPL0	**MPAGE**		**OEA**				
3	DPH0			**OEB**				
4	**DPL1**			**OEC**				
5	**DPH1**			**OED**				
6	**DPS**			**OEE**				
7	PCON							
8	TCON	SCON0	IE	IP	T2CON	**EICON**	**EIE**	**EIP**
9	TMOD	SBUF0						
A	TL0	**AUTOPTRH1**	**EP2468STAT**	**EP01STAT**	RCAP2L			
B	TL1	**AUTOPTRL1**	**EP24FIFOFLGS**	**GPIFTRIG**	RCAP2H			
C	TH0	**Reserved**	**EP68FIFOFLGS**		TL2			
D	TH1	**AUTOPTRH2**		**GPIFSGLDATH**	TH2			
E	**CKCON**	**AUTOPTRL2**		**GPIFSGLDATLX**				
F		**Reserved**	**AUTOPTRSET-UP**	**GPIFSGLDATLNOX**				

3.3 I²C™ Bus

FX2LP18 supports the I²C bus as a master only at 100 or 400 KHz. SCL and SDA pins have open-drain outputs and hysteresis inputs. These signals must be pulled up to either V_{CC} or V_{CC_IO}, even if no I²C device is connected. (Connecting to V_{CC_IO} may be more convenient.)

3.4 Buses

This 56-pin package has an 8- or 16-bit ‘FIFO’ bidirectional data bus, multiplexed on I/O ports B and D.

3.5 USB Boot Methods

During the power up sequence, internal logic checks the I²C port for the connection of an EEPROM whose first byte is 0xC2. If found, it boot-loads the EEPROM contents into internal RAM (0xC2 load). If no EEPROM is present, an external processor must emulate an I²C slave. The FX2LP18 does not enumerate using internally stored descriptors (for example, Cypress’s VID/PID/DID is not used for enumeration).[1]

3.6 ReNumeration™

Because the FX2LP18’s configuration is soft, one chip can take on the identities of multiple distinct USB devices.

When first plugged into USB, the FX2LP18 enumerates automatically and downloads firmware and USB descriptor tables over the USB cable. Next, the FX2LP18 enumerates again, this time as a device defined by the downloaded information. This patented two-step process, called ReNumeration™, happens instantly when the device is plugged in, with no hint that the initial download step has occurred.

Two control bits in the USBCS (USB Control and Status) register control the ReNumeration process: DISCON and RENUM. To simulate a USB disconnect, the firmware sets DISCON to 1. To reconnect, the firmware clears DISCON to 0.

Before reconnecting, the firmware sets or clears the RENUM bit to indicate whether the firmware or the Default USB Device handles device requests over endpoint zero: if RENUM = 0, the Default USB Device handles device requests; if RENUM = 1, the firmware does.

3.7 Bus-Powered Applications

The FX2LP18 fully supports bus-powered designs by enumerating with less than 100 mA as required by the USB 2.0 specification.

3.8 Interrupt System

The FX2LP18 interrupts are described in this section.

3.8.1 INT2 Interrupt Request and Enable Registers

FX2LP18 implements an autovector feature for INT2. There are 27 INT2 (USB) vectors. See the *MoBL-USB™ Technical Reference Manual (TRM)* for more details.

3.8.2 USB Interrupt Autovectors

The main USB interrupt is shared by 27 interrupt sources. To save the code and processing time that is normally required to identify the individual USB interrupt source, the FX2LP18 provides a second level of interrupt vectoring, called ‘Autovectoring.’ When a USB interrupt is asserted, the FX2LP18 pushes the program counter onto its stack then jumps to address 0x0043, where it expects to find a ‘jump’ instruction to the USB interrupt service routine.

The FX2LP18 jump instruction is encoded as shown in Table 2 on page 5.

Note

1. The I²C bus SCL and SDA pins must be pulled up, even if an EEPROM is not connected. Otherwise this detection method does not work properly.

If Autovectoring is enabled (AV2EN = 1 in the INTSET-UP register), the FX2LP18 substitutes its INT2VEC byte. Therefore, if the high byte (‘page’) of a jump-table address is preloaded at location 0x0044, the automatically inserted INT2VEC byte at 0x0045 directs the jump to the correct address out of the 27 addresses within the page.

Table 2. INT2 USB Interrupts

Priority	INT2VEC Value	Source	Notes
1	00	SUDAV	Setup data available
2	04	SOF	Start of frame (or microframe)
3	08	SUTOK	Setup token received
4	0C	SUSPEND	USB suspend request
5	10	USB RESET	Bus reset
6	14	HISPEED	Entered high speed operation
7	18	EP0ACK	FX2LP18 ACK’d the control handshake
8	1C		Reserved
9	20	EP0-IN	EP0-IN ready to be loaded with data
10	24	EP0-OUT	EP0-OUT has USB data
11	28	EP1-IN	EP1-IN ready to be loaded with data
12	2C	EP1-OUT	EP1-OUT has USB data
13	30	EP2	IN: buffer available. OUT: buffer has data
14	34	EP4	IN: buffer available. OUT: buffer has data
15	38	EP6	IN: buffer available. OUT: buffer has data
16	3C	EP8	IN: buffer available. OUT: buffer has data
17	40	IBN	IN-Bulk-NAK (any IN endpoint)
18	44		Reserved
19	48	EP0PING	EP0 OUT was pinged and it NAK’d
20	4C	EP1PING	EP1 OUT was pinged and it NAK’d
21	50	EP2PING	EP2 OUT was pinged and it NAK’d
22	54	EP4PING	EP4 OUT was pinged and it NAK’d
23	58	EP6PING	EP6 OUT was pinged and it NAK’d
24	5C	EP8PING	EP8 OUT was pinged and it NAK’d
25	60	ERRLIMIT	Bus errors exceeded the programmed limit
26	64		
27	68		Reserved
28	6C		Reserved
29	70	EP2ISOERR	ISO EP2 OUT PID sequence error
30	74	EP4ISOERR	ISO EP4 OUT PID sequence error
31	78	EP6ISOERR	ISO EP6 OUT PID sequence error
32	7C	EP8ISOERR	ISO EP8 OUT PID sequence error

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