CY7C64713

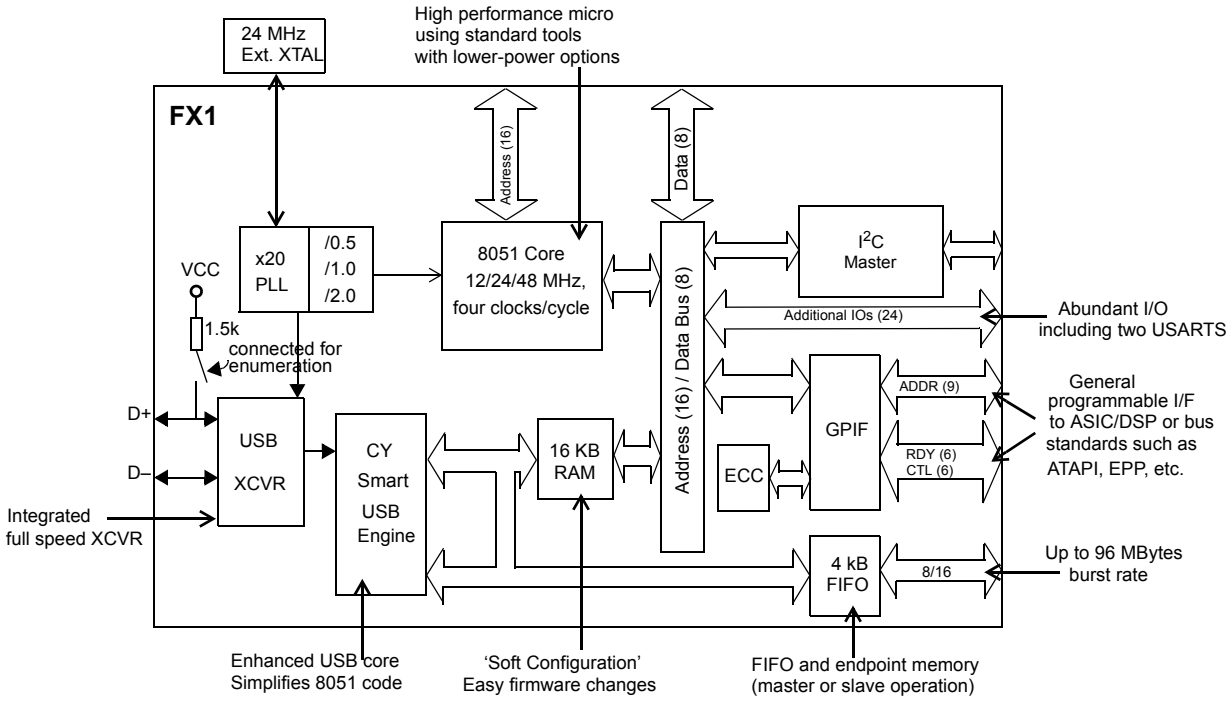
EZ-USB FX1™ USB Microcontroller Full Speed USB Peripheral Controller

Features

- Single chip integrated USB transceiver, SIE, and enhanced 8051 microprocessor
- Fit, form, and function upgradable to the FX2LP (CY7C68013A)
  - Pin compatible
  - Object code compatible
  - Functionally compatible (FX1 functionality is a subset of the FX2LP)
- Draws no more than 65 mA in any mode, making the FX1 suitable for bus powered applications
- Software: 8051 runs from internal RAM, which is:
  - Downloaded using USB
  - Loaded from EEPROM
  - External memory device (128 pin configuration only)
- 16 KB of on-chip code/data RAM
- Four programmable BULK/INTERRUPT/ISOCHRONOUS endpoints
  - Buffering options: double, triple, and quad
- Additional programmable (BULK/INTERRUPT) 64-byte endpoint
- 8- or 16-bit external data interface
- Smart media standard ECC generation
- GPIF
  - Allows direct connection to most parallel interfaces; 8- and 16-bit
  - Programmable waveform descriptors and configuration registers to define waveforms
  - Supports multiple ready (RDY) inputs and Control (CTL) outputs
- Integrated, industry standard 8051 with enhanced features:
  - Up to 48 MHz clock rate
  - Four clocks for each instruction cycle
  - Two USARTS
  - Three counters or timers
  - Expanded interrupt system
  - Two data pointers
- 3.3 V operation with 5 V tolerant inputs
- Smart SIE
- Vectored USB interrupts
- Separate data buffers for the setup and DATA portions of a CONTROL transfer
- Integrated I^2C controller, running at 100 or 400 KHz
- 48 MHz, 24 MHz, or 12 MHz 8051 operation
- Four integrated FIFOs
  - Brings glue and FIFOs inside for lower system cost
  - Automatic conversion to and from 16-bit buses
  - Master or slave operation
  - FIFOs can use externally supplied clock or asynchronous strobes
  - Easy interface to ASIC and DSP ICs
- Vectored for FIFO and GPIF Interrupts
- Up to 40 general purpose IOs (GPIO)
- Four package options:
  - 128-pin TQFP
  - 100-pin TQFP
  - 56-pin SSOP
  - 56-pin QFN Pb-free

Errata: For information on silicon errata, see "Errata" on page 71. Details include trigger conditions, devices affected, and proposed workaround.

Logic Block Diagram



Contents

Functional Description

EZ-USB FX1™ (CY7C64713) is a full speed, highly integrated, USB microcontroller. By integrating the USB transceiver, Serial Interface Engine (SIE), enhanced 8051 microcontroller, and a programmable peripheral interface in a single chip, Cypress has created a very cost effective solution that provides superior time-to-market advantages.

The EZ-USB FX1 is more economical, because it incorporates the USB transceiver and provides a smaller footprint solution than the USB SIE or external transceiver implementations. With EZ-USB FX1, the Cypress Smart SIE handles most of the USB protocol in hardware, freeing the embedded microcontroller for application specific functions and decreasing the development time to ensure USB compatibility.

The General Programmable Interface (GPIF) and Master/Slave Endpoint FIFO (8 or 16-bit data bus) provide an easy and glueless interface to popular interfaces such as ATA, UTOPIA, EPP, PCMCIA, and most DSP/processors.

Four Pb-free packages are defined for the family: 56-pin SSOP, 56-pin QFN, 100-pin TQFP, and 128-pin TQFP.

Applications

- DSL modems
- ATA interface
- Memory card readers
- Legacy conversion devices
- Home PNA
- Wireless LAN
- MP3 players
- Networking

The Reference Designs section of the cypress website provides additional tools for typical USB applications. Each reference design comes complete with firmware source and object code, schematics, and documentation. Please visit http://www.cypress.com for more information.

Functional Overview

USB Signaling Speed

FX1 operates at one of the three rates defined in the USB Specification Revision 2.0, dated April 27, 2000:

Full speed, with a signaling bit rate of 12 Mbps.

FX1 does not support the low speed signaling mode of 1.5 Mbps or the high speed mode of 480 Mbps.

8051 Microprocessor

The 8051 microprocessor embedded in the FX1 family has 256 bytes of register RAM, an expanded interrupt system, three timer/counters, and two USARTs.

8051 Clock Frequency

FX1 has an on-chip oscillator circuit that uses an external 24 MHz (±100 ppm) crystal with the following characteristics:

- Parallel resonant
- Fundamental mode
- 500 µW drive level
- 12 pF (5% tolerance) load capacitors.

An on-chip PLL multiplies the 24 MHz oscillator up to 480 MHz, as required by the transceiver/PHY, and the internal counters divide it down for use as the 8051 clock. The default 8051 clock frequency is 12 MHz. The clock frequency of the 8051 is dynamically changed by the 8051 through the CPUCS register.

The CLKOUT pin, which is three-stated and inverted using the internal control bits, outputs the 50% duty cycle 8051 clock at the selected 8051 clock frequency which is 48, 24, or 12 MHz.

USARTS

FX1 contains two standard 8051 USARTs, addressed by Special Function Register (SFR) bits. The USART interface pins are available on separate I/O pins, and are not multiplexed with port pins.

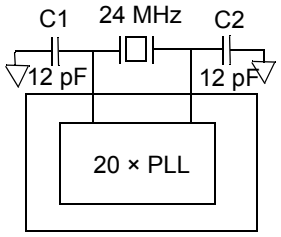
UART0 and UART1 can operate using an internal clock at 230 KBaud with no more than 1% baud rate error. 230 KBaud operation is achieved by an internally derived clock source that generates overflow pulses at the appropriate time. The internal clock adjusts for the 8051 clock rate (48, 24, 12 MHz) such that it always presents the correct frequency for 230-KBaud operation.[1]

Special Function Registers

Certain 8051 SFR addresses are populated to provide fast access to critical FX1 functions. These SFR additions are shown in Table 1 on page 5. Bold type indicates non-standard, enhanced 8051 registers. The two SFR rows that end with ‘0’ and ‘8’ contain bit addressable registers. The four I/O ports A–D use the SFR addresses used in the standard 8051 for ports 0–3, which are not implemented in the FX1. Because of the faster and more efficient SFR addressing, the FX1 I/O ports are not addressable in the external RAM space (using the MOVX instruction).

Note
1. 115-KBaud operation is also possible by programming the 8051 SMOD0 or SMOD1 bits to a ‘1’ for UART0 and UART1, respectively.

Figure 1. Crystal Configuration



12-pF capacitor values assumes a trace capacitance of 3 pF per side on a four layer FR4 PCA

Table 1. Special Function Registers

x	8x	9x	Ax	Bx	Cx	Dx	Ex	Fx
0	**IOA**	**IOB**	**IOC**	**IOD**	SCON1	PSW	ACC	B
1	SP	**EXIF**	**INT2CLR**	**IOE**	SBUF1			
2	DPL0	**MPAGE**	**INT4CLR**	**OEA**				
3	DPH0			**OEB**				
4	**DPL1**			**OEC**				
5	**DPH1**			**OED**				
6	**DPS**			**OEE**				
7	PCON							
8	TCON	SCON0	IE	IP	T2CON	**EICON**	**EIE**	**EIP**
9	TMOD	SBUF0						
A	TL0	**AUTOPTRH1**	**EP2468STAT**	**EP01STAT**	RCAP2L			
B	TL1	**AUTOPTRL1**	**EP24FIFOFLGS**	**GPIFTRIG**	RCAP2H			
C	TH0	**reserved**	**EP68FIFOFLGS**		TL2			
D	TH1	**AUTOPTRH2**		**GPIFSGLDATH**	TH2			
E	**CKCON**	**AUTOPTRL2**		**GPIFSGLDATLX**				
F		**reserved**	**AUTOPTRSETUP**	**GPIFSGLDATLNOX**				

I²C Bus

FX1 supports the I²C bus as a master only at 100/400 KHz. SCL and SDA pins have open drain outputs and hysteresis inputs. These signals must be pulled up to 3.3 V, even if no I²C device is connected.

Buses

All packages: 8 or 16-bit 'FIFO' bidirectional data bus, multiplexed on I/O ports B and D. 128-pin package: adds 16-bit output only 8051 address bus, 8-bit bidirectional data bus.

USB Boot Methods

During the power up sequence, internal logic checks the I²C port for the connection of an EEPROM whose first byte is either 0xC0 or 0xC2. If found, it uses the VID/PID/DID values in the EEPROM in place of the internally stored values (0xC0). Alternatively, it boot-loads the EEPROM contents into an internal RAM (0xC2). If no EEPROM is detected, FX1 enumerates using internally stored descriptors. The default ID values for FX1 are VID/PID/DID (0x04B4, 0x6473, 0xAxxx where xxx=Chip revision).[2]

Table 2. Default ID Values for FX1

Default VID/PID/DID		
Vendor ID	0x04B4	Cypress Semiconductor
Product ID	0x6473	EZ-USB FX1
Device release	0xAnnn	Depends on chip revision (nnn = chip revision where first silicon = 001)

Notes
2. The I²C bus SCL and SDA pins must be pulled up, even if an EEPROM is not connected. Otherwise this detection method does not work properly.

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