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**Sartore et al.**

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- (54) **UNIVERSAL SERIAL BUS INTERFACE SYSTEM AND METHOD**
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- (73) **Assignee:** **Cypress Semiconductor, San Jose, CA (US)**
- (\*) **Notice:** Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

- (21) **Appl. No.:** **09/476,923**
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**Related U.S. Application Data**

- (63) Continuation of application No. 08/886,923, filed on Jul. 2, 1997, now Pat. No. 6,012,103.
- (51) **Int. Cl.<sup>7</sup>** ..... **G06F 13/368**
- (52) **U.S. Cl.** ..... **710/8; 710/9; 710/10**
- (58) **Field of Search** ..... **713/1, 100; 710/8, 710/7, 9, 10; 320/21; 709/220, 221, 250; 711/103-105**

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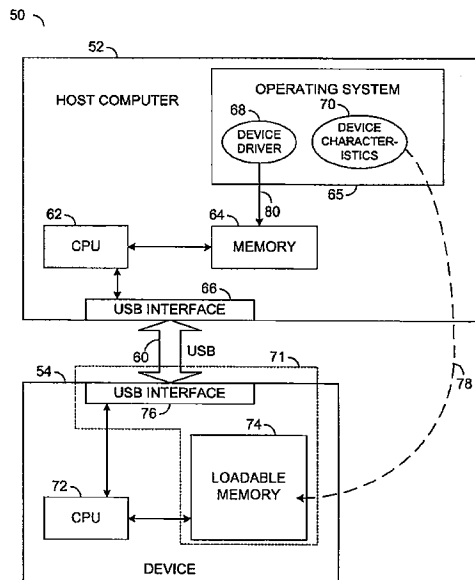
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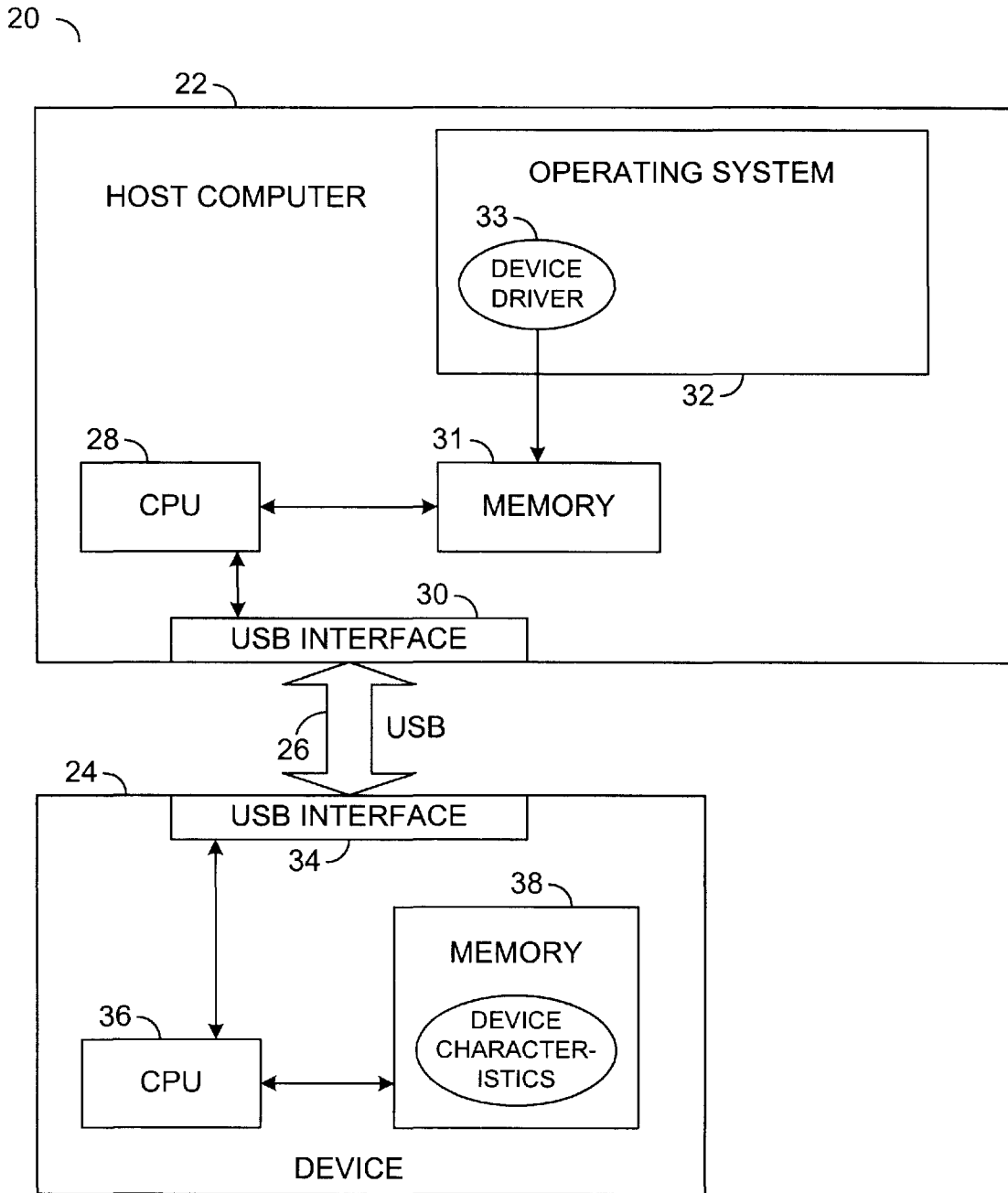
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(57) **ABSTRACT**

A system for reconfiguring a peripheral device having a first configuration connected by a computer bus and a port to a host computer. The system comprises a first circuit and a second circuit. The first circuit may be configured to download information for a second configuration from the host computer into the peripheral device over the computer bus. The second circuit may be configured to electronically simulate, over the computer bus, a physical disconnection and reconnection of the peripheral device to reconfigure the peripheral device to the second configuration.

**20 Claims, 7 Drawing Sheets**





**FIG. 1**  
(PRIOR ART)

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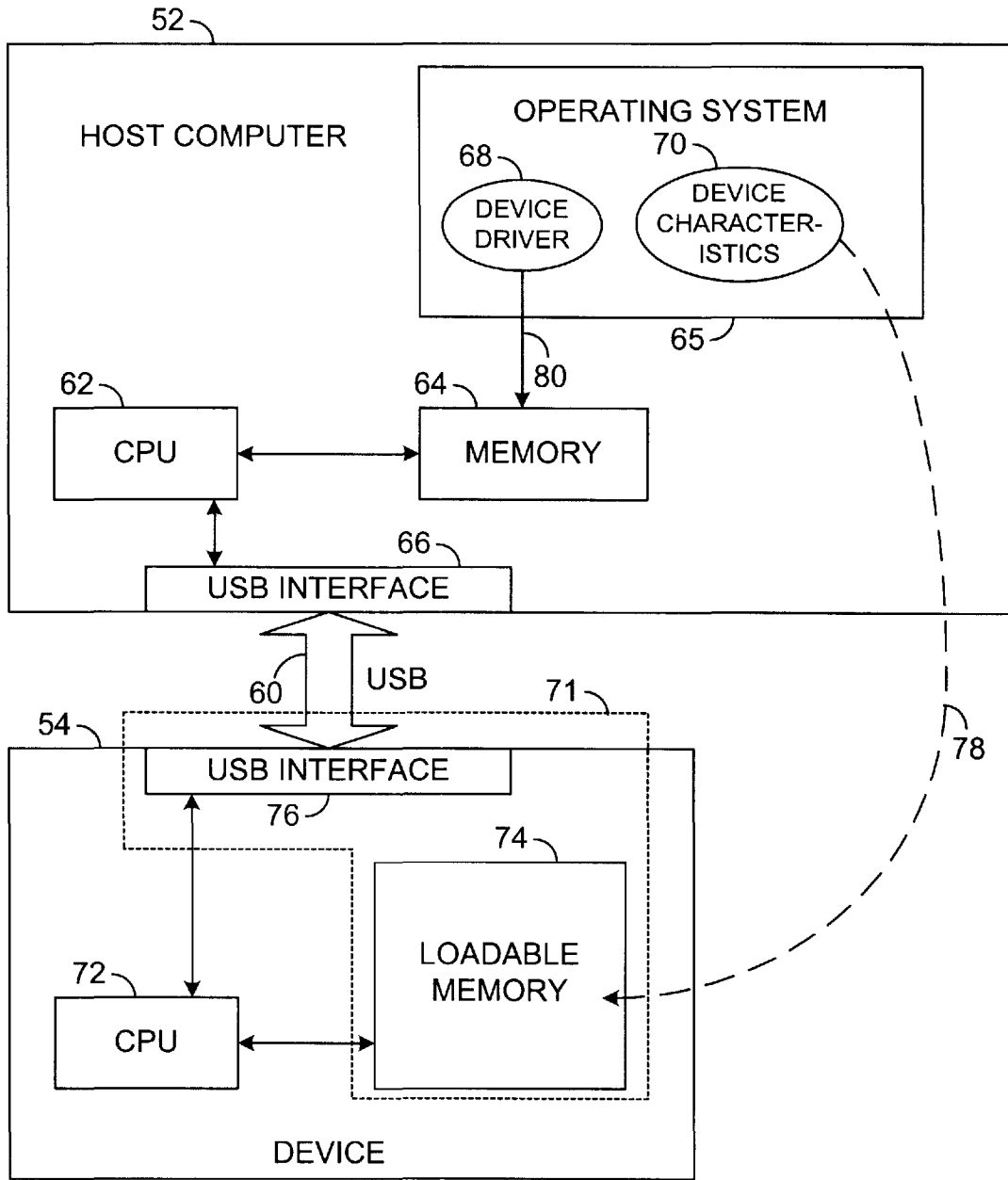
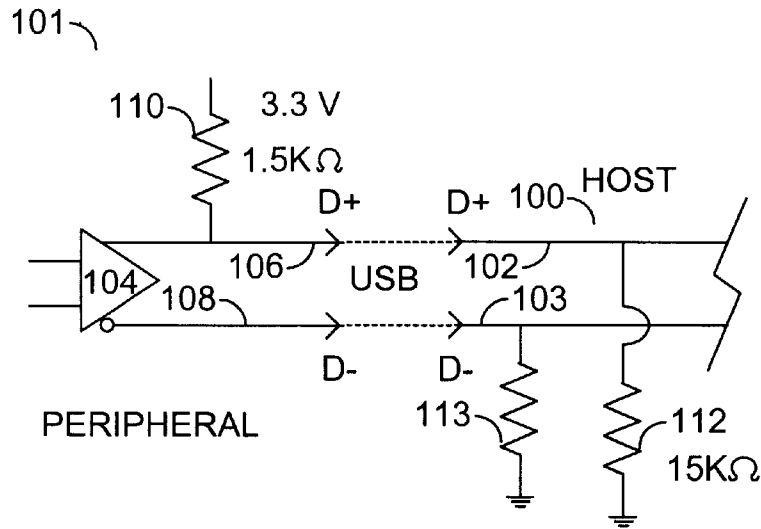
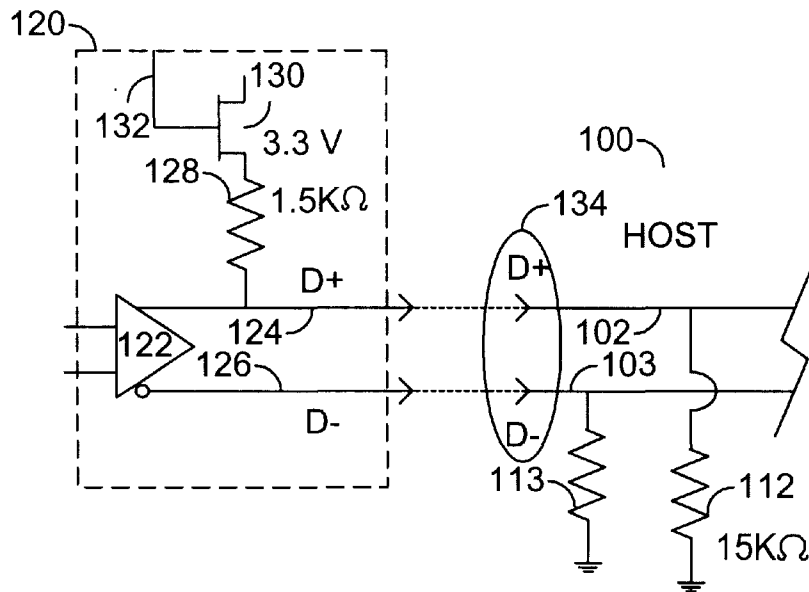


FIG. 2



**FIG. 3**  
(PRIOR ART)



**FIG. 4**

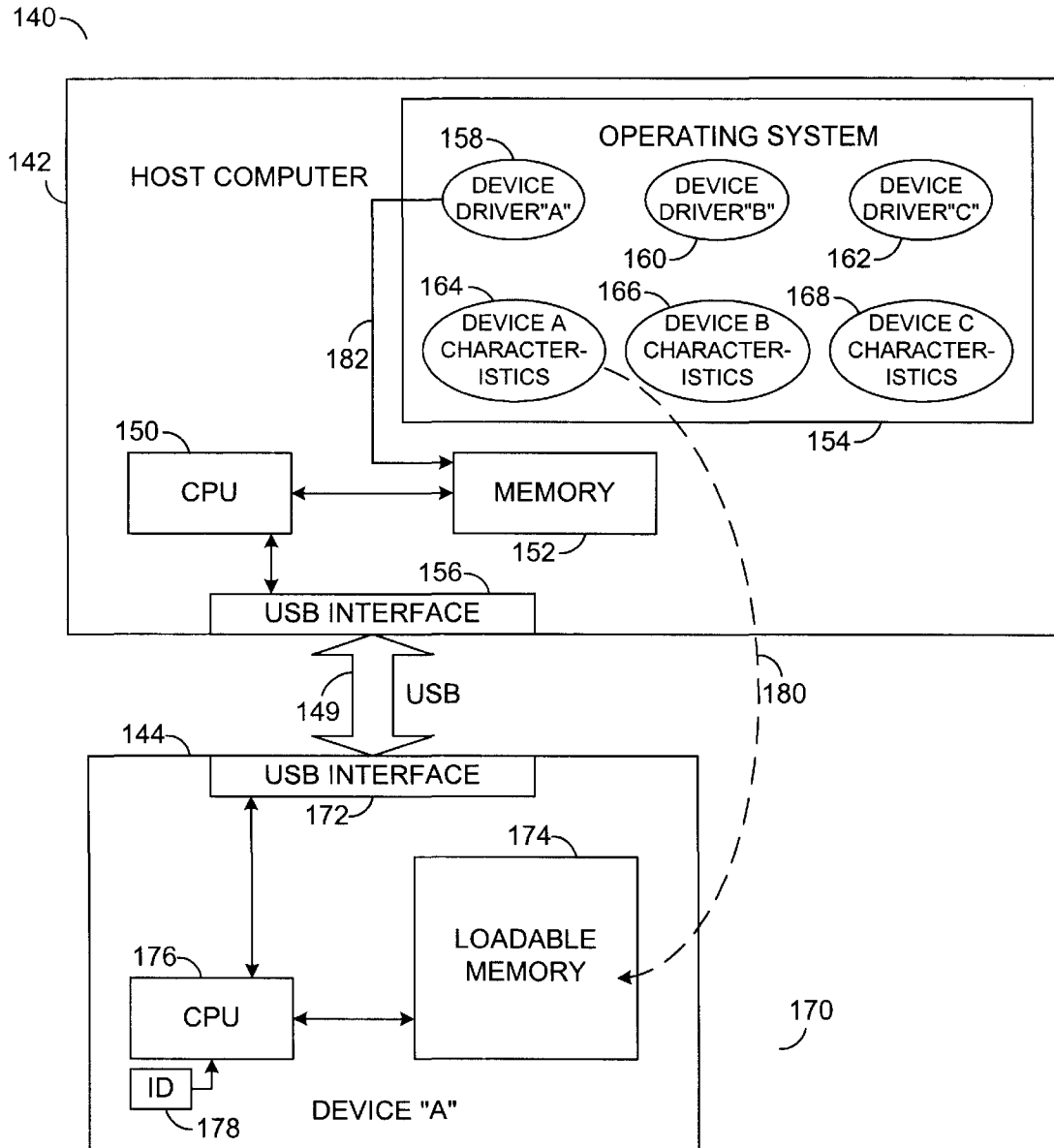


FIG. 5

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