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#95 JUNE 1998

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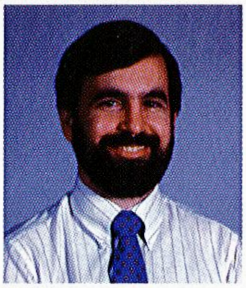

how often do you get the opportunity to influence and shape tomorrow's design engineers? If you're involved in education, you're already there. I'm not talking to you. I'm talking to the engineers who sit in a lab or in front of a computer all day hose community involvement may extend to playing softball with the s rec program.

One of our local universities (Eastern Connecticut State University) is ing the possibility of building upon their already-established computer e program by adding one or more new majors and/or minors. One of eps school officials are taking is to get feedback from the local unity about what programs should be offered and how they should be ured. The Computer Science Advisory Board asked Circuit Cellar to a representative to join the group, and I was elected. Other members e representatives from insurance companies, computer vendors, y and secondary schools, community colleges, and nearby nationally universities.

At our first meeting last night, I was amazed at how well such a e group could work together to discuss a common goal: what can we oday's college students to best prepare them for the changing world S and computer engineering. Being able to tap into my own educa- background coupled with over a decade of work experience, I hope le to offer some useful feedback and suggestions in the coming s.

As a magazine, I like to think we have some influence over row's engineers as well. Many dyed-in-the-wool engineers begin menting with computers and electronics long before entering college. ave many readers who fit that category and who benefit from articles by engineers in the field. We also have our college program in which pply professors with free copies of the magazine for all the students r engineering classes.

So what's my point? I want your help. We've been doing some work r Web site, and are going to start offering perks to subscribers. Among will be short application notes. If you have a favorite tip or technique ou'd like to share, send it along and perhaps we can use it on the site. Our published articles are a technical source for these college nts. Supplemental application notes and technical tips can only add to otal understanding.

At the same time, I want to encourage you to become involved in your school system. Students need to be exposed to computers as early ssible if they are going to come out ahead in today's high-tech y. Teachers have enough to do without having to figure out what's with a PC's configuration or why they can't see the server on the rk. Our readers possess an incredible wealth of computer knowledge, st a fraction of that applied to the schools could benefit dozens of minds.

I look forward to continued work on the Advisory Board. And when my daughter starts kindergarten in a few months, I plan to check with her l to see if I can do anything to help.

Ken

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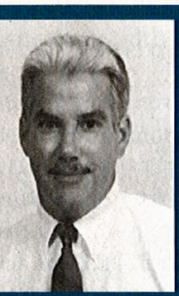
Tom Cantrell

Fabulous '51s



Even though it's been around for a long time, the 8-bit micro keeps on going and going and going. In fact, new variations keep popping up. Tom lets us in on the smarts some of these new ones possess.

No doubt, you've heard dire predictions like "The 8-bit micro is dead." Of course, the source is usually some expert who happens to make a living marketing 16- and 32-bit chips. Or, it might be an analyst who sells rosy studies to those marketeers so they have some ammo for the next staff meeting.

Well, it's nonsense! Statisticians may quibble over the exact number, but there's no doubt the lowly 8-bit MCU plays a huge—and growing—role in our lives. Yes, 16- and 32-bit chips are doing wonderful things, but their strong growth derives from the law of small numbers, not the death of 8-bitters.

Indeed, today's billions of units per year are just the tip of the iceberg. It's not hard to imagine a cyberfuture where little chips permeate our existence.

MCU CLASSIC

I've worked with various companies hoping to enter the micro business. It's critical, but sometimes difficult, to convey to a commodity IC outfit that micros are a different beast altogether.

For example, a manager recently asked me how designers decide which micro to use. To him, if a micro offered a few key features for a good price and delivery, that was all there was to it.

Of course, that's not at all what happens. The decision is driven by human factors. Designers sometimes choose a new chip for the fun of learning it. Usually, though, they rely on their own stable of chips, tools, and accumulated know-how. Only truly compelling technical issues justify the nontrivial challenge and risk of switching to a completely new architecture.

That's why 20-year-old designs like the '51, 68xx, PIC, and Z8 still play a lead role. The issue isn't whether a new architecture is technically superior (not hard with 20 years of hindsight) but whether the old chips are good enough.

MULTISOURCE CODE

Old-timers will remember the heyday of second sourcing, when chip

- Compatible with MCS-51 products
- 8 KB of in-system reprogrammable downloadable flash memory
  - SPI serial interface for program downloading
  - Endurance: 1000 write/erase cycles
- 2-KB EEPROM
  - Endurance: 100,000 write/erase cycles
- 4.0–6-V operating range
- Fully static operation: DC to 24 MHz
- Three-level program memory lock
- 256 × 8-bit internal RAM
- 32 programmable I/O lines
- Three 16-bit timer/counters
- 9 interrupt sources
- Programmable UART serial channel
- SPI serial interface
- Low-power idle and power-down modes
- Interrupt recovery from powerdown
- Programmable watchdog timer
- Dual data pointer
- Power-off flag

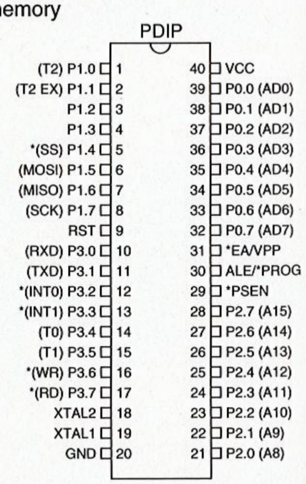
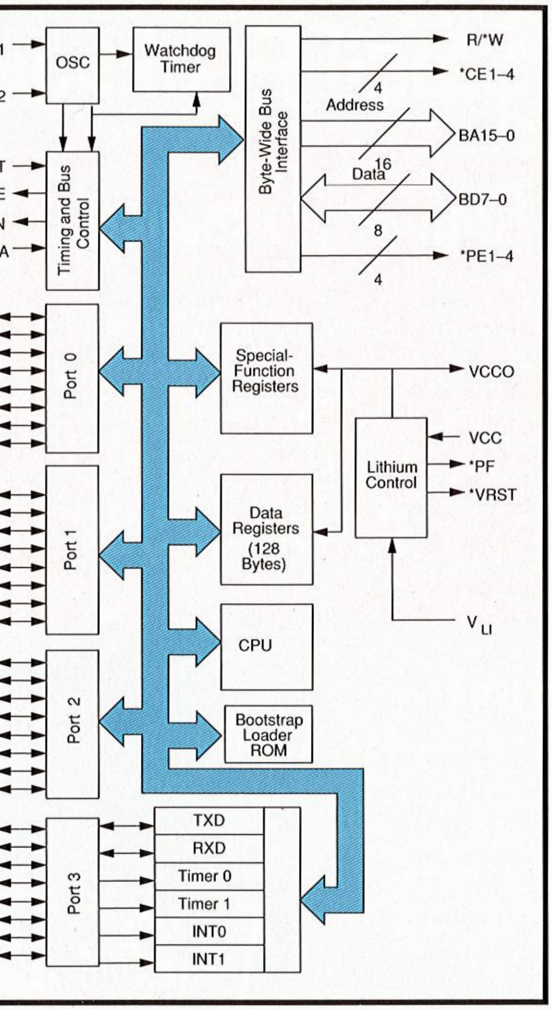


Figure 1—*Atmel, a flash '51 pioneer, offers a new '8252 which incorporates 8-KB flash memory for code and 2-KB EEPROM for data. The chip can be programmed in parallel or serial mode, the latter via a four-pin (select, clock, in, out) SPI interface.*



—The Dallas '5001FP supplements a standard '51 core with a dedicated code and data bus, freeing port pins to handle peripheral I/O functions.

rs battled for designers' share of by encouraging, at least on the , wide sourcing. I remember a ola press conference where they the 68k's big tent with a bunch nsees that included the likes of i, Philips, Rockwell, and others. n a purchasing agent's point of t was the golden age—much as it s for commodity ICs today. You all multiple distributors and get bidding against each other by each that the other guy was until only one was left standing. t might work for DRAMs, but cro business needs more fixed nent (for R&D, tools, etc.), and rofits, than such destructive tition allows. Inexorably, the ourced micro disappeared and practically extinct.

ept for the '51, that is. Of the old var-horses, it's unique by virtue ligate sourcing. It's a veritable people's micro, if you will.

This doesn't mean the laws of economics are repealed. Yes, you can shop around for a cheap, plug-compatible 8051. But don't expect suppliers to cut their own throats. They're about as excited about a lowball '51 deal as the folks at Rockwell or Hitachi are about a 68k inquiry. In other words, don't call me, I'll call you.

What it means is that, across the raft of suppliers, '51 designers have access to a broad spectrum of products—a lineup more extensive than possible from any single supplier. Furthermore, it means the '51 is continually freshened and upgraded, ensuring that the technology gap with newer architectures doesn't get too wide.

Finally, although true plug compatibility is limited to the old baseline chips, plug similarity goes a long way towards ensuring healthy competition. It's a lot easier to switch from one '51 to another with a few different features than to a completely new architecture.

Let's take a look at the latest developments on the '51 front, and you'll see what I mean.

FLASH IN YOUR FUTURE?

Flash micros are starting to take off, and there's a lot of reason to believe they'll become even more popular. Atmel, the undisputed leader in flash-based '51s, is well-positioned for such an eventuality. However, Philips (the largest '51 supplier overall) has recently announced plans to join the fray.

Before checking out the parts, realize that all flash micros aren't created equal. For example, first-generation flash micros are little more than an EPROM/OTP replacement because they use the same parallel programming scheme, 12.5 V_{PP}, and so on.

This is OK, but it really doesn't support the popular idea of streamlined assembly line programming. Sure, it's possible to kludge together some kind of hack for a pseudo-EPROM flash chip (e.g., muxes for all the pins, switchable 12 V_{PP}, etc.), but it isn't clean.

By contrast, Atmel's latest flash '51s, such as the 89S8252 shown in Figure 1, offer the best of both worlds. They still support parallel, high V_{PP} programming for those happy to stick with gang programming.

At the same time, they include a serial programmer that only needs a few pins (SPI interface) and a single power supply (5 V). Holding

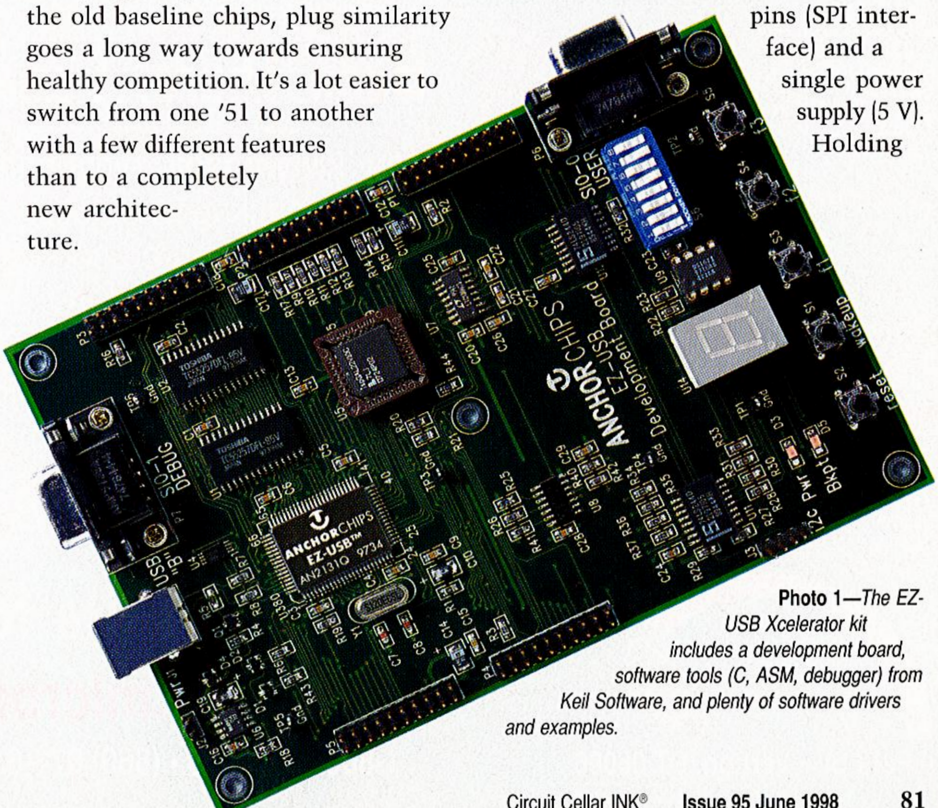


Photo 1—*The EZ-USB Xcelerator kit includes a development board, software tools (C, ASM, debugger) from Keil Software, and plenty of software drivers and examples.*

the part in RESET invokes the serial programming mode, which lets the flash (and extra 2 KB of on-chip data EEPROM) change a single byte at a time (i.e., no need to erase the entire chip).

The new Philips 89C51RX+ dishes up another flavor of flash memory. Like Atmel, Philips supports traditional parallel and in-system programming (ISP) modes.

However, the Philips ISP philosophy is subtly, but profoundly, different from Atmel's. Both parts are ISP in the sense of easy post-PCB assembly (re)programming. Philips goes a step further with self-programming that enables the chip to dynamically change its own code.

Here's how it works. A Boot ROM overlays the top 1 KB of code space, which contains routines to erase a block, program byte, verify byte, and so on. There's also a Boot Vector that defines what happens after RESET depending on the state of a flash-status byte. Execution at the Boot Vector can also be forced by external pin setting.

The Boot Vector in turn points to a user-written Loader in one block of the flash memory that's responsible for erasing and programming the other blocks. The Loader, taking advantage of calls to the Boot ROM, can self-program the chip using any technique. For example, using the 89C51RX+, you can remotely (re)program it via modem a built-in feature of your design.

Note the default shipping configuration includes a prewritten Loader to accept commands and data via the on-chip UART. That means a factory-fresh part can be inserted in a board and programmed serially at a later time.

One key difference: in serial programming mode, the Atmel part only needs 5 V, whereas the Philips uses 12 V. For compatibility with existing programmers, both require high voltage for parallel programming.

Otherwise, Atmel and Philips parts have a lot of other neat features and upgrades. They have dual data pointers, fancier peripherals, watchdog timers, faster clocks, and more. Designers are sure to benefit from the battle for their flash '51 favor.

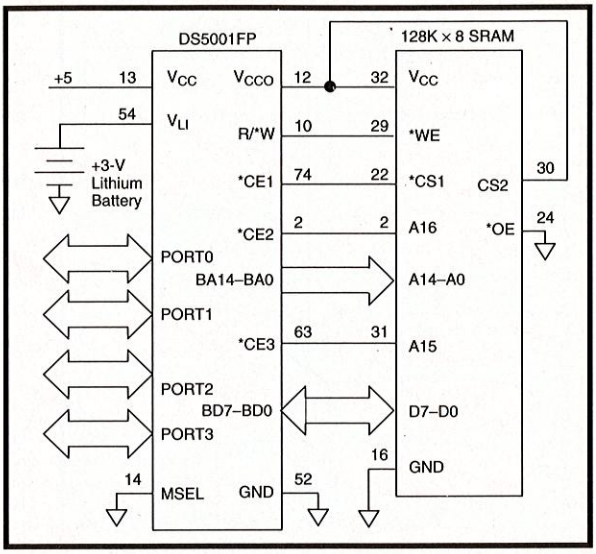


Figure 3—*With built-in voltage supervisor, battery switching, and bootstrap ROM, the '5001FP is especially well-suited for SRAM connection. The chip completely manages the SRAM power and control signal generation, maintaining data integrity without needing any glue logic.*

'51 RAM CRAM

Dallas Semi is known for its fast (4 clock/instruction at 33 MHz) 80C320, but it has other tricks up its sleeve, too.

The DS5001FP depicted in Figure 2 is an interesting alternative that combines a vanilla '51 with a dedicated byte-wide memory bus, so adding external memory doesn't consume I/O port pins. Four chip enables (*CE1–4) support various combinations of 32-KB blocks for a total of up to 128-KB memory. Likewise, four peripheral enables (*PE1–4) handle data accesses.

While any type of memory can be used, the DS5001FP is especially well-suited for SRAMs (see Figure 3). An on-chip voltage supervisor not only generates power-fail detect (*PF) and reset (*VRST) but also controls the previously mentioned byte-wide bus enables to prevent spurious writes.

Like Philips' flash parts, the '5001 includes a bootstrap loading feature that downloads the SRAM via serial port after first-time powerup. Once initialized and verified, the bootstrap loader leaves the stage, and power-management logic ensures that the SRAM remains valid (up to 10 years, depending on the battery). The SRAM need never again be touched (at least until the battery runs dry), but it can be rebootstrapped as often as desired by driving the *PROG input.

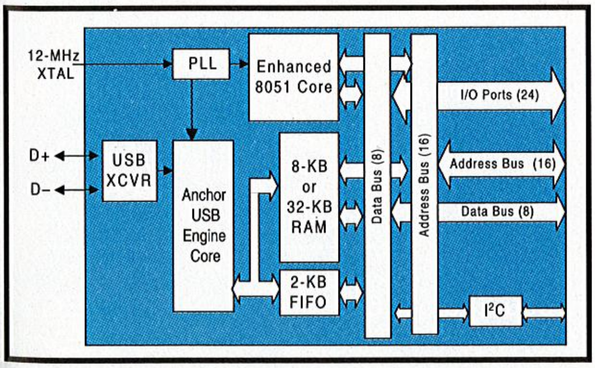


Figure 4—*When USB finally starts rolling, look for '51-based derivatives like the Anchor Chips AN21xx to get onboard.*

Besides the '5001 chip, Dallas also offers the DS2251T module, which combines the MCU with a 32–128 KB of SRAM, real-time clock, and battery.

"OH SAY CAN USB?"

That was the title of my article about USB in *INK* 74. There, I pointed out that the USB concept was grand, especially compared to the ludicrous rat's nest of parallel, serial, mouse, game pad, and so forth lurking behind PCs.

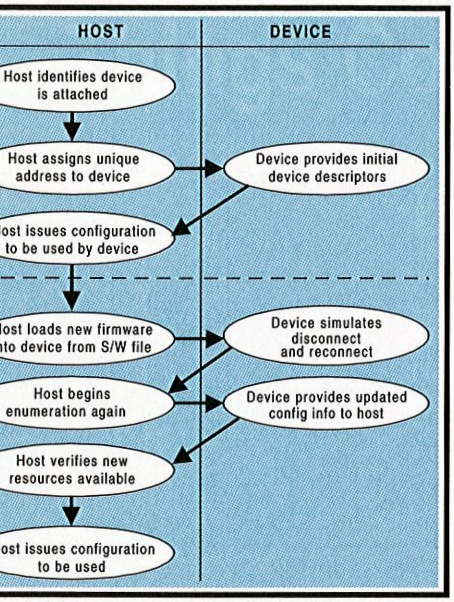
However, the downside of vaunted PC compatibility is inertia. I correctly reckoned USB wouldn't take off until the arrival of a critical mass of built-in driver software with Win98.

Despite the fact there's a zillion USB-capable PCs out there, the vast majority of USB ports are gathering dust.

The issue is complicated by the fact that Win98 seems to be slipping (no real surprise), with the rather interesting kicker that an awful lot of lawyers are involved. As well, the quality and quantity of USB support in Win98 remains to be seen. I overheard one Microsoft engineer saying they've "got more important networks to deal with."

The transition to Win98 and/or USB may not be as quick and clean as anticipated. At this point, USB is scratching for each peripheral design and inch of shelf space one torturous step at a time.

Ultimately, however, I believe the combination of automatic-installed base (i.e., USB on every motherboard) and



—Booting up the AN21xx is a two-step process. First, normal USB enumeration cycle, and application-specific downloaded into the on-chip RAM. Next, renumeration es the PC to the now-personalized chip.

sanity will prevail. And when the market for USB chips—no of them '51 based—will explode. AN21xx from Anchor Chips is example of the way new blood keeps the '51 young at heart. It combines the best aspects of other derivatives in a unique combination (see Figure 4).

Anchor Chips starts with a hot-rodded four-clock/instruction core. A PLL fed by an external 12-MHz crystal generates the 24-MHz CPU clock and 12-/1.5-Mbps (high/low data rate) USB clock.

The USB engine is powerful, with a default device descriptor that lets it boot as a generic device. Logic handles the low-level transfer details, accomplishing an entire multipacket transaction in hardware. Thus, according to Anchor, managing the network consumes only 10% of CPU bandwidth, leaving the rest for application-specific processing.

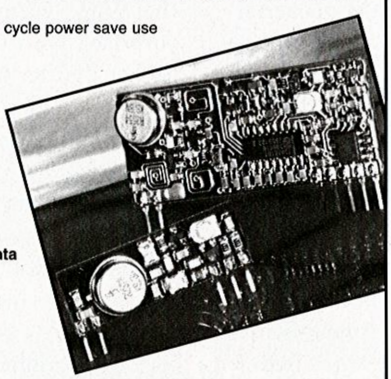
Although a ROM version is available, Anchor's claim to fame is exploiting on-chip RAM—and there's a lot of it (up to 32 KB). There's also an extra 2 KB of USB FIFO which, using a ping-pong approach, supports full 1024-byte isochronous (i.e., time-sensitive stuff like audio, video, and high-speed data acquisition) packet transfers in less than half of a single 1-ms USB frame.

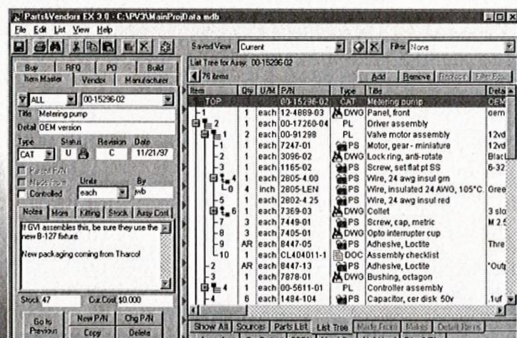
The chip comes in low-cost 44- and 80-pin PQFP packages (Photo 1). Larger versions support external expansion by bringing the address and data bus (non-muxed, don't need a latch) off chip.

Another variant brings out only the data bus for connection to an external FIFO, providing dedicated read and write pins (*FRD, *FWR) to drive it. Otherwise, every version of the chip includes an I²C port and 24 I/O lines configurable to function as PIO or the usual alternates (e.g., UARTs, timers, interrupts, etc.).

Of course, a RAM-based design raises the obvious question of how to install code after powerup? One approach, like an FPGA, relies on accessing an external boot memory (either I²C or parallel) to load the on-chip RAM after powerup.

Anchor calls its more novel approach "renumeration." The USB spec requires bus enumeration when a peripheral disconnects or connects (i.e., hot plug).





At powerup, the Anchor chip automatically enumerates as a default USB device. Then, as shown in Figure 5, a host PC downloads the '51 code via the USB connection into the on-chip RAM.

Once loaded, the chip simulates a disconnect/reconnect, causing the host PC to renumerate. This time, Anchor's chip responds to interrogation with the just downloaded device description.

This feature provides a neat chameleon-like capability. For instance, take a piece of USB-based data-acquisition gear with a variety of functions and modes. Depending on the task, an Anchor-based solution can switch hats by redefining the number of endpoints (up to 16), type of connection (e.g., isochronous, bulk, interrupt, control), and FIFO allocation appropriately.

AND THE CHIP PLAYED ON

The 8-bit micro was initially pronounced dead 20 years ago during the height of the original showdown between the 8086 and 68k.

The marketing guy giving the premature eulogy moved on to a small startup. The company did very well over the years, making him quite wealthy along the way.

If you haven't already guessed, that company's success was based in no small part on a popular line of 8-bit chips! You can bet I always ask him if the 8-bit market is dead yet every time I see him.

MCUs may come and go, but '51s are here forever. ■

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