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John Garney

Objective

To provide critical computer hardware and software expertise to successfully resolve intellectual property proceedings.

Summary of Qualifications

Demonstrated strong broad and deep individual contributor skills in: computer system new technology architecture definition, analysis and specification; cross business group communication and group leadership. Proven ability to derive specific technical requirements from vague problem areas and work in broad PC industry environments to stimulate deployment of new technologies (e.g. PCMCIA, CardBus, Plug&Play, Power Management, Universal Serial Bus 1.0, 2.0, 3.0 & 3.1). Consistently recognized by peers and managers for my ability to rapidly assimilate and master new technical areas and then become acknowledged as a key leader in driving additional technical progress. Widely respected for ability to generate, articulate, and critically analyze: technical proposals, concepts and specifications. Extensive hands-on experience with prototyping/debugging/analysis of hardware/firmware/software. 27+ years experience in various research and development assignments in the PC industry. Provided expert witness services to 6 clients, to date; all have settled out of court.

Work experience

2007 – Present Garney Consulting, L.L.C. Portland, OR

System Architect (consulting/expert-witness services to client companies)

- Vice-Chair of USB 3.0 10G Hub Working Group. Member of other USB 3.0 10G Working Groups and extensive reviewer of drafts in progress.
- Major technical contributor to USBIF UASP Device Class Working Group compliance test definitions.
- Intensive debugging of reliability problems and workarounds for USB 2.0 Hub in consumer home network product that successfully resolved customer release problems.
- Support USB-IF Peripheral Integration Lab testing of customer products using client company USB software stack. Usually requires analysis of operational failures and USB specification requirements to determine required corrective action in either/both customer or client company software/hardware.
- USB 3.0, xHCI & UASP (USB Attached SCSI Protocol) embedded product architectures: Detailed analysis/review of USB 3.0 SuperSpeed Stream protocol and state machines resulted in numerous clarifications in Errata. Review of xHCI specification and listed as a contributor in the published Intel document. Client company advisory representative to ANSI T10/CAP/UAS working group and USB-IF UASP working group. Member of USB-IF Mass Storage, OTG2, OTG3 and AV working groups.
- Wireless USB projects: Refined overall WUSB embedded system device and host architectures extending existing client products. Work involved several on-site, international, three-way customer, in-depth technical discussions. Defined embedded system (cell phone appropriate) Cable Association Method (CAM) protocol interfaces for host and device side, supporting Wireless USB CAM requirements. Proposed embedded system device-side Numeric Association Method (NAM) protocol interfaces. Drove key requirements into definition of radio controller interface. Defined cryptographic product

requirements for host and device in support of WUSB and WiMedia functionality suitable for RFQ technical details. Client company representative to WiMedia Embedded Controller Interface and WiMedia Association Method Workgroups.

- Reviewer of USB 3.0 draft specifications.
- Delivered 2 3-day USB 2.0 Training Workshops (Germany, Norway) providing in-depth material on core aspects of USB 2.0. Included hand's-on USB bus trace analysis of actual USB products.
- Provided expert witness services for several USB patent infringement cases in the US and UK; involving storage, configuration and other USB technologies. Analyzed patents and wrote expert report on plaintiff claims. Cases were settled out of court before going to deposition or trial.

1989 - 2007 Intel CorporationHillsboro, OR

Sr. Staff Software Architect, Corporate Technology Group & Intel Architecture Labs

A variety of technology Research & Development assignments from 1-3 years duration each. Many required Microsoft interactions to achieve broad PC industry acceptance.

- System architect for cross platform (handheld/mobile, desktop, server) exploration expanding on virtualization/partitioning advanced technologies. Established design directions for provisioning, chain-of-trust, isolation and communication mechanisms in investigations of possible future IA32 platforms. Made proposals to CPU and chipset architects for new instructions and silicon inter process/processor communication features in support of this overall technology. Provided technical leadership/direction to many other engineers on the team in US and India.
- Software project lead for new high density, non-volatile, silicon storage technology development. Responsible for overall software architecture definition of a disk caching subsystem (extension of Intel Application Accelerator 3.5) including HW programming interface definition. Oversaw demos delivered to ESM and other VPs. Acting project manager of 4 person geographically distributed team until fulltime manager hired. Developed analytic model to estimate silicon area requirements. Eventually deployed as Intel Robson disk cache/storage technology and current Intel SSDs.
- Universal Serial Bus 2.0: Intel technical lead/chair for protocol, hub and other non-electrical definitions. Proposed, defined and drove ratification of transaction translator (core element of USB2.0 Hubs) in international, cross company working group. Engaged with Intel Desktop Products Group to define Enhanced Host Controller Interface product specification with other junior engineers. USB2.0 received PC Magazine Best New Technology award. Received Intel Achievement Award 2003 for USB. Stable specification broadly adopted in PC industry.
- Isochronous Data Platform Support: Proposed and defined advanced features in chipset hardware for higher quality, lower cost streaming data support (video, audio, etc.). Engaged with Desktop Products Group Sr. Architects for future chipset product plans.
- 3D Graphics: Developed detailed analytic model of Microsoft Talisman architecture for non-DSP implementation of chunk based 3D rendering with on-the-fly sprite compositing. Defined basic driver framework pursued by software team and contributed to key decisions related to hardware performance implementation choices. Efforts contributed to Intel suspending their involvement in developing this technology. Assignment included achieving Microsoft acceptance of Intel's contributions and requirements in the published PC98 3D Graphics chapter (as chapter editor).

- Universal Serial Bus 1.0: Intel technical lead for V1.0 Specification creation, adoption and USB core team interactions. Wrote core system architecture chapter (5), coordinated other chapters and delivered many presentations/tutorials at other companies and industry events (WinHEC, Intel, Telephony Conferences). Specification stability contributed to mass market availability in less than 3 years from initial specification. Extensive hands-on technical leadership during prototype/debug/certification of early USB products by Intel and other USB vendors.
- Plug and Play, Power Management: Extensive work with Microsoft technical experts to define OS architecture for enhanced functionality. Member of Microsoft team and recognized by Microsoft VP as being significant contributor to definition of Plug and Play for Windows95.
- Intel's PCMCIA software representative: extensively reviewed PCMCIA pre-2.0, co-defined software interfaces (Card and Socket Services, 200+ pages) sections of PCMCIA 2.01 (November 1992) and 2.1 (July 1993), wrote Intel compatible subset definition that was subsequently adopted by PC industry (ExCA) for dependable card interchange, managed team that enhanced 16 bit definition to 32 bit PCI related extension (CardBus). Specification stability and accurate understanding of other industry players contributed to enrolling Microsoft as active supporter vs. detractor. Software architect for 2 Intel HW product teams building 2 different PCMCIA host adapters, both incorporated in 3rd party laptops. Demonstrated PCMCIA Execute-in-Place (XIP) prototype tools/driver for converting commonly available Windows 3.x applications (such as MS Word and Powerpoint) and executing them directly from a flash memory card (without requiring copy to DRAM).

1988 - 1989 BiiN CorporationHillsboro, OR

Staff Software Architect/ Project Leader

- Responsible for fault tolerance(FT) software design of BiiN/OS and member of security design team. Specified and designed overall system architecture for hardware/software FT including: online module replacement, dynamic selection of FT level and detection/recovery of hardware/software subsystem failures. Integrated/debugged core OS software with novel fine-grained protection domain, capability based hardware. Developed method for function inheritance support for a strongly typed, hardware enforced (i960XA) abstract type manager environment. Involved in design of OS enhancements to pursue NCSC B2 Security Rating. Project leader and indirectly provided leadership for many other developers. Working FT functionality was in alpha test phase at termination of company. BiiN was a joint venture spun off by Intel/Siemens that provided a "golden parachute" return to Intel upon its demise.

1980 - 1988 Intel CorporationHillsboro, OR

Software Architect/ Project Leader

- Steadily advanced through variety of assignments in software evaluation of several operating systems (iRMX 80/88/86, iMAX/432) and then OS subsystem design/development (overall IO architecture, initialization/ shutdown, dynamic reconfiguration of BiiN/OS). Also established software development methodologies and reference drivers for use by other team members. Recognized as key technical leader for all OS driver development.

Various years

Personal Projects

Various projects for home automation involving hardware/circuit design, PCB layout, firmware and software design/development and integration testing.

- Reverse engineered Litetouch 2000 low voltage residential lighting control protocol and designed/ implemented Scenix SX28 microcontroller hardware/firmware protocol module that converted between RS232 serial commands/events and Litetouch proprietary protocol.
- Reverse engineered Kustom whole house audio wall control protocol and designed/ implemented Scenix SX28 microcontroller hardware/firmware protocol module that converted between RS232 serial commands and Kustom wall control protocol.
- Designed/built ultra low power, battery powered, wireless radio sensor modules using PIC12F6xx microcontrollers for sensing light, contact closure and temperature. Custom radio protocol designed including support for detection of missed reports and current battery level. Designed Rabbit 2000 ethernet connected based radio receiver. Used to detect: water heater pilot light vs. main burner lit, mousetrap trigger, day/night, and room temperatures. 16 sensors deployed with rolling 3 year readings logged and displayed via web interface.
- Designed/built Rabbit 2000 microcontroller based, 2x40 character VFD ethernet connected general purpose display console. Used to display time/date and various household/weather status indications.

Education

1978 - 1980 Purdue UniversityWest Lafayette, IN

M.S. Computer Science

1975 - 1978 Purdue UniversityWest Lafayette, IN

B.S. Computer Science & B.S. Mathematics

References

Available upon request

Patents, Publications and Presentations

62 patents granted; 12+ as solo inventor; usually the lead inventor for all patents. Approximately 12 patents pending.

Patents are in a variety of computer system areas including: operating system device drivers, BIOS, 3D graphics, serial buses (such as USB), disk caches, memory buses. For example, *Device driver configuration in a computer system (1994), System for copying device driver stub in allocated portion of system memory corresponding to receiving resource to enable device driver execution from resource memory (1995), Preservation of a computer system processing state in a mass storage device (1995), System for enabling access to device driver residing in resource memory corresponding to coupled resource by allowing memory mapping to device driver to be executed (1995), Method and apparatus for executing applications in place from write once/seldom memories (1996).*

Involved in several Patent Trademark Office (PTO) Office Actions to resolve questions pertaining to pending patent applications. Frequently asked to review patents from other inventions to clarify novelty of a pending patent. On one occasion, flown to Wash. D.C. to meet directly with patent examiner to expedite patent application.

Full patent list available on request.

Jan-Mar 2000: CS350 Adjunct Professor at Portland State University

Taught Winter Term CS350 Course

Catalogue Description: Techniques for the design and analysis of algorithms. Problem solving. Case studies of existing algorithms (sorting, searching, graph algorithms, dynamic programming, string matching). NP-completeness.
Prerequisites: CS 252
Goals: To develop a group of useful algorithms which can be used to solve common problems. The development of tools and principles for analyzing the time, space, and correctness used by these algorithms.

1997-1999: Co-developed and taught several 2-day USB 1.0 workshops

Co-developed 2-day class material on Universal Serial Bus 1.0 and taught many 10-40 person classes over 1+ years. Some classes taught internationally.

1998: Lead Co-author of "USB Hardware and Software" Book

Technical reference book "USB Hardware and Software" (ISBN 0-929392-37-X) written with 4 other authors and published in 1998. Also available in Japanese translation. Wrote chapters 1, 3, 7 & 8. Coordinated book review and assembly.

2000: USB 2.0 Hub Working Group chairperson/editor/technical-lead

Hub working group chairperson/editor for Universal Serial Bus (USB) Technical Specification Revision 2.0. Responsible for driving technical details/solutions for all non-electrical areas of USB 2.0. Defined, designed, proposed, defended and wrote almost all high speed details in Chapter 5 (USB Data Flow Model), Chapter 8 (Protocol Layer), Chapter 11.14-11.22 (Hub Transaction Translator). Inventor of transaction translator extension to USB hubs (a central element of USB 2.0). Only minor errata has been released for the specification since its publication in April 2000.

Spoke at international conferences with simultaneous translation (Taiwan and Japan)

USB Developers Conferences, WinHEC conferences (on USB, Power Management and Plug and Play).

Intel Software Developer's Conference 1996, 1997 papers.

Awards received

Intel Achievement Award 2003 (USB2.0), Intel Architecture Labs Divisional Award, Intel Software Developer's Conference: Best Paper, several Business Group Recognition Awards. USB Developers Conference: Best Speaker.

Keywords: Operating Systems, USB, PCMCIA, PCCard, Fault Tolerance, Hot plug, disk cache, 3D graphics, power management.

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