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LG Elecs. v. Cypress Semiconductor IPR2014:01396, U.S. Pat. 6,249,825

PCMCIA PC CARD STANDARD Release 2.1

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## **Release Record**

#### Edition

#### Release 1.0 Release 2.0 Release 2.01 Release 2.1

#### Date Published November, 1990 September, 1991 November, 1992 July, 1993

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July, 1993

PC CARD ATA SPECIFICATION 1.01

CARD SERVICES SPECIFICATION 2.0

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PC CARD ATA SPECIFICATION 1.01

SPECIFICATION 2.0

RECOMMENDED

CARD SERVICES SPECIFICATION 2.0

3-5

The interconnect system shall pass all requirements of subsection 3.4 (Connector Reliability) and subsection 3.5 (Connector Durability).

If a connector ejector mechanism is used, it is recommended the ejector mechanism pass all requirements for reliability and durability, as applicable, in subsections 3.4 and 3.5.

## 3.3 PC Card Guidance

The PC Card shall be guided by the host connector for a minimum distance of 0.394" (10.0) before the socket connector bottoms on the host (pin) connector (Figure 3-15).

To ensure alignment of the PC Card to connectors, the PC Card should be guided for a minimum distance of 1.570" (40.0) before engagement.

### 3.4 Connector Reliability

The interconnect system as specified in subsection 3.2 shall meet or exceed all reliability test requirements of this subsection. Unless otherwise specified, all test and measurements shall be made at:

Temperature	emperature 15°C to 35°C	
Air pressure	650 to 800 mm mercury (860 to 1060 mbar)	
Relative humidity	25% to 85%	-

If conditions must be closely controlled in order to obtain reproducible results, the parameters shall be:

Temperature	23°C +/- 1°C	
Air pressure	650 to 800 mm mercury (860 to 1060 mbar)	
Relative humidity	50% +/- 2%	1.178

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## PCMCIA PC CARD STANDARD

Release 2.01

CARD PHYSICAL **Connector Reliability** 

#### **Mechanical Performance** 3.4.1

The interconnect system mechanical performance is specified as follows:

#### **Office Environment** 3.4.1.1

1	STANDARD	TESTING
		Paragraph 3.5.1
	Guaranteed number of insertions/ejections =10,000 min.	

#### Harsh Environment 3.4.1.2

STANDARD	TESTING	
Guaranteed number of insertions/ejections = 5,000 min.	Paragraph 3.5.2	

#### **Total Insertion Force** 3.4.1.3

STANDARD	TESTING
8.8lbs (4kg) max.	Insert and extract at speed of 1" (25mm)/min.

#### **Total Pulling Force** 3.4.1.4

STANDARD	TESTING
1.5lbs (.68kg) min.	Insert and extract at speed of 1" (25mm)/min.

#### Single Pin Pulling Force 3.4.1.5

STANDARD	TESTING
0.022lbs (10g) minimum initial value only.	Pull the gauge pin shown to left at speed of 1* (25mm)/min. Gauge pin's surface must be wiped clean of dirt and lubrication oil.
Gauge: Material - Tool making steel Hardness - HRC = 50 to 55	

#### 3.4.1.6 Single Pin Holding Force

STANDARD	TESTING
Pin shall not push out of the insulator when 2.2lbs (1kg) minimum force is applied to the pin.	Push pin on the axis with 2.2 lbs (1kg) minimum force while holding insulator rigid.
	1.1 lbs Min Force PIN

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## 4.3.2 Data BUS (D0-D15)

Signals D0 through D15 constitute the bidirectional data bus. The most significant bit is D15. Bit number (and significance) decrease downward to D0.

## 4.3.3 Card Enable (-CE1 & -CE2)

The -CE1 and -CE2 lines are active-low, card-enable, input signals. The -CE1 input enables evennumbered-address bytes and -CE2 enables odd-numbered-address bytes. A multiplexing scheme based on A0, -CE1 and -CE2 allows 8-bit hosts to access all data on D0 through D7 if desired. See Table 4-7.

To ensure data retention on battery-backed-up SRAM cards, and permit power-up initialization of peripheral cards, a minimum of 20 milliseconds must elapse after:

- 1. the application of Vcc to the card, or
- 2. the end of the RESET signal to the card (in systems which support the RESET signal),

whichever event occurs latest.

The card enables are used to access both Common and Attribute Memory, and to access 1/0.

Refer to Section 4.7 for additional information on Common Memory Read Functionality.

Refer to Section 4.14 for additional information regarding I/O Read and Write Functionality.

#### 4.3.4 **Output Enable (-OE)**

The -OE line is the active-low, input signal used to gate Memory Read data from the memory card. SRAM memory cards fall into two categories:

- 1. cards where the -OE signal must be negated during write operations, and
- 2. cards that do not use the -OE signal during write operations and allow the signal to be in either state.

Hosts must negate the -OE signal during write operations.

#### 4.3.5 Write Enable/Program (-WE/-PGM)

The -WE/-PGM input signal is used for strobing Memory Write data into the memory card. This line is also used for memory cards employing programmable-memory technologies. See Section 5.2.6 for identification of Programmable Memory Technology cards.

#### 4.3.6 Ready/Busy (+RDY/-BSY)

The Ready/Busy function is provided by the +RDY/-BSY signal when the card and the host socket are configured for the Memory-Only Interface. When a host socket and the card inserted into it are both configured for the I/O interface, the +RDY/-BSY function is provided by the +RDY/-BSY status bit in the card's Pin Replacement Register. When the Pin Replacement Register is not implemented on a card configured for the I/O Interface, the +RDY/-BSY function is continuously in the Ready condition. The following descriptions of the +RDY/-BSY signal apply equally to both the +RDY/-BSY signal of the Memory- Only Interface and to the +RDY/-BSY bit in the Pin Replacement Register of a card configured for the I/O Interface. See Section 4.14.3 for a description

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