Chapter 10 General Programmable Interface (GPIF)

10.1 Introduction

The General Programmable Interface (GPIF) is an *internal master* to the FX2's endpoint FIFOs. It replaces the external "glue" logic which might otherwise be required to build an interface between the FX2 and the outside world.

At the GPIF's core is a programmable state machine which generates up to six "control" and nine "address" outputs, and accepts six external and two internal "ready" inputs. Four user-defined *Waveform Descriptors* control the state machine; generally (but not necessarily), one is written for FIFO reads, one for FIFO writes, one for single-byte/word reads, and one for single-byte/word writes.

"Read" and "Write" are from the FX2's point of view. *"Read" waveforms transfer data from the outside world to the FX2; "Write" waveforms transfer data from the FX2 to the outside world.*

FX2 firmware can assign the FIFO-read and -write waveforms to any of the four FIFOs, and the GPIF will generate the proper strobes and handshake signals to the outside-world interface as data is transferred into or out of that FIFO.

As with external mastering (see *Chapter 9 "Slave FIFOs"*), the data bus between the FIFOs and the outside world can be either 8 or 16 bits wide.

The GPIF is not limited to simple handshaking interfaces between the FX2 and external ASICs or microprocessors; it's powerful enough to directly implement such protocols as ATAPI (PIO and UDMA), IEEE 1284 (EPP Parallel Port), Utopia, etc. An FX2 can, for instance, function as a single-chip interface between USB and an IDE hard disk drive or CompactFlash™ memory card.

This chapter provides an overview of GPIF, discusses external connections, and explains the operation of the GPIF engine. Figure 10-1 presents a block diagram illustrating GPIF's place in the FX2 system.

GPIF waveforms are generally created with the Cypress GPIFTool *utility, a Windows™-based application which is distributed with the Cypress EZ-USB FX2 Development Kit. Although this*

chapter will describe the structure of the Waveform Descriptors in some detail, knowledge of that structure is usually ***not*** *necessary. The* GPIFTool *simply hides the complexity of the Waveform Descriptors; it doesn't compromise the programmer's control over the GPIF in any way.*

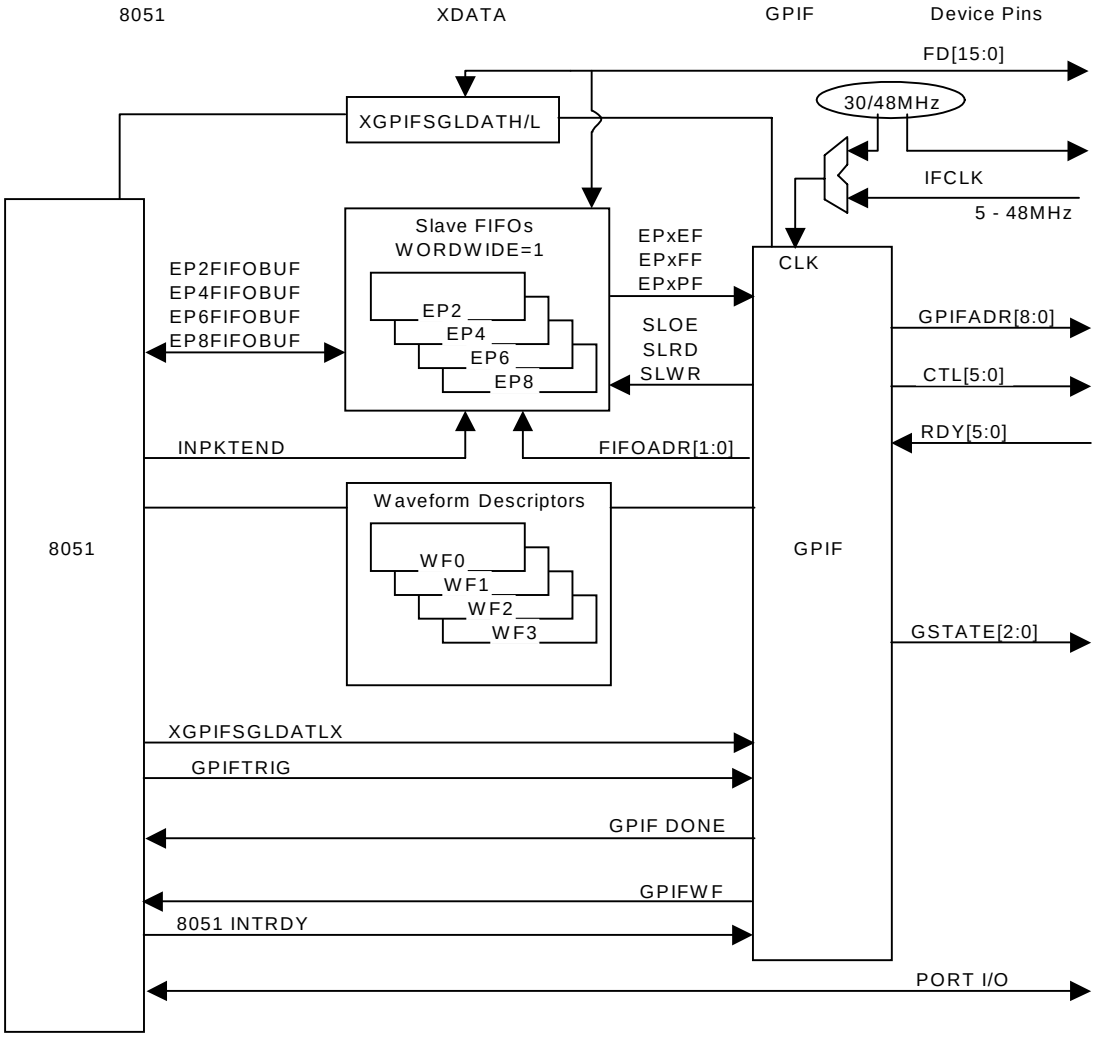


Figure 10-1. GPIF's Place in the FX2 System

Figure 10-2 shows an example of a simple GPIF transaction. For this transaction, the GPIF generates an address (GPIFADR[8:0]), drives the FIFO data bus (FD[15:0]), then waits for an externally-supplied handshake signal (RDY0) to go low, after which it pulls its CTL0 output low. When the RDY0 signal returns high, the GPIF brings its CTL0 output high, then floats the data bus.

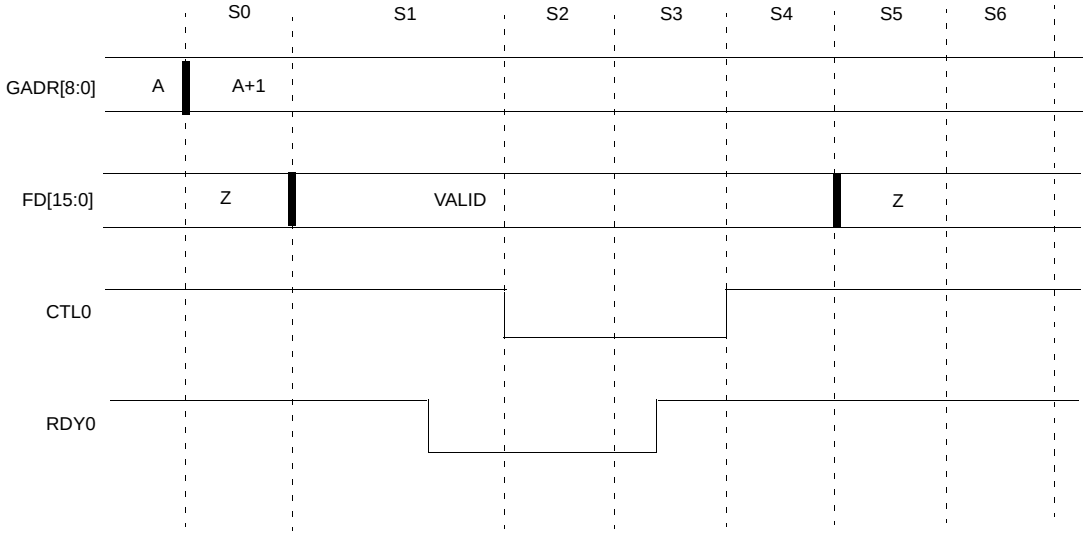


Figure 10-2. Example GPIF Waveform

10.1.1 Typical GPIF Interface

The GPIF allows the EZ-USB FX2 to connect directly to external peripherals such as ASICs, DSPs, or other digital logic that uses an 8- or 16-bit parallel interface.

The GPIF provides external pins that can operate as outputs (CTL[5:0]), inputs (RDY[5:0]), Data bus (FD[15:0]), and Address Lines (GPIFADR[8:0]).

A Waveform Descriptor in internal RAM describes the behavior of each of the GPIF signals. The Waveform Descriptor is loaded into the GPIF registers by the FX2 firmware during initialization, and it is then used throughout the execution of the code to perform transactions over the GPIF interface.

Figure 10-3 shows a block diagram of a typical interface between the EZ-USB FX2 and a peripheral function.

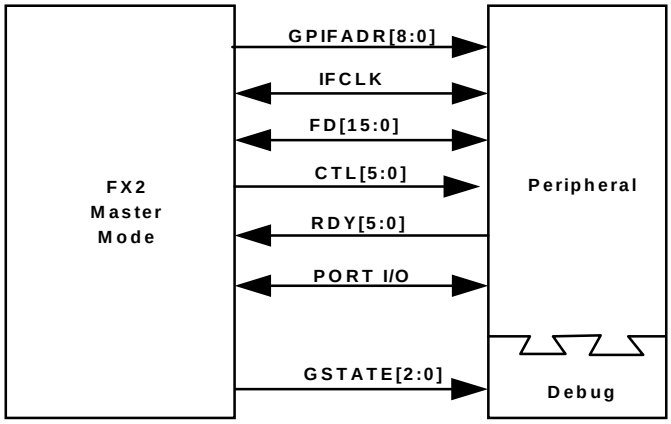


Figure 10-3. EZ-USB FX2 Interfacing to a Peripheral

The following sections detail the features available and steps needed to create an efficient GPIF design. This includes definition of the external GPIF connections and the internal register settings, along with FX2 firmware needed to execute data transactions over the interface.

10.2 Hardware

Table 10-1 lists the registers associated with the GPIF hardware; a detailed description of each register may be found in *Chapter 15, "Registers."*

Table 10-1. Registers Associated with GPIF Hardware

GPIFIDLECS	IFCONFIG
GPIFIDLECTL	FIFORESET
GPIFCTLCFG	EP*x*CFG
PORTCCFG	EP*x*FIFOCFG
PORTECFG	EP*x*AUTOINLENH/L
GPIFADRH/L	EP*x*FIFOPFH/L
GPIFTCB3:0	
GPIFWFSELECT	EPxTRIG
EP*x*GPIFFLGSEL	GPIFABORT
EP*x*GPIFPFSTOP	XGPIFSGLDATH/LX/LNOX
GPIFREADYCFG	GPIFSGLDATH/LX/NOX
GPIFREADYSTAT	GPIFTRIG

Note: The "*x*" in these register names represents 2, 4, 6, or 8; endpoints 0 and 1 are not associated with the GPIF.

10.2.1 The External GPIF Interface

The GPIF provides many general input and output signals with which external peripherals may be interfaced *gluelessly* to the FX2.

The GPIF interface signals are shown in Table 10-2.

Table 10-2. GPIF Pin Descriptions

PIN	IN/OUT	Description
CTL[5:0]	O / Hi-Z	Programmable control outputs
RDY[5:0]	I	Sampleable ready inputs
FD[15:0]	I / O / Hi-Z	Bidirectional FIFO data bus
GPIFADR[8:0]	O / Hi-Z	Address outputs
IFCLK	I / O	Interface clock
GSTATE[2:0]	O / Hi-Z	Current GPIF State number (for debug)

The Control Output pins (CTL[5:0]) are usually used as strobes (enable lines), read/write lines, etc.

The Ready Input pins (RDY[5:0]) are sampled by the GPIF and can force a transaction to wait (inserting wait states), continue, or repeat until they're in a particular state.

The GPIF Data Bus is a collection of the FD[15:0] pins.

- An 8-bit wide GPIF interface uses pins FD[7:0].
- A 16 bit-wide GPIF interface uses pins FD[15:0].

The GPIF Address lines (GPIFADR[8:0]) can generate an incrementing address as data is transferred. If higher-order address lines are needed, other non-GPIF I/O signals (i.e., general-purpose I/O pins) may be used.

The Interface Clock, IFCLK, can be configured to be either an input (default) or an output interface clock for synchronous interfaces to external logic.

The GSTATE[2:0] pins are outputs which show the current GPIF State number; they are typically used only when debugging GPIF waveforms.

10.2.2 Default GPIF Pins Configuration

The FX2 comes out of reset with its I/O pins configured in "Ports" mode, not "GPIF Master" mode. To configure the pins for GPIF mode, the IFCFG1:0 bits in the IFCONFIG register must be set to 10 (see Table 13-10, "IFCFG Selection of Port I/O Pin Functions" for details).

10.2.3 Six Control OUT Signals

The 100- and 128-pin FX2 packages bring out all six Control Output pins, CTL[5:0]. The 56-pin package brings out three of these signals, CTL[2:0]. CTLx waveform edges can be programmed to make transitions as often as once per IFCLK clock (once every 20.8 ns if IFCLK is running at 48MHz).

By default, these signals are driven high.

10.2.3.1 Control Output Modes

The GPIF Control pins (CTL[5:0]) have several output modes:

- CTL[3:0] can act as CMOS outputs (optionally tristatable) or open-drain outputs.
- CTL[5:4] can act as CMOS outputs or open-drain outputs.

  If CTL[3:0] are configured to be tristatable, CTL[5:4] are not available.

Table 10-3. CTL[5:0] Output Modes

TRICTL (GPIFCTLCFG.7)	GPIFCTLCFG[6:0]	CTL[3:0]	CTL[5:4]
0	0	CMOS, Not Tristatable	CMOS, Not Tristatable
0	1	Open-Drain	Open-Drain
1	X	CMOS, Tristatable	Not Available

10.2.4 Six Ready IN signals

The 100- and 128-pin FX2 packages bring out all six Ready inputs, RDY[5:0]. The 56-pin package brings out two of these signals, RDY[1:0].

The RDY inputs can be sampled synchronously or asynchronously. When the GPIF is in asynchronous mode (SAS=1), the RDY inputs are unavoidably delayed by a small amount (approximately 24 ns at 48 MHz IFCLK). In other words, when the GPIF “looks” at a RDY input, it actually “sees” the state of that input 24 ns ago.

10.2.5 Nine GPIF Address OUT signals

Nine GPIF address lines, GPIFADR[8:0], are available. If the GPIF address lines are configured as outputs, writing to the GPIFADRH:L registers drives these pins immediately. The GPIF engine can then increment them under control of the Waveform Descriptors. The GPIF address lines can be tristated by clearing the associated PORTxCFG bits and OEx bits to 0 (see Section 13.3.3, "Port C Alternate Functions" and Section 13.3.4, "Port E Alternate Functions").

10.2.6 Three GSTATE OUT signals

Three GPIF State lines, GSTATE[2:0], are available as an alternate configuration of PORTE[2:0]. These default to general-purpose inputs; setting GSTATE (IFCONFIG.2) to 1 selects the alternate configuration and overrides PORTECFG[2:0] bit settings.

The GSTATE[2:0] pins output the current GPIF State number; this feature is typically used only while debugging GPIF waveforms.

10.2.7 8/16-Bit Data Path, WORDWIDE = 1 (default) and WORDWIDE = 0

When the FX2 is configured for GPIF Master mode, PORTB is always configured as FD[7:0].

If *any* of the WORDWIDE bits (EPxFIFOCFG.0) are set to 1, PORTD is automatically configured as FD[15:8]. If all the WORDWIDE bits are cleared to 0, PORTD is available for general-purpose I/O.

10.2.8 Byte Order for 16-bit GPIF Transactions

Data is sent over USB in packets of 8-bit bytes, not 16-bit words. When the FIFO Data bus is 16 bits wide, the first byte in every pair sent over USB is transferred over FD[7:0] and the second byte is transferred over FD[15:8].

10.2.9 Interface Clock (IFCLK)

The GPIF interface can be clocked from either an internal or an external source. The FX2's internal clock source can be configured to run at either 30 or 48 MHz, and it can optionally be output on the IFCLK pin. If the FX2 is configured to use an external clock source, the IFCLK pin can be driven at any frequency between 5 MHz and 48 MHz. On power-on reset, the FX2 defaults to the internal source at 48 MHz, normal polarity, with the IFCLK output disabled. See Figur e10-4.

IFCONFIG.7 selects between internal and external sources: 0 = external, 1 = internal.

IFCONFIG.6 selects between the 30- and 48-MHz internal clock: 0 = 30 MHz, 1 = 48 MHz. This bit has no effect when IFCONFIG.7 = 0.

IFCONFIG.5 is the output enable for the internal clock source: 0 = disable, 1 = enable. This bit has no effect when IFCONFIG.7 = 0.

IFCONFIG.4 inverts the polarity of the interface clock (whether it's internally or externally sourced): 0 = normal, 1 = inverted. IFCLK inversion can make it easier to interface the FX2 with certain external circuitry; Figure 10-5, for example, demonstrates the use of IFCLK inversion in order to ensure a long-enough setup time for reading peripheral signals.

When IFCLK is configured as an input, the minimum external frequency that can be applied to it is 5 MHz.

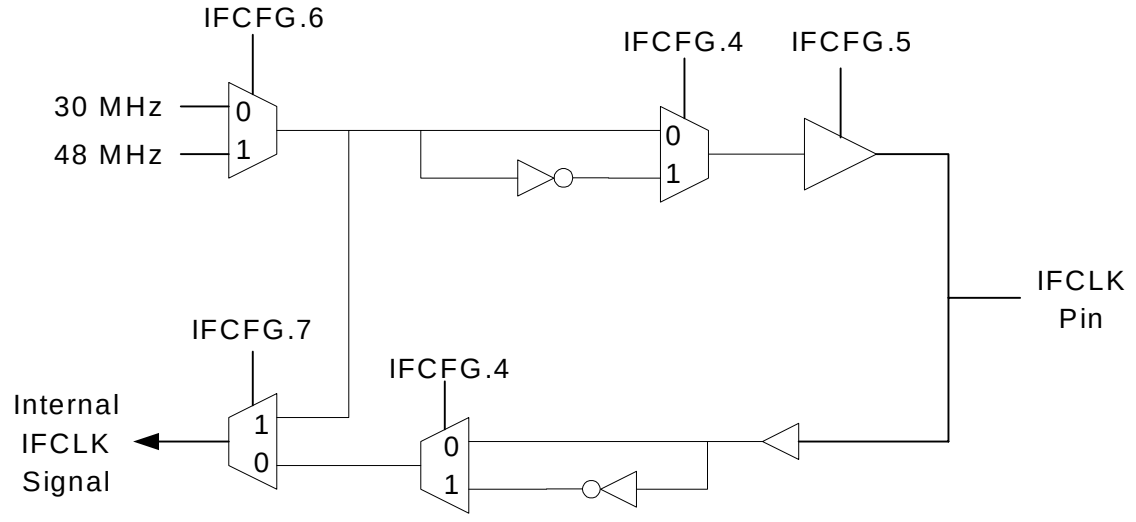


Figure 10-4. IFCLK Configuration

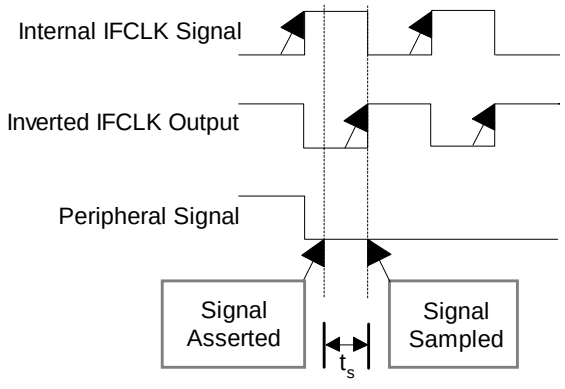


Figure 10-5. Satisfying Setup Timing by Inverting the IFCLK Output

10.2.10 Connecting GPIF Signal Pins to Hardware

The first step in creating the interface between the FX2's GPIF and an external peripheral is to define the hardware interconnects.

1. **Choose IFCLK settings**. Decide whether to use an asynchronous or synchronous interface. If synchronous, choose either the internal or external interface clock. If internal, choose either 30 or 48 MHz; if external, ensure that the frequency of the external clock is in the range 5-48 MHz.
2. **Determine the proper FIFO Data Bus size.** If the data bus for the interface is 8 bits wide, use the FD[7:0] pins and set WORDWIDE=0. If the data bus for the interface is 16 bits wide, use FD[15:0] and set WORDWIDE=1.
3. **Assign the CTLx signals to the interface**. Make a list of all interface signals to be driven from the GPIF to the peripheral, and assign them to the CTL[5:0] inputs. If there are more output signals than available CTL outputs, non-GPIF I/O signals must be driven manually by FX2 firmware. In this case, the CTLx outputs should be assigned only to signals that must be driven as part of a data transaction.
4. **Assign the RDYn signals to the interface.** Make a list of all interface signals to be driven from the peripheral to the GPIF, and assign them to the RDY[5:0] inputs. If there are more input signals than available RDY inputs, non-GPIF I/O signals must be sampled manually by FX2 firmware. In this case, the RDYn inputs should be used only for signals that must be sampled as part of a data transaction.
5. **Determine the proper GPIF Address connections**. If the interface uses an Address Bus, use the GPIFADR[8:0] signals for the least significant bits, and other non-GPIF I/O signals for the most significant bits. If the address pins are not needed (as when, for instance, the peripheral is a FIFO) they may be left unconnected.

10.2.11 Example GPIF Hardware Interconnect

The following example illustrates the hardware connections that can be made for a standard interface to a 27C256 EPROM.

Table 10-4. Example GPIF Hardware Interconnect

Step	Result	Connection Made
1. Choose IFCLK settings.	Internal IFCLK, 48MHz, Async, GPIF.	No connection.
2. Determine proper FIFO Data Bus size.	8 bits from the EPROM.	FD[7:0] to D[7:0]. Firmware writes WORDWIDE=0.
3. Assign CTLx signals to the interface.	$\overline{CS}$ and $\overline{OE}$ are inputs to the EPROM.	CTL0 to $\overline{CS}$. CTL1 to $\overline{OE}$.
4. Assign RDYn signals to the interface.	27C256 EPROM has no output ready/wait signals.	No connection.
5. Determine the proper GPIFADR connections.	16 bits of address.	GPIFADR[8:0] to A[8:0] and other I/O pins to A[15:9].

The process is the same for larger, more-complicated interfaces.

10.3 Programming the GPIF Waveforms

Each GPIF Waveform Descriptor can define up to 7 States. In each State, the GPIF can be programmed to:

- Drive (high or low) or float the CTL outputs
- Sample or drive the FIFO Data bus
- Increment the value on the GPIF Address bus
- Increment the pointer into the current FIFO
- Trigger a GPIFWF (GPIF Waveform) interrupt

Additionally, each State may either sample any two of the following:

- The RDYx input pins
- A FIFO flag
- The INTRDY (internal RDY) flag
- The Transaction-Count-Expired flag

then AND, OR, or XOR the two terms and branch on the result to any State

or:

- Delay a specified number [1-256] of IFCLK cycles

States which sample and branch are called “Decision Points” (DPs); States which don’t are called “Non-Decision Points” (NDPs).

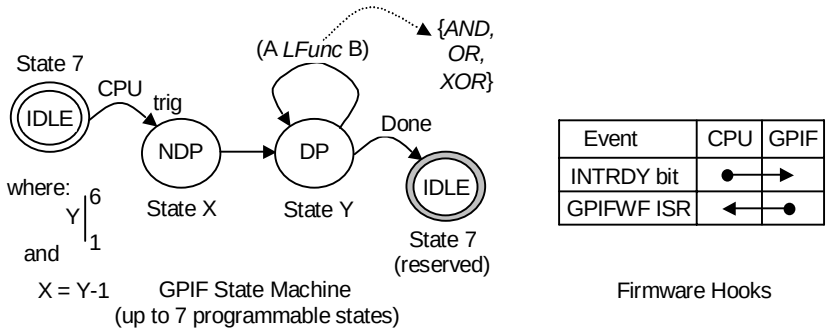


Figure 10-6. GPIF State Machine Overview

10.3.1 The GPIF Registers

Two blocks of registers control the GPIF state machine:

- **GPIF Configuration Registers —** These registers configure the general settings and report the status of the interface. Refer to *Chapter 15, "Registers,"* and the remainder of this chapter for details.
- **Waveform Registers —** These registers are loaded with the Waveform Descriptors that configure the GPIF state machine; there are a total of 128 bytes located at addresses 0xE400 to 0xE47F. *It is strongly recommended that the* GPIFTool *utility be used to create Waveform Descriptors.*

GPIF transactions cannot be initiated until the Configuration Registers and Waveform Registers are loaded by FX2 firmware.

Access to the waveform registers is only allowed while the FX2 is in GPIF mode (i.e., IFCFG1:0 = 10). The waveform registers may only be written while the GPIF engine is halted (i.e., DONE = 1).

If it's desired to dynamically reconfigure Waveform Descriptors, this may be accomplished by writing just the bytes which change; it's not necessary to reload the entire set of Waveform Descriptors in order to modify only a few bytes.

10.3.2 Programming GPIF Waveforms

The "programs" for GPIF waveforms are the *Waveform Descriptors*, which are stored in the Waveform Registers by FX2 firmware.

The FX2 can hold up to four Waveform Descriptors, each of which can be used for one of four types of transfers: Single Write, Single Read, FIFO Write, or FIFO Read. By default, one Waveform Descriptor is assigned to each transfer type, but it's not necessary to retain that configuration; all four Waveform Descriptors could, for instance, be configured for FIFO Write usage (see the GPIFWFSELECT register in *Chapter 15 "Registers"*).

Each Waveform Descriptor consists of up to seven 32-bit *State Instructions* that program key transition points for GPIF interface signals. There's a one-to-one correspondence between the State Instructions and the GPIF state-machine States. Among other things, each State Instruction defines the state of the CTLx outputs, the state of FD[15:0], the use of the RDYn inputs, and the behavior of GPIFADR[8:0].

Transitions from one State to another always happen on a rising edge of the IFCLK, but the GPIF may remain in one State for many IFCLK cycles.

10.3.2.1 The GPIF IDLE State

A Waveform consists of *up to* seven programmable States, numbered S0 to S6, and one special *Idle State,* S7. **A Waveform terminates when the GPIF program branches to its Idle State.**

To complete a GPIF transaction, the GPIF program must branch to the IDLE State, *regardless of the State that the GPIF program is currently executing*. For example, a GPIF Waveform might be defined by a program which contained only 2 programmed States, S0 and S1. The GPIF program would branch from S1 (or S0) to S7 when it wished to terminate.

The state of the GPIF signals during the Idle State is determined by the contents of the GPIFIDLECS and GPIFIDLECTL registers.

Once a waveform is triggered, another waveform may not be started until the first one terminates. Termination of a waveform is signaled through the DONE bit (GPIFIDLECS.7 or GPIFTRIG.7) or, optionally, through the GPIFDONE interrupt.

- If DONE = 0, the GPIF is *busy* generating a Waveform.
- If DONE = 1, the GPIF is *done* (GPIF is in the Idle State) and ready for firmware to start the next GPIF transaction.

Important: *With one exception (writing to the GPIFABORT register in order to force the current waveform to terminate) it is illegal to write to any of the GPIF-related registers (including the Waveform Registers) while the GPIF is busy. Doing so will cause indeterminate behavior likely to result in data corruption.*

10.3.2.1.1 GPIF Data Bus During IDLE

During the Idle State, the GPIF Data Bus (FD[15:0]) can be either driven or tristated, depending on the setting of the IDLEDRV bit (GPIFIDLECS.0):

- If IDLEDRV = 0, the GPIF Data Bus is tristated during the Idle State.
- If IDLEDRV = 1, the GPIF Data Bus is actively driven during the Idle State, to the value last placed on the bus by a GPIF Waveform.

10.3.2.1.2 CTL Outputs During IDLE

During the IDLE State, the state of CTL[5:0] depends on the following register bits:

- TRICTL (GPIFCTLCFG.7), as described in Section 10.2.3.1, "Control Output Modes".
- GPIFCTLCFG[5:0]
- GPIFIDLECTL[5:0].

The combination of these bits defines CTL5:0 during IDLE as follows:

- If TRICTL is 0, GPIFIDLECTL[5:0] directly represent the output states of CTL5:0 during the IDLE State. The GPIFCTLCFG[5:0] bits determine whether the CTL5:0 outputs are CMOS or open-drain: If GPIFCTLCFG.x = 0, CTLx is CMOS; if GPIFCTLCFG.x = 1, CTLx is open-drain.

- If TRICTL is 1, GPIFIDLECTL[7:4] are the output enables for the CTL[3:0] signals, and GPIFIDLECTL[3:0] are the output values for CTL[3:0]. CTL4 and CTL5 are unavailable in this mode.

Table 10-5 illustrates this relationship.

Table 10-5. Control Outputs (CTLn) During the IDLE State

TRICTL	Control Output	Output State	Output Enable
0	CTL0	GPIFIDLECTL.0	N/A (CTL Outputs are always enabled when TRICTL = 0)
	CTL1	GPIFIDLECTL.1	
	CTL2	GPIFIDLECTL.2	
	CTL3	GPIFIDLECTL.3	
	CTL4	GPIFIDLECTL.4	
	CTL5	GPIFIDLECTL.5	
1	CTL0	GPIFIDLECTL.0	GPIFIDLECTL.4
	CTL1	GPIFIDLECTL.1	GPIFIDLECTL.5
	CTL2	GPIFIDLECTL.2	GPIFIDLECTL.6
	CTL3	GPIFIDLECTL.3	GPIFIDLECTL.7
	CTL4	N/A (CTL4 and CTL5 are not available when TRICTL = 1)	
	CTL5		

10.3.2.2 Defining States

Each Waveform is made up of a number of States, each of which is defined by a 32-bit State Instruction. Each State can be one of two basic types: a *Non-Decision Point* (NDP) or a *Decision Point* (DP).

For “write” waveforms, the data bus is either driven or tristated during each State. For “read” waveforms, the data bus is either sampled/stored or not sampled during each State.

10.3.2.2.1 Non-Decision Point (NDP) States

For NDP States, the control outputs (CTLx) are defined by the GPIF instruction to be either 1, 0, or tristated during the entire State. NDP States have a programmable fixed duration in units of IFCLK cycles.

Figure 10-7 illustrates the basic concept of NDP States. A write waveform is shown, and for simplicity all the States are shown with equal spacing. Although there are a total of six programmable CTL outputs, only one (CTL0) is shown in Figure 10-7.

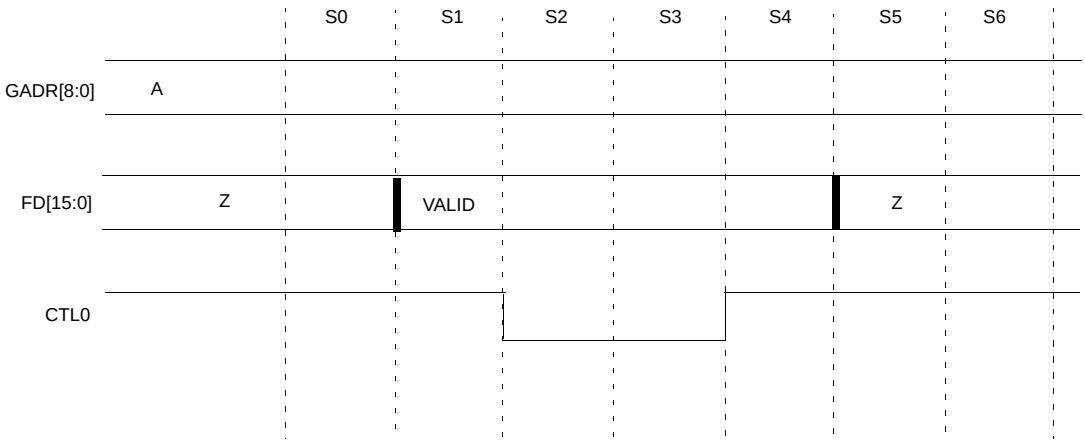


Figure 10-7. Non-Decision Point (NDP) States

Referring to Figure 10-7:

In State 0:

- FD[7:0] is programmed to be tristated.
- CTL0 is programmed to be driven to a logic 1.

In State 1:

- FD[7:0] is programmed to be driven.
- CTL0 is still programmed to be driven to a logic 1.

In State 2:

- FD[7:0] is programmed to be driven.
- CTL0 is programmed to be driven to a logic 0.

In State 3:

- FD[7:0] is programmed to be driven.
- CTL0 is still programmed to be driven to a logic 0.

In State 4:

- FD[7:0] is programmed to be driven.
- CTL0 is programmed to be driven to a logic 1.

In State 5:

- FD[7:0] is programmed to be tristated.
- CTL0 is still programmed to be driven to a logic 1.

In State 6:

- FD[7:0] is programmed to be tristated.
- CTL0 is still programmed to be driven to a logic 1.

Since all States in this example are coded as NDPs, the GPIF automatically branches from the last State (S6) to the Idle State (S7). This is the State in which the GPIF waits until the next GPIF waveform is triggered by the firmware.

States 2 and 3 in the example are identical, as are States 5 and 6. In a real application, these would probably be combined (there's no need to duplicate a State in order to "stretch" it, since each NDP State can be assigned a duration in terms of IFCLK cycles). If fewer than 7 States were defined for this waveform, the Idle State wouldn't automatically be entered after the last programmed State; that last programmed State's State Instruction would have to include an explicit branch to the Idle State.

10.3.2.2.2 Decision Point (DP) States

Any State can be designated as a Decision Point (DP). A DP allows the GPIF engine to sample two signals — each of the "two" can be the same signal, if desired — perform a boolean operation on the sampled values, then branch to other States (or loop back on itself, remaining in the current State) based on the result.

If a State Instruction includes a control task (advance the FIFO pointer, increment the GPIFADR address, etc.), that task is always executed once upon entering the State, regardless of whether the State is a DP or NDP. If the State is a DP that loops back on itself, however, it can be programmed to re-execute the control task on every loop.

With a Decision Point, the GPIF can perform simple tasks (wait until a RDY line is low before continuing to the next State, for instance). Decision point States can also perform more-complex tasks by branching to one State if the operation on the sampled signals results in a logic 1, or to a different State if it results in a logic 0.

In each State Instruction, the two signals to sample can be selected from any of the following:

- the six external RDY signals (RDY0-RDY5)
- one of the current FIFO's flags (PF, EF, FF)
- the INTRDY bit in the READY register
- a "Transaction Count Expired" signal (which replaces RDY5)

The State Instruction also specifies a logic function (AND, OR, or XOR) to be applied to the two selected signals. If it's desired to act on the state of only one signal, the usual procedure is to select the same signal twice and specify the logic function as AND.

The State Instruction also specifies which State to branch to if the result of the logical expression is 0, and which State to branch to if the result of the logical expression is 1.

Below is an example waveform created using one Decision Point State (State 1); Non-Decision Point States are used for the rest of the waveform.

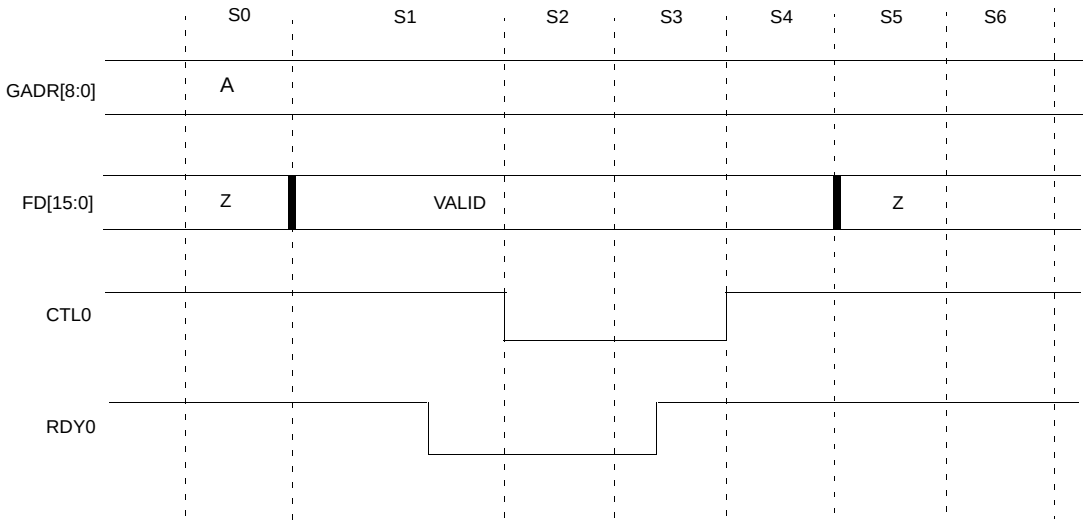


Figure 10-8. One Decision Point: Wait States Inserted Until RDY0 Goes Low

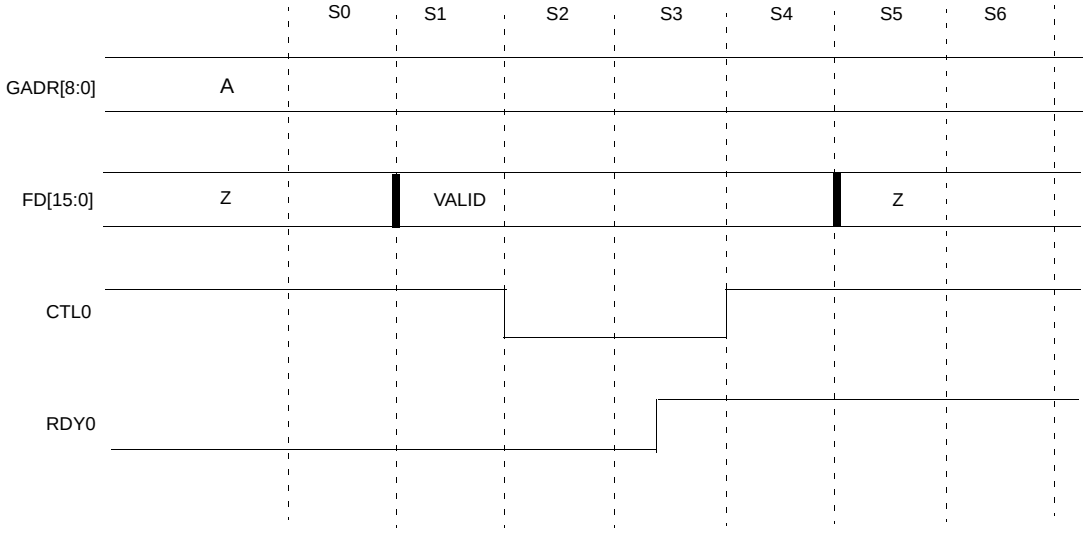


Figure 10-9. One Decision Point: No Wait States Inserted: RDY0 is Already Low at Decision Point I1

In Figure 10-8 and Figure 10-9, there is a single Decision Point defined as State 1. In this example, the input ready signal is assumed to be connected to RDY0, and the State Instruction for S1 is configured to branch to State 2 if RDY0 is a logic 0 or to branch to State 1 (i.e., loop indefinitely) if RDY0 is a logic 1.

In Figure 10-8, the GPIF remains in S1 until the RDY0 signal goes low, then branches to S2. Figure 10-9 illustrates the GPIF behavior when the RDY0 signal is *already* low when S1 is entered: The GPIF branches to S2.

*Although it appears in Figure 10-8 that the GPIF branches **immediately** from State 0 to State 2, this isn't exactly true. Even if RDY0 is already low before the GPIF enters State 1, the GPIF spends one IFCLK cycle in State 1.*

10.3.3 Re-Executing a Task Within a DP State

In the simple DP examples shown earlier in this chapter, a control task (e.g., output a word on FD[15:0] and increment GPIFADR[8:0]) executes only once at the start of a DP State, then the GPIF waits, sampling a RDYx input repeatedly until that input "tells" the GPIF to branch to the next State.

The GPIF also has the capability to re-execute the control task every time the RDYx input is sampled; this feature can be used to burst a large amount of data without passing through the Idle State.

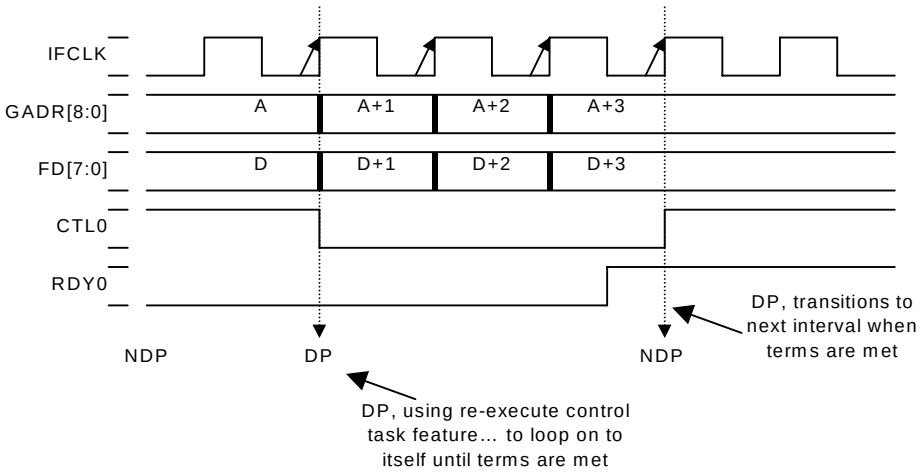


Figure 10-10. Re-Executing a Task within a DP State

State	0	1	2	3	4	5	6	7
AddrMode	Same Val	Inc Val	Same Val	Same Val	Same Val	Same Val	Same Val	
DataMode	Activate	Activate	NO Data	NO Data	NO Data	NO Data	NO Data	
NextData	SameData	NextData	SameData	SameData	SameData	SameData	SameData	
Int Trig	No Int	No Int	No Int	No Int	No Int	No Int	No Int	
IF/Wait	Wait 4	IF	Wait 1	Wait 1	Wait 1	Wait 1	Wait 1	
Term A		RDY0						
LFUNC		AND						
Term B		RDY0						
Branch1		Then 2						
Branch0		Else 1						
Re-execute		Yes						
CTL0	1	0	1	1	1	1	1	1
CTL1	1	1	1	1	1	1	1	1
CTL2	1	1	1	1	1	1	1	1
CTL3	1	1	1	1	1	1	1	1
CLT4	1	1	1	1	1	1	1	1
CTL5	1	1	1	1	1	1	1	1

Figure 10-11. GPIFTool Setup for the Waveform of Figure 10-10

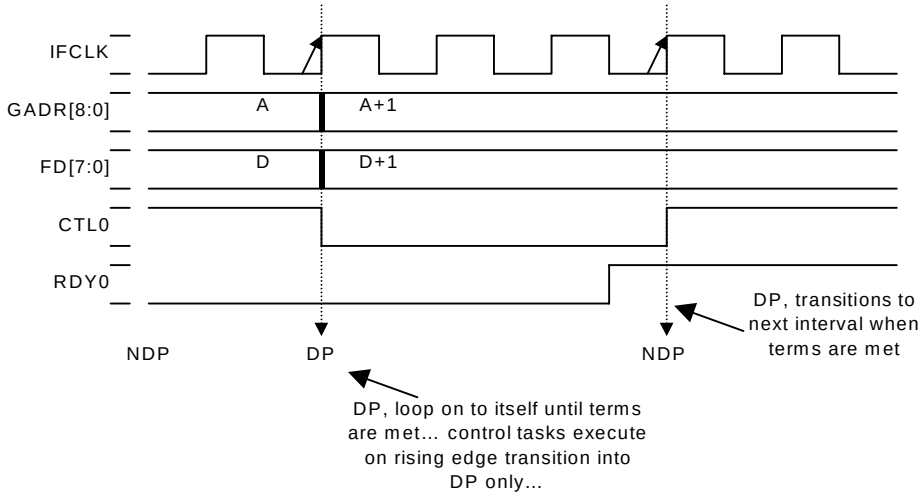


Figure 10-12. A DP State Which Does NOT Re-Execute the Task

State	0	1	2	3	4	5	6	7
AddrMode	Same Val	Inc Val	Same Val	Same Val	Same Val	Same Val	Same Val	
DataMode	Activate	Activate	NO Data	NO Data	NO Data	NO Data	NO Data	
NextData	SameData	NextData	SameData	SameData	SameData	SameData	SameData	
Int Trig	No Int	No Int	No Int	No Int	No Int	No Int	No Int	
IF/Wait	Wait 4	IF	Wait 1	Wait 1	Wait 1	Wait 1	Wait 1	
Term A		RDY0						
LFUNC		AND						
Term B		RDY0						
Branch1		Then 2						
Branch0		Else 1						
Re-execute		No						
CTL0	1	0	1	1	1	1	1	1
CTL1	1	1	1	1	1	1	1	1
CTL2	1	1	1	1	1	1	1	1
CTL3	1	1	1	1	1	1	1	1
CLT4	1	1	1	1	1	1	1	1
CTL5	1	1	1	1	1	1	1	1

Figure 10-13. GPIFTool Setup for the Waveform of Figure 10-12

10.3.4 State Instructions

Each State's characteristics are defined by a 4-byte State Instruction. The four bytes are named *LENGTH / BRANCH*, *OPCODE*, *LOGIC FUNCTION*, and *OUTPUT*.

Note that the State Instructions are interpreted differently for Decision Points (DP = 1) and Non-Decision Points (DP = 0).

Non-Decision Point State Instruction (DP = 0)

LENGTH / BRANCH

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Number of IFCLK cycles to stay in this State (0 = 256 cycles)							

OPCODE

7	6	5	4	3	2	1	0
x	x	SGL	GINT	INCAD	NEXT/ SGLCRC	DATA	DP = 0

LOGIC FUNCTION

7	6	5	4	3	2	1	0
Not Used							

OUTPUT (if TRICTL Bit = 1)

7	6	5	4	3	2	1	0
OE3	OE2	OE1	OE0	CTL3	CTL2	CTL1	CTL0

OUTPUT (if TRICTL Bit = 0)

7	6	5	4	3	2	1	0
x	x	CTL5	CTL4	CTL3	CTL2	CTL1	CTL0

Decision Point State Instruction (DP = 1)

LENGTH / BRANCH

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Re-Execute	x	BRANCHON1			BRANCHON1		

OPCODE

7	6	5	4	3	2	1	0
x	x	SGL	GINT	INCAD	NEXT/ SGLCRC	DATA	DP = 1

LOGIC FUNCTION

7	6	5	4	3	2	1	0
LFUNC		TERMA			TERMB		

OUTPUT (if TRICTL Bit = 1)

7	6	5	4	3	2	1	0
OE3	OE2	OE1	OE0	CTL3	CTL2	CTL1	CTL0

OUTPUT (if TRICTL Bit = 0)

7	6	5	4	3	2	1	0
x	x	CTL5	CTL4	CTL3	CTL2	CTL1	CTL0

LENGTH / BRANCH Register: This register's interpretation depends on the DP bit:

- For DP = 0 (Non-Decision Point), this is a LENGTH field; it holds the fixed duration of this State in IFCLK cycles. A value of 0 is interpreted as 256 IFCLK cycles.
- For DP = 1 (Decision Point), this is a BRANCH field; it specifies the State to which the GPIF will branch:

  BRANCHON1: Specifies the State to which the GPIF will branch if the logic expression evaluates to 1.

  BRANCHON0: Specifies the State to which the GPIF will branch if the logic expression evaluates to 0.

OPCODE Register: This register sets a number of State characteristics.

SGL Bit: has no effect in a Single-Read or Single-Write waveform. In a FIFO waveform, it specifies whether a single-data transaction should occur (from/to the SGLDATAH:L or UDMA_CRCH:L registers), even in a FIFO-Write or FIFO-Read transaction. See also “NEXT/SGLCRC”, below.

1 = Use SGLDATAH:L or UDMA_CRCH:L.
0 = Use the FIFO.

GINT Bit: specifies whether to generate a GPIFWF interrupt during this State.

1 = Generate GPIFWF interrupt (on INT4) when this State is reached.
0 = Do not generate interrupt.

INCAD Bit: specifies whether to increment the GPIF Address lines GPIFADR[8:0].

1 = Increment the GPIFADR[8:0] bus at the beginning of this State.
0 = Do not increment the GPIFADR[8:0] signals.

NEXT/SGLCRC Bit:

If SGL = 0, specifies whether the FIFO should be advanced at the start of this State.

1 = Move the next data in the OUT FIFO to the top.
0 = Do not advance the FIFO.
The NEXT bit has no effect when the waveform is applied to an IN FIFO.

If SGL = 1, specifies whether data should be transferred to/from SGLDATAH:L or UDMA_CRCH:L. See also “SGL Bit”, above.

1 = Use UDMA_CRCH:L.
0 = Use SGLDATAH:L.

DATA Bit: specifies whether the FIFO Data bus is to be driven, tristated, or sampled.

During a write:
1 = Drive the FIFO Data bus with the output data.
0 = Tristate (don’t drive the bus).

During a read:
1 = Sample the FIFO Data bus and store the data.
0 = Don’t sample the data bus.

DP Bit: indicates whether the State is a DP or NDP:

1 = Decision Point.
0 = Non-Decision Point.

LOGIC FUNCTION Register: This register is used only in DP State Instructions. It specifies the inputs (TERMA and TERMB) and the Logic Function (LFUNC) to apply to those inputs. The result of the logic function determines the State to which the GPIF will branch (see also “LENGTH / BRANCH Register”, above).

TERMA and **TERMB bits**:

= 000: RDY0
= 001: RDY1
= 010: RDY2
= 011: RDY3
= 100: RDY4
= 101: RDY5 (or Transaction-Count Expiration, if GPIFREADYCFG.5 = 1)
= 110: FIFO flag (PF, EF, or FF), preselected via EPxGPIFFLGSEL
= 111: INTRDY (Bit 7 of the GPIFREADYCFG register)

LFUNC bits:

= 00: A AND B
= 01: A OR B
= 10: $\overline{A}$ XOR B
= 11: $\overline{A}$ AND B

The TERMA and TERMB inputs are sampled at each rising edge of IFCLK. The logic function is applied, then the branch is taken on the next rising edge.

This register is meaningful only for DP Instructions; when the DP bit of the OPCODE register is cleared to 0, the contents of this register are ignored.

OUTPUT Register: This register controls the state of the 6 Control outputs (CTL5:0) during the entire State defined by this State Instruction.

OEn Bit: If TRICTL = 1, specifies whether the corresponding CTLx output signal is tristated.

1 = Drive CTLx
0 = Tristate CTLx

CTLn Bit: specifies the state to set each CTLx signal to during this entire State.

1 = High level

If the CTLx bit in the GPIFCTLCFG register is set to 1, the output driver will be an open-drain.

If the CTLx bit in the GPIFCTLCFG register is set to 0, the output driver will be driven to CMOS levels.

0 = Low level

10.3.4.1 Structure of the Waveform Descriptors

Up to four different Waveforms can be defined. Each Waveform Descriptor comprises up to 7 State Instructions which are loaded into the Waveform Registers as defined in this section.

Table 10-6. Waveform Descriptor Addresses

Waveform Descriptor	Base XDATA Address
0	0xE400
1	0xE420
2	0xE440
3	0xE460

Within each Waveform Descriptor, the State Instructions are packed as described in *Table 10-7, "Waveform Descriptor 0 Structure"*. Waveform Descriptor 0 is shown as an example. The other Waveform Descriptors follow exactly the same structure but at higher XDATA addresses.

Table 10-7. Waveform Descriptor 0 Structure

XDATA Address	Contents
0xE400	LENGTH / BRANCH [0] (LENGTH / BRANCH field of State 0 of Waveform Program 0)
0xE401	LENGTH / BRANCH [1] (LENGTH / BRANCH field of State 1 of Waveform Program 0)
0xE402	LENGTH / BRANCH [2] (LENGTH / BRANCH field of State 2 of Waveform Program 0)
0xE403	LENGTH / BRANCH [3] (LENGTH / BRANCH field of State 3 of Waveform Program 0)
0xE404	LENGTH / BRANCH [4] (LENGTH / BRANCH field of State 4 of Waveform Program 0)
0xE405	LENGTH / BRANCH [5] (LENGTH / BRANCH field of State 5 of Waveform Program 0)
0xE406	LENGTH / BRANCH [6] (LENGTH / BRANCH field of State 6 of Waveform Program 0)
0xE407	Reserved
0xE408	OPCODE[0] (OPCODE field of State 0 of Waveform Program 0)
0xE409	OPCODE[1] (OPCODE field of State 1 of Waveform Program 0)
0xE40A	OPCODE[2] (OPCODE field of State 2 of Waveform Program 0)
0xE40B	OPCODE[3] (OPCODE field of State 3 of Waveform Program 0)
0xE40C	OPCODE[4] (OPCODE field of State 4 of Waveform Program 0)
0xE40D	OPCODE[5] (OPCODE field of State 5 of Waveform Program 0)
0xE40E	OPCODE[6] (OPCODE field of State 6 of Waveform Program 0)
0xE40F	Reserved
0xE410	OUTPUT[0] (OUTPUT field of State 0 of Waveform Program 0)
0xE411	OUTPUT[1] (OUTPUT field of State 1 of Waveform Program 0)
0xE412	OUTPUT[2] (OUTPUT field of State 2 of Waveform Program 0)
0xE413	OUTPUT[3] (OUTPUT field of State 3 of Waveform Program 0)
0xE414	OUTPUT[4] (OUTPUT field of State 4 of Waveform Program 0)
0xE415	OUTPUT[5] (OUTPUT field of State 5 of Waveform Program 0)
0xE416	OUTPUT[6] (OUTPUT field of State 6 of Waveform Program 0)
0xE417	Reserved
0xE418	LOGIC FUNCTION[0] (LOGIC FUNCTION field of State 0 of Waveform Program 0)
0xE419	LOGIC FUNCTION[1] (LOGIC FUNCTION field of State 1 of Waveform Program 0)

Table 10-7. Waveform Descriptor 0 Structure (Continued)

0xE41A	LOGIC FUNCTION[2] (LOGIC FUNCTION field of State 2 of Waveform Program 0)
0xE41B	LOGIC FUNCTION[3] (LOGIC FUNCTION field of State 3 of Waveform Program 0)
0xE41C	LOGIC FUNCTION[4] (LOGIC FUNCTION field of State 4 of Waveform Program 0)
0xE41D	LOGIC FUNCTION[5] (LOGIC FUNCTION field of State 5 of Waveform Program 0)
0xE41E	LOGIC FUNCTION[6] (LOGIC FUNCTION field of State 6 of Waveform Program 0)
0xE41F	Reserved

10.4 Firmware

Table 10-8. Registers Associated with GPIF Firmware

GPIFTRIG (SFR)
GPIFSGLDATH (SFR)
GPIFSGLDATLX (SFR)
GPIFSGLDATLNOX (SFR)
EPxGPIFTRIG
XGPIFSGLDATH
XGPIFSGLDATLX
XGPIFSGLDATLNOX
GPIFABORT
GPIFIE
GPIFIRQ
GPIFTCB3
GPIFTCB2
GPIFTCB1
GPIFTC0

EPxBCH/L
EPxFIFOBCH/L
EPxFIFOBUF
INPKTEND

EPxCFG
EPxFIFOCFG
EPxAUTOINLENH/L
EPxFIFOPFH/L
EP2468STAT(SFR)
EP24FIFOFLGS(SFR)
EP68FIFOFLGS(SFR)
EPxCS
EPxFIFOFLGS

EPxFIFOIE
EPxFIFOIRQ
INT2IVEC
INT4IVEC
INTSETUP
IE (SFR)
IP (SFR)
INT2CLR(SFR)
INT4CLR(SFR)
EIE (SFR)
EXIF (SFR)

The "*x*" in these register names represents 2, 4, 6, or 8; endpoints 0 and 1 are not associated with the Slave FIFOs.

The *GPIFTool* utility, distributed with the Cypress EZ-USB FX2 Development Kit, generates C code which may be linked with the rest of an application's source code. The *GPIFTool* output includes the following basic GPIF framework and functions:

```
TD_Init():
    … … … … …
    GpifInit();  // Configures GPIF from GPIFTool generated waveform data

    // TODO: configure other endpoints, etc. here

    // TODO: arm OUT buffer(s) here

    // setup INT4 as internal source for GPIF interrupts
    // using INT4CLR (SFR), automatically enabled
    //INTSETUP |= 0x03;  //Enable INT4 Autovectoring
    // SYNCDELAY;
    //GPIFIE = 0x03;  // Enable GPIFDONE and GPIFWF interrupt(s)
    // SYNCDELAY;
    //EIE |= 0x04;  // Enable INT4 ISR, EIE.2(EIEX4)=1

    // TODO: configure GPIF interrupt(s) to meet your needs here
       … … … … …

void GpifInit( void )
{
  BYTE i;

  // Registers which require a synchronization delay, see section 15.14
  // FIFORESET        FIFOPINPOLAR
  // INPKTEND         OUTPKTEND
  // EPxBCH:L         REVCTL
  // GPIFTCB3         GPIFTCB2
  // GPIFTCB1         GPIFTCB0
  // EPxFIFOPFH:L     EPxAUTOINLENH:L
  // EPxFIFOCFG       EPxGPIFFLGSEL
  // PINFLAGSxx       EPxFIFOIRQ
  // EPxFIFOIE        GPIFIRQ
  // GPIFIE           GPIFADRH:L
  // UDMACRCH:L       EPxGPIFTRIG
  // GPIFTRIG

  // Note: The pre-REVE EPxGPIFTCH/L register are affected, as well...
  //      ...these have been replaced by GPIFTC[B3:B0] registers

  // 8051 doesn't have access to waveform memories 'til
  // the part is in GPIF mode.

  IFCONFIG = 0xCE;
  // IFCLKSRC=1   , FIFOs executes on internal clk source
  // xMHz=1       , 48MHz internal clk rate
  // IFCLKOE=0    , Don't drive IFCLK pin signal at 48MHz
  // IFCLKPOL=0   , Don't invert IFCLK pin signal from internal clk
  // ASYNC=1      , master samples asynchronous
  // GSTATE=1     , Drive GPIF states out on PORTE[2:0], debug WF
  // IFCFG[1:0]=10, FX2 in GPIF master mode

  GPIFABORT = 0xFF;  // abort any waveforms pending

  GPIFREADYCFG = InitData[ 0 ];
  GPIFCTLCFG = InitData[ 1 ];
  GPIFIDLECS = InitData[ 2 ];
  GPIFIDLECTL = InitData[ 3 ];
```

```
  GPIFWFSELECT = InitData[ 5 ];
  GPIFREADYSTAT = InitData[ 6 ];

  // use dual autopointer feature...
  AUTOPTRSETUP = 0x07;          // inc both pointers,
                                // ...warning: this introduces pdata hole(s)
                                // ...at E67B (XAUTODAT1) and E67C (XAUTODAT2)

  // source
  APTR1H = MSB( &WaveData );
  APTR1L = LSB( &WaveData );

  // destination
  AUTOPTRH2 = 0xE4;
  AUTOPTRL2 = 0x00;

  // transfer
  for ( i = 0x00; i < 128; i++ )
  {
    EXTAUTODAT2 = EXTAUTODAT1;
  }

// Configure GPIF Address pins, output initial value,
  PORTCCFG = 0xFF;    // [7:0] as alt. func. GPIFADR[7:0]
  OEC = 0xFF;         // and as outputs
  PORTECFG |= 0x80;   // [8] as alt. func. GPIFADR[8]
  OEC |= 0x80;        // and as output

// ...OR... tri-state GPIFADR[8:0] pins
//  PORTCCFG = 0x00;  // [7:0] as port I/O
//  OEC = 0x00;       // and as inputs
//  PORTECFG &= 0x7F; // [8] as port I/O
//  OEC &= 0x7F;      // and as input

// GPIF address pins update when GPIFADRH/L written
  SYNCDELAY;                    //
  GPIFADRH = 0x00;    // bits[7:1] always 0
  SYNCDELAY;                    //
  GPIFADRL = 0x00;    // point to PERIPHERAL address 0x0000
}

#ifdef TESTING_GPIF
// TODO: You may add additional code below.

void OtherInit( void )
{ // interface initialization
  // ...see TD_Init( );
}

// Set Address GPIFADR[8:0] to PERIPHERAL
void Peripheral_SetAddress( WORD gaddr )
{
  SYNCDELAY;                    //
  GPIFADRH = gaddr >> 8;
  SYNCDELAY;                    //
  GPIFADRL = ( BYTE )gaddr; // setup GPIF address
}
```

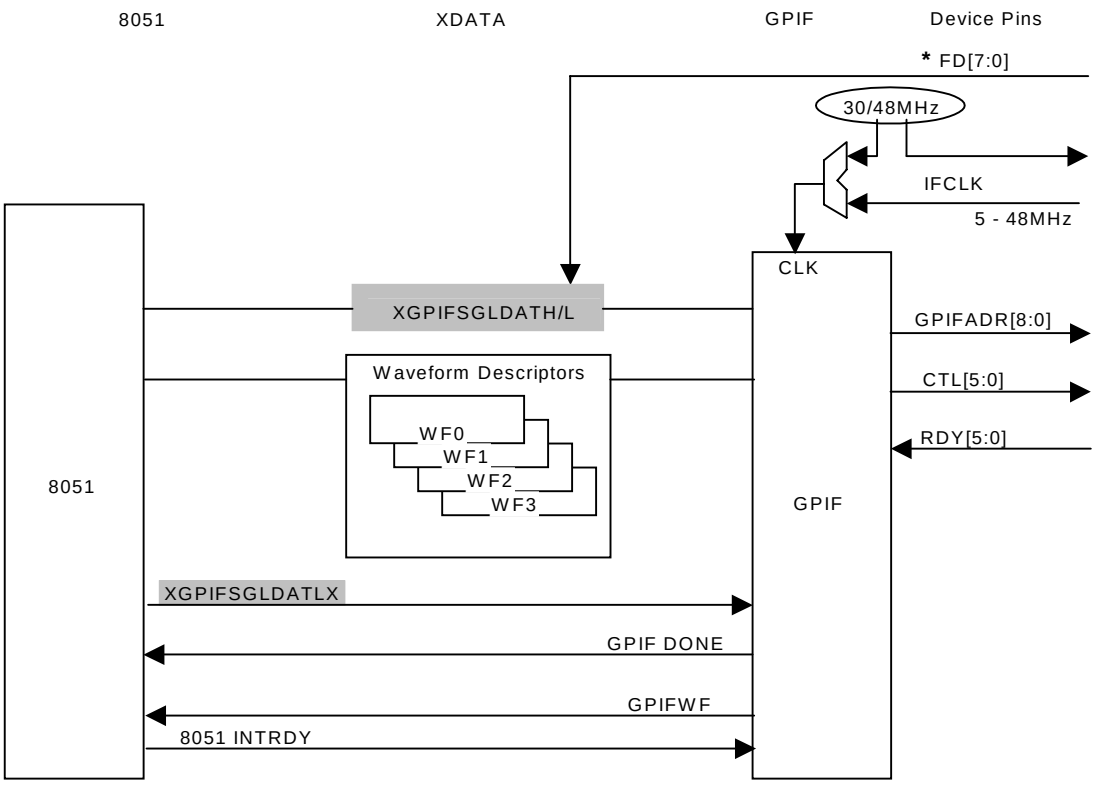
```
// Set EP2GPIF Transaction Count
void Peripheral_SetEP2GPIFTC( WORD xfrcnt )
{
  SYNCDELAY;                    //
  EP2GPIFTCH = xfrcnt >> 8;  // setup transaction count
  SYNCDELAY;                    //
  EP2GPIFTCL = ( BYTE )xfrcnt;
}

// Set EP4GPIF Transaction Count
void Peripheral_SetEP4GPIFTC( WORD xfrcnt )
{
  SYNCDELAY;                    //
  EP4GPIFTCH = xfrcnt >> 8;  // setup transaction count
  SYNCDELAY;                    //
  EP4GPIFTCL = ( BYTE )xfrcnt;
}

// Set EP6GPIF Transaction Count
void Peripheral_SetEP6GPIFTC( WORD xfrcnt )
{
  SYNCDELAY;                    //
  EP6GPIFTCH = xfrcnt >> 8;  // setup transaction count
  SYNCDELAY;                    //
  EP6GPIFTCL = ( BYTE )xfrcnt;
}

// Set EP8GPIF Transaction Count
void Peripheral_SetEP8GPIFTC( WORD xfrcnt )
{
  SYNCDELAY;                    //
  EP8GPIFTCH = xfrcnt >> 8;  // setup transaction count
  SYNCDELAY;                    //
  EP8GPIFTCL = ( BYTE )xfrcnt;
}

#define GPIF_FLGSELPF 0
#define GPIF_FLGSELEF 1
#define GPIF_FLGSELFF 2

// Set EP2GPIF Decision Point FIFO Flag Select (PF, EF, FF)
void SetEP2GPIFFLGSEL( WORD DP_FIFOFlag )
{
  EP2GPIFFLGSEL = DP_FIFOFlag;
}

// Set EP4GPIF Decision Point FIFO Flag Select (PF, EF, FF)
void SetEP4GPIFFLGSEL( WORD DP_FIFOFlag )
{
  EP4GPIFFLGSEL = DP_FIFOFlag;
}

// Set EP6GPIF Decision Point FIFO Flag Select (PF, EF, FF)
void SetEP6GPIFFLGSEL( WORD DP_FIFOFlag )
{
  EP6GPIFFLGSEL = DP_FIFOFlag;
}
```

```
// Set EP8GPIF Decision Point FIFO Flag Select (PF, EF, FF)
void SetEP8GPIFFLGSEL( WORD DP_FIFOFlag )
{
  EP8GPIFFLGSEL = DP_FIFOFlag;
}

// Set EP2GPIF Programmable Flag STOP, overrides Transaction Count
void SetEP2GPIFPFSTOP( void )
{
  EP2GPIFPFSTOP = 0x01;
}

// Set EP4GPIF Programmable Flag STOP, overrides Transaction Count
void SetEP4GPIFPFSTOP( void )
{
  EP4GPIFPFSTOP = 0x01;
}

// Set EP6GPIF Programmable Flag STOP, overrides Transaction Count
void SetEP6GPIFPFSTOP( void )
{
  EP6GPIFPFSTOP = 0x01;
}

// Set EP8GPIF Programmable Flag STOP, overrides Transaction Count
void SetEP8GPIFPFSTOP( void )
{
  EP8GPIFPFSTOP = 0x01;
}

// write single byte to PERIPHERAL, using GPIF
void Peripheral_SingleByteWrite( BYTE gdata )
{
  while( !( GPIFTRIG & 0x80 ) ) // poll GPIFTRIG.7 Done bit
  {
     ;
  }

  XGPIFSGLDATLX = gdata;        // trigger GPIF
                                // ...single byte write transaction
}

// write single word to PERIPHERAL, using GPIF
void Peripheral_SingleWordWrite( WORD gdata )
{
  while( !( GPIFTRIG & 0x80 ) )  // poll GPIFTRIG.7 Done bit
  {
    ;
  }

// using register(s) in XDATA space
  XGPIFSGLDATH = gdata >> 8;
  XGPIFSGLDATLX = gdata;        // trigger GPIF
                                // ...single word write transaction
}

// read single byte from PERIPHERAL, using GPIF
void Peripheral_SingleByteRead( BYTE xdata *gdata )
```

```
{
  static BYTE g_data = 0x00;

  while( !( GPIFTRIG & 0x80 ) )  // poll GPIFTRIG.7 Done bit
  {
     ;
  }

// using register(s) in XDATA space, dummy read
  g_data = XGPIFSGLDATLX;       // trigger GPIF
                                // ...single byte read transaction
  while( !( GPIFTRIG & 0x80 ) ) // poll GPIFTRIG.7 Done bit
  {
     ;
  }

// using register(s) in XDATA space,
  *gdata = XGPIFSGLDATLNOX;     // ...GPIF reads byte from PERIPHERAL
}

// read single word from PERIPHERAL, using GPIF
void Peripheral_SingleWordRead( WORD xdata *gdata )
{
  BYTE g_data = 0x00;

  while( !( GPIFTRIG & 0x80 ) ) // poll GPIFTRIG.7 Done bit
  {
     ;
  }

// using register(s) in XDATA space, dummy read
  g_data = XGPIFSGLDATLX;       // trigger GPIF
                                // ...single word read transaction

  while( !( GPIFTRIG & 0x80 ) ) // poll GPIFTRIG.7 Done bit
  {
     ;
  }

// using register(s) in XDATA space, GPIF reads word from PERIPHERAL
  *gdata = ( ( WORD )XGPIFSGLDATH << 8 ) | ( WORD )XGPIFSGLDATLNOX;
}

#define GPIFTRIGWR 0
#define GPIFTRIGRD 4

#define GPIF_EP2 0
#define GPIF_EP4 1
#define GPIF_EP6 2
#define GPIF_EP8 3

// write byte(s)/word(s) to PERIPHERAL, using GPIF and EPxFIFO
// if EPx WORDWIDE=0 then write byte(s)
// if EPx WORDWIDE=1 then write word(s)
void Peripheral_FIFOWrite( BYTE FIFO_EpNum )
{
  while( !( GPIFTRIG & 0x80 ) ) // poll GPIFTRIG.7 Done bit
  {
```

```
      ;
  }

  // trigger FIFO write transaction(s), using SFR
  GPIFTRIG = FIFO_EpNum;  // R/W=0, EP[1:0]=FIFO_EpNum for EPx write(s)
}

// read byte(s)/word(s) from PERIPHERAL, using GPIF and EPxFIFO
// if EPx WORDWIDE=0 then read byte(s)
// if EPx WORDWIDE=1 then read word(s)
void Peripheral_FIFORead( BYTE FIFO_EpNum )
{
  while( !( GPIFTRIG & 0x80 ) ) // poll GPIFTRIG.7 GPIF Done bit
  {
     ;
  }

  // trigger FIFO read transaction(s), using SFR
  GPIFTRIG = GPIFTRIGRD | FIFO_EpNum; // R/W=1, EP[1:0]=FIFO_EpNum for EPx read(s)
}
```

10.4.1 Single-Read Transactions



* All EPx WORDWIDE bits must be cleared to 0 for 8-bit single transactions. If any of the EPx WORDWIDE bits are set to 1, then single transactions will be 16 bits wide.

Figure 10-14. Firmware Launches a Single-Read Waveform, WORDWIDE=0

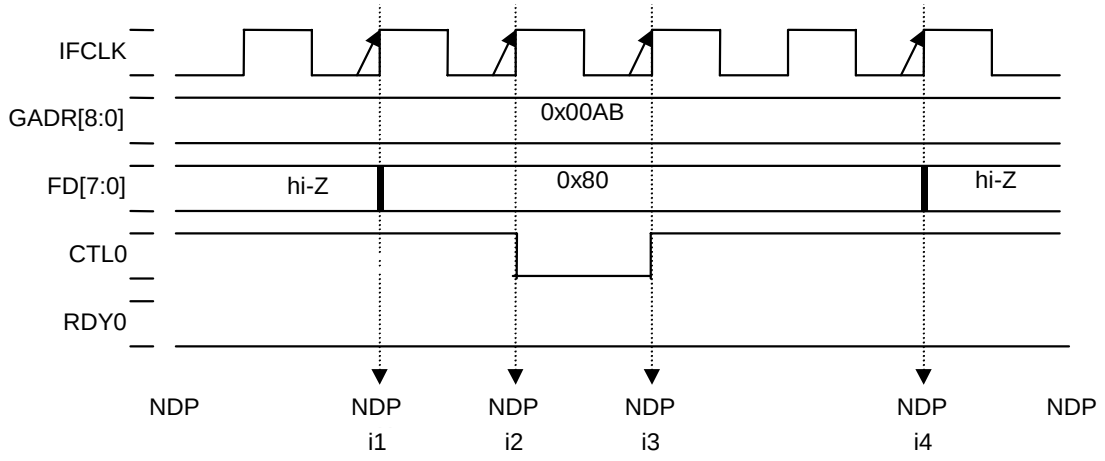


Figure 10-15. Single-Read Transaction Waveform

State	0	1	2	3	4	5	6	7
AddrMode	Same Val	Same Val	Same Val	Same Val	Same Val	Same Val	Same Val	
DataMode	No Data	No Data	Activate	NO Data	NO Data	NO Data	NO Data	
NextData	SameData	SameData	SameData	SameData	SameData	SameData	SameData	
Int Trig	No Int	No Int	No Int	No Int	No Int	No Int	No Int	
IF/Wait	Wait 4	Wait 1	Wait 1	Wait 2	Wait 1	Wait 1	Wait 1	
Term A								
LFUNC								
Term B								
Branch1								
Branch0								
Re-execute								
CTL0	1	1	0	1	1	1	1	1
CTL1	1	1	1	1	1	1	1	1
CTL2	1	1	1	1	1	1	1	1
CTL3	1	1	1	1	1	1	1	1
CLT4	1	1	1	1	1	1	1	1
CTL5	1	1	1	1	1	1	1	1

Figure 10-16. GPIFTool Setup for the Waveform of Figure 10-15

To perform a Single-Read transaction:

1. Initialize the GPIF Configuration Registers and Waveform Descriptors.
2. Perform a dummy **read** of the XGPIFSGLDATLX register to start a single transaction.
3. Wait for the GPIF to indicate that the transaction is complete. When the transaction is complete, the DONE bit (GPIFIDLECS.7 or GPIFTRIG.7) will be set to 1. If enabled, a GPIFDONE interrupt will also be generated.
4. Depending on the bus width and the desire to start another transaction, the read data can be retrieved from the XGPIFSGLDATH, XGPIFSGLDATLX, and/or the XGPIFSGLDATLNOX register (or from the SFR-space copies of these registers):

   In 16-bit mode **only**, the most significant byte, FD[15:8], of data is read from the XGPIFSGLDATH register.

   In 8- and 16-bit modes, the least significant byte of data is read by either:

   - reading XGPIFSGLDATLX, which reads the least significant byte and starts another Single-Read transaction.
   - reading XGPIFSGLDATLNOX, which reads the least significant byte but does **not** start another Single-Read transaction.

   The following C program fragments (Figures 10-17 and 10-18) illustrate how to perform a Single-Read transaction in 8-bit mode (WORDWIDE=0):

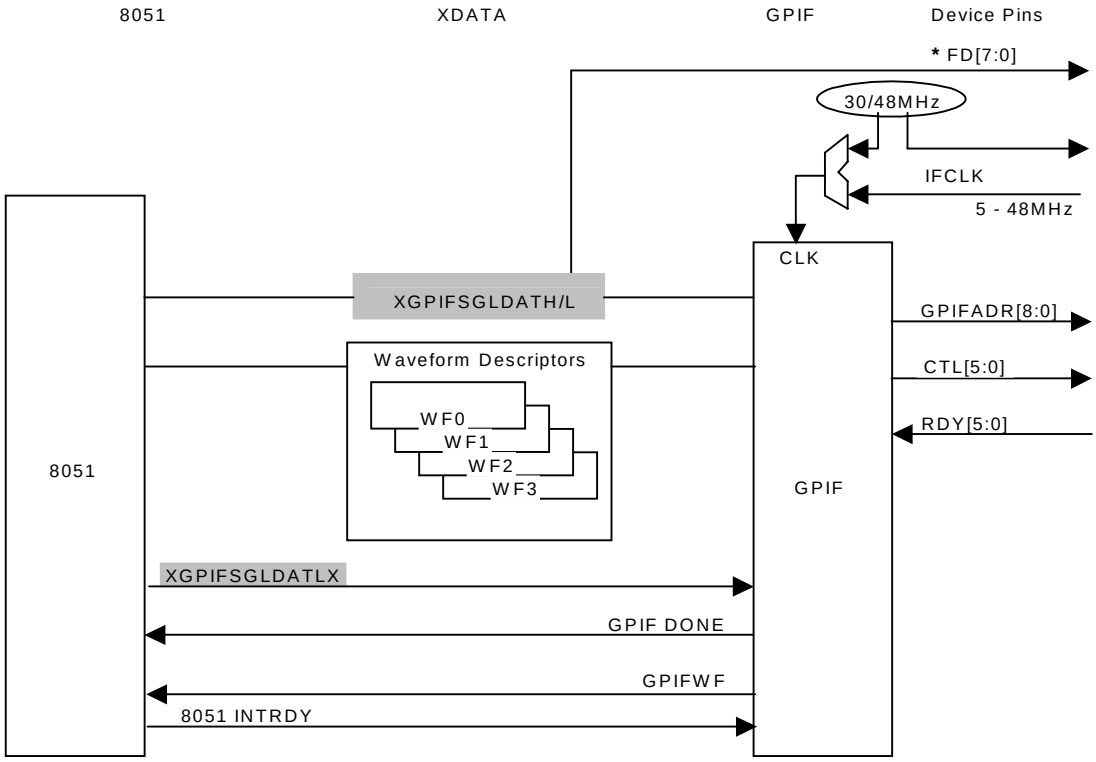
```
#define PERIPHCS 0x00AB
#define AOKAY 0x80
#define BURSTMODE 0x0000
#define TRISTATE 0xFFFF
#define EVER ;;

// prototypes
void GpifInit( void );

// Set Address GPIFADR[8:0] to PERIPHERAL
void Peripheral_SetAddress( WORD gaddr )
{
  if( gaddr < 512 )
  { // drive GPIF address bus w/gaddr
    GPIFADRH = gaddr >> 8;
    SYNCDELAY;
    GPIFADRL = ( BYTE )gaddr; // setup GPIF address
  }
  else
  { // tristate GPIFADR[8:0] pins
    PORTCCFG = 0x00;  // [7:0] as port I/O
    OEC = 0x00;  // and as inputs
    PORTECFG &= 0x7F;  // [8] as port I/O
     OEC &= 0x7F;  // and as input
  }
}

// read single byte from PERIPHERAL, using GPIF
void Peripheral_SingleByteRead( BYTE xdata *gdata )
{
  static BYTE g_data = 0x00;

  while( !( GPIFTRIG & 0x80 ) )  // poll GPIFTRIG.7 Done bit
  {
     ;
  }

  // using register(s) in XDATA space, dummy read
  g_data = XGPIFSGLDATLX;  // to trigger GPIF single byte read transaction

  while( !( GPIFTRIG & 0x80 ) )  // poll GPIFTRIG.7 Done bit
  {
     ;
  }

  // using register(s) in XDATA space, GPIF read byte from PERIPHERAL here
  *gdata = XGPIFSGLDATLNOX;
}
```

Figure 10-17. Single-Read Transaction Functions

```
void TD_Init( void )
{
  BYTE xdata periph_status;

  … … … … …
  GpifInit();  // Configures GPIF from GPIFTool generated waveform data

  // TODO: configure other endpoints, etc. here

  // TODO: arm OUT buffer(s) here

  // setup INT4 as internal source for GPIF interrupts
  // using INT4CLR (SFR), automatically enabled
  //INTSETUP |= 0x03;  //Enable INT4 Autovectoring
  //SYNCDELAY;
  //GPIFIE = 0x03;  // Enable GPIFDONE and GPIFWF interrupt(s)
  //SYNCDELAY;
  //EIE |= 0x04;  // Enable INT4 ISR, EIE.2(EIEX4)=1

  // TODO: configure GPIF interrupt(s) to meet your needs here
     … … … … …

  // get status of peripheral function
  Peripheral_SetAddress( PERIPHCS );
  Peripheral_SingleByteRead( &periph_status );

  if( periph_status == AOKAY )
  { // set it and forget it
    Peripheral_SetAddress( BURSTMODE );
  }
  else
  {
    Peripheral_SetAddress( TRISTATE );
    Housekeeping( );
    EZUSB_Discon( TRUE ); // Disconnect from the bus
    for( EVER )
    { // do not xfr peripheral data
      ;
    }
  }
}
```

Figure 10-18. Initialization Code for Single-Read Transactions

10.4.2 Single-Write Transactions



* All EPx WORDWIDE bits must be cleared to zero for 8-bit single transactions. If any of the EPx WORDWIDE bits are set to 1, then single transactions will be 16 bits wide.

Figure 10-19. Firmware Launches a Single-Write Waveform, WORDWIDE=0

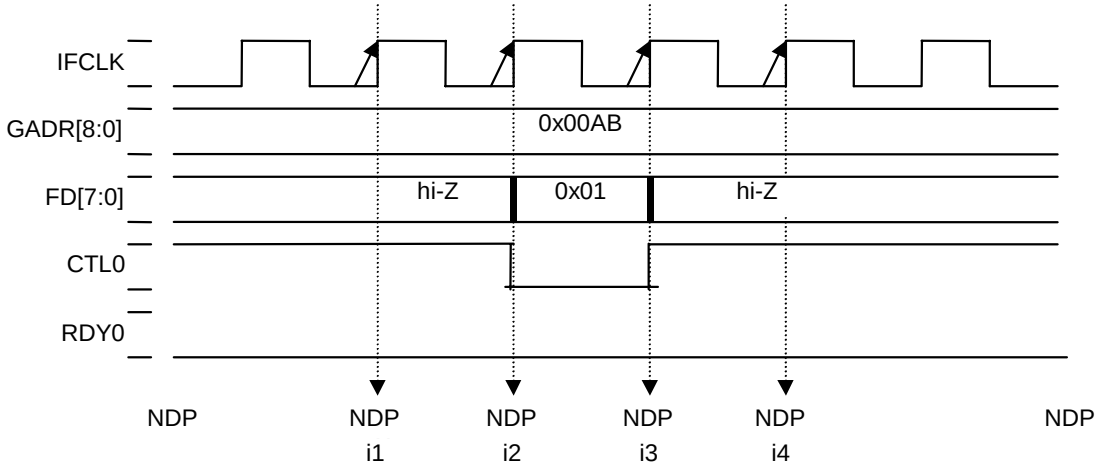


Figure 10-20. Single-Write Transaction Waveform

State	0	1	2	3	4	5	6	7
AddrMode	Same Val	Same Val	Same Val	Same Val	Same Val	Same Val	Same Val	
DataMode	No Data	No Data	Activate	NO Data	NO Data	NO Data	NO Data	
NextData	SameData	SameData	SameData	SameData	SameData	SameData	SameData	
Int Trig	No Int	No Int	No Int	No Int	No Int	No Int	No Int	
IF/Wait	Wait 4	Wait 1	Wait 1	Wait 1	Wait 1	Wait 1	Wait 1	
Term A								
LFUNC								
Term B								
Branch1								
Branch0								
Re-execute								
CTL0	1	1	0	1	1	1	1	1
CTL1	1	1	1	1	1	1	1	1
CTL2	1	1	1	1	1	1	1	1
CTL3	1	1	1	1	1	1	1	1
CLT4	1	1	1	1	1	1	1	1
CTL5	1	1	1	1	1	1	1	1

Figure 10-21. GPIFTool Setup for the Waveform of Figur e10-20

Single-Write transactions are simpler than Single-Read transactions because no dummy-read operation is required. To execute a Single-Write transaction:

1. Initialize the GPIF Configuration Registers and Waveform Descriptors.
2. If in 16-bit mode (WORDWIDE = 1), write the most-significant byte of the data to the XGPIFSGLDATH register, then **write** the least-significant byte to the XGPIFSGLDATLX regis-

ter to start a Single-Write transaction.

In 8-bit mode, simply **write** the data to the XGPIFSGLDATLX register to start a Single-Write transaction.

3. Wait for the GPIF to indicate that the transaction is complete. When the transaction is complete, the DONE bit (GPIFIDLECS.7 or GPIFTRIG.7) will be set to 1. If enabled, a GPIFDONE interrupt will also be generated.

   The following C program fragments (Figures 10-22 and 10-23) illustrate how to perform a Single-Write transaction in 8-bit mode (WORDWIDE=0):

```
#define PERIPHCS 0x00AB
#define P_HSMODE 0x01

// prototypes
void GpifInit( void );

// Set Address GPIFADR[8:0] to PERIPHERAL
void Peripheral_SetAddress( WORD gaddr )
{
  GPIFADRH = gaddr >> 8;
  SYNCDELAY;
  GPIFADRL = ( BYTE )gaddr; // setup GPIF address
}

// write single byte to PERIPHERAL, using GPIF
void Peripheral_SingleByteWrite( BYTE gdata )
{
  while( !( GPIFTRIG & 0x80 ) )  // poll GPIFTRIG.7 Done bit
  {
     ;
  }

  XGPIFSGLDATLX = gdata;  // trigger GPIF single byte write transaction
}
```

Figure 10-22. Single-Write Transaction Functions

```
void TD_Init( void )
{
  … … … … …
  GpifInit();  // Configures GPIF from GPIFTool generated waveform data

  // TODO: configure other endpoints, etc. here

  // TODO: arm OUT buffer(s) here

  // setup INT4 as internal source for GPIF interrupts
  // using INT4CLR (SFR), automatically enabled
  //INTSETUP |= 0x03;  //Enable INT4 Autovectoring
  //SYNCDELAY;
  //GPIFIE = 0x03;  // Enable GPIFDONE and GPIFWF interrupt(s)
  //SYNCDELAY;
  //EIE |= 0x04;  // Enable INT4 ISR, EIE.2(EIEX4)=1

  // TODO: configure GPIF interrupt(s) to meet your needs here
     … … … … …

  // tell peripheral we're going into high speed xfr mode
  Peripheral_SetAddress( PERIPHCS );
  Peripheral_SingleByteWrite( P_HSMODE );
}
```

Figure 10-23. Initialization Code for Single-Write Transactions

10.4.3 FIFO-Read and FIFO-Write Transactions

FIFO-Read and FIFO-Write waveforms transfer data to and from the FX2's Slave FIFOs (see *Chapter 9 "Slave FIFOs"*). The waveform is started by writing to EPxTRIG, where "x" represents the FIFO (2, 4, 6, or 8) to/from which data should be transferred, or to GPIFTRIG.

A FIFO-Read or FIFO-Write waveform will generally transfer a long stream of data rather than a single byte or word. Usually, the waveform is programmed to terminate when a FIFO flag asserts (e.g., when an IN FIFO is full or an OUT FIFO is empty) or after a specified number of *transactions*. A "transaction" is a transfer of a single byte (if WORDWIDE = 0) or word (if WORDWIDE = 1) to or from a FIFO. Using the *GPIFTool*'s terminology, a transaction is either an "Active" or "Next Data".

10.4.3.1 Transaction Counter

To use the Transaction Counter for FIFO "x", load GPIFTCB3:0 with the desired number of transactions (1 to 4,294,967,295; 0 = 4,294,967,296). When a FIFO-Read or -Write waveform is triggered on that FIFO, the GPIF will transfer the specified number of bytes (or words, if WORDWIDE = 1) automatically.

This mode of operation is called *Long Transfer Mode*; when the Transaction Counter is used in this way, the Waveform Descriptor should branch to the Idle State after each transaction.

Each time through the Idle State, the GPIF will decrement the Transaction Count; when it expires, the waveform terminates and the DONE bit is set.

Otherwise, the GPIF re-executes the entire Waveform Descriptor. *In Long Transfer Mode, the DONE bit isn't set until the Transaction Count expires.*

While the Transaction Count is active, the GPIF checks the Full Flag (for IN FIFOs) or the Empty Flag (for OUT FIFOs) on every pass through the Idle State. If the flag is asserted, the GPIF pauses until the over/underflow threat is removed, then it automatically resumes. In this way, the GPIF automatically throttles data flow in Long Transfer Mode.

The GPIFTCB3:0 registers are readable and they update as transactions occur, so the CPU can read the Transaction Count value at any time.

10.4.3.2 Reading the Transaction-Count Status in a DP State

To sample the transaction-count status in a DP State, set GPIFREADYCFG.5 to 1 (which instructs the FX2 to replace the RDY5 input with the transaction-count status), then launch a FIFO transaction which uses a transaction count. The FX2 will set RDY5 to 1 when the transaction count expires.

Typically, this feature is used with "re-execute" control tasks; it allows the Transaction Counter to be used without passing through the Idle State after each transaction.

10.4.4 GPIF Flag Selection

The GPIF can examine the PF, EF, or FF (of the current FIFO) during a waveform. One of the three flags is selected by the FS[1:0] bits in the EPxGPIFFLGSEL register; that selected flag is called the GPIF Flag.

10.4.5 GPIF Flag Stop

When EPxGPIFPFSTOP.0 is set to 1, FIFO-Read and -Write transactions are terminated by the assertion of the GPIF Flag. When this feature is used, it overrides the Transaction Counter; the GPIF waveform terminates (sets DONE to 1) *only* when the GPIF Flag asserts.

No special programming of the Waveform Descriptors is necessary, and FIFO Waveform Descriptors that transition through the Idle State on each transaction (i.e., waveforms that don't use the Transaction Counter) are unaffected. Automatic throttling of the FIFOs in IDLE still occurs, so there's no danger that the GPIF will write to a full FIFO or read from an empty FIFO.

*Unless the firmware aborts the GPIF transfer by writing to the GPIFABORT register, **only** the GPIF Flag assertion will terminate the waveform and set the DONE bit.*

A waveform can potentially execute forever if the GPIF Flag never asserts.

The GPIF Flag is tested only while transitioning through the Idle State, and it isn't latched. *If a GPIF Flag assertion occurs in one State, and the next State is a DP which tests the GPIF Flag and waits until it's de-asserted before allowing the state machine to continue to the Idle State, the GPIF will automatically branch back to State 0 as though the GPIF Flag had never been asserted.*

10.4.5.1 Performing a FIFO-Read Transaction

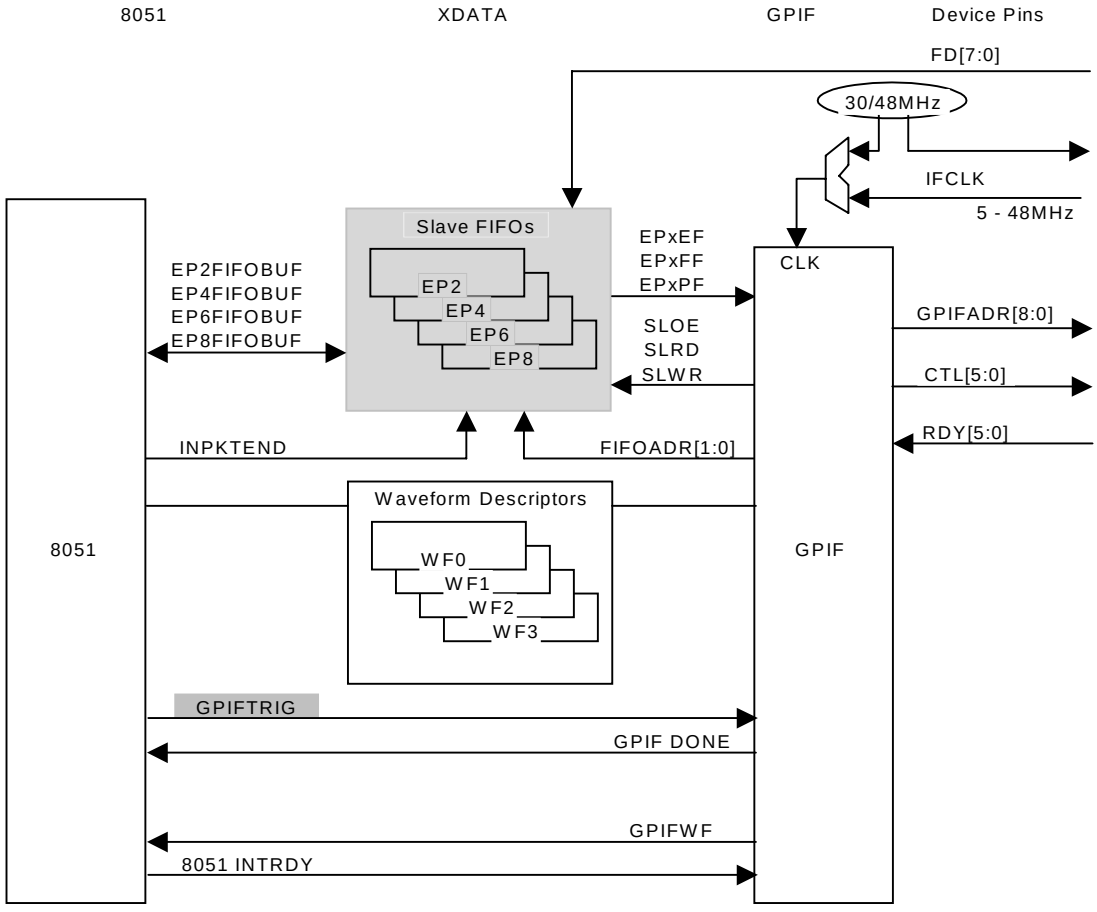


Figure 10-24. Firmware Launches a FIFO-Read Waveform

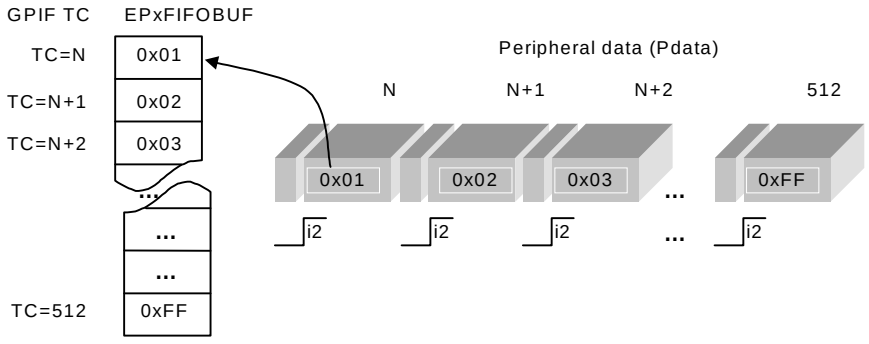


Figure 10-25. Example FIFO-Read Transaction

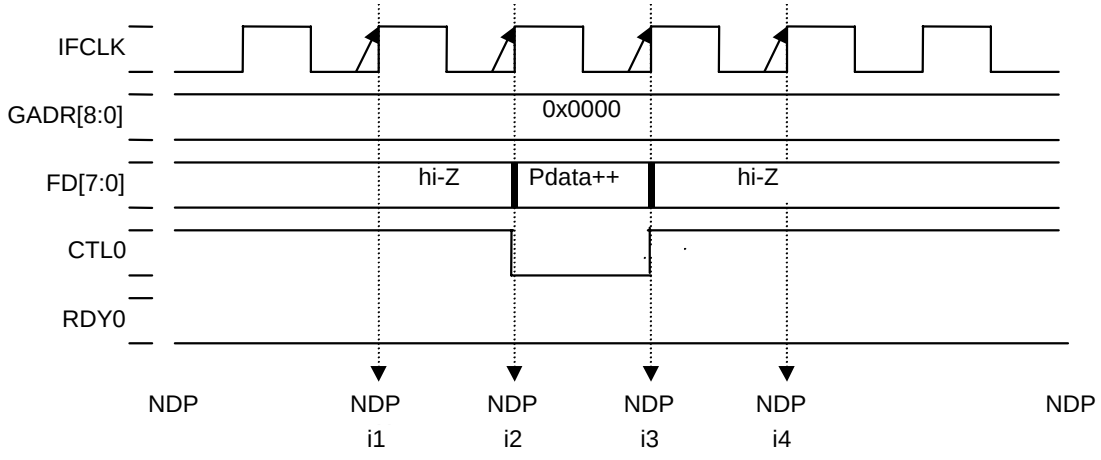


Figure 10-26. FIFO-Read Transaction Waveform

The above waveform executes until the Transaction Counter expires (until it counts to 512, in this example). The Transaction Counter is decremented and sampled on each pass through the Idle State.

Each iteration of the waveform reads a data value from the FIFO Data bus into the FIFO, then decrements and checks the Transaction Counter. When it expires, the DONE bit is set to 1 and the GPIFDONE interrupt request is asserted.

State	0	1	2	3	4	5	6	7
AddrMode	Same Val	Same Val	Same Val	Same Val	Same Val	Same Val	Same Val	
DataMode	No Data	No Data	Activate	NO Data	NO Data	NO Data	NO Data	
NextData	SameData	SameData	SameData	SameData	SameData	SameData	SameData	
Int Trig	No Int	No Int	No Int	No Int	No Int	No Int	No Int	
IF/Wait	Wait 4	Wait 1	Wait 1	Wait 1	Wait 1	Wait 1	Wait 1	
Term A								
LFUNC								
Term B								
Branch1								
Branch0								
Re-execute								
CTL0	1	1	0	1	1	1	1	1
CTL1	1	1	1	1	1	1	1	1
CTL2	1	1	1	1	1	1	1	1
CTL3	1	1	1	1	1	1	1	1
CLT4	1	1	1	1	1	1	1	1
CTL5	1	1	1	1	1	1	1	1

Figure 10-27. GPIFTool Setup for the Waveform of Figur e10-26

Typically, when performing a FIFO Read, only one “Activate” is needed in the waveform, since each execution of “Activate” increments the internal FIFO pointer (and EPxBCH:L) automatically.

To perform a FIFO-Read Transaction:

1. In the GPIFTRIG register, set the RW bit to 1 and load EP1:0 with the appropriate value for the FIFO which is to receive the data.
2. Program the FX2 to detect completion of the transaction. As with all GPIF Transactions, bit 7 of the GPIFTRIG register (the DONE bit) signals when the Transaction is complete.
3. Program the FX2 to commit (“pass-on”) the data from the FIFO to the endpoint. The data can be transferred from the FIFO to the endpoint by either of the following methods:
   - AUTOIN=1: CPU is not in the data path; the FX2 automatically commits data from the FIFO Data bus to the USB.
   - AUTOIN=0: Firmware must manually commit data to the USB by writing either EPxBCL or INPKTEND (with SKIP=0).

   The following C program fragments (Figures 10-28 through 10-31) illustrate how to perform a FIFO-Read transaction in 8-bit mode (WORDWIDE = 0) with AUTOIN = 0:

```
#define GPIFTRIGRD 4

#define GPIF_EP2 0
#define GPIF_EP4 1
#define GPIF_EP6 2
#define GPIF_EP8 3

#define BURSTMODE 0x0000
#define HSPKTSIZE 512

… … … … …

// read(s) from PERIPHERAL, using GPIF and EPxFIFO
void Peripheral_FIFORead( BYTE FIFO_EpNum )
{
  while( !( GPIFTRIG & 0x80 ) ) // poll GPIFTRIG.7 GPIF Done bit
  {
     ;
  }

  // trigger FIFO read transaction(s), using SFR
  GPIFTRIG = GPIFTRIGRD | FIFO_EpNum;   // R/W=1, EP[1:0]=FIFO_EpNum
                                        // for EPx read(s)
}

// Set EP8GPIF Transaction Count
void Peripheral_SetEP8GPIFTC( WORD xfrcnt)
{
  EP8GPIFTCH = xfrcnt >> 8;  // setup transaction count
  EP8GPIFTCL = ( BYTE )xfrcnt;
}

… … … … …
```

Figure 10-28. FIFO-Read Transaction Functions

```
void TD_Init( void )
{
  … … … … …
  GpifInit();  // Configures GPIF from GPIFTool generated waveform data

  // TODO: configure other endpoints, etc. here
  EP8CFG = 0xE0;  // EP8 is DIR=IN, TYPE=BULK
  SYNCDELAY;
  EP8FIFOCFG = 0x04;  // EP8 is AUTOOUT=0, AUTOIN=0, ZEROLEN=1, WORDWIDE=0

  // TODO: arm OUT buffer(s) here

  // setup INT4 as internal source for GPIF interrupts
  // using INT4CLR (SFR), automatically enabled
  //INTSETUP |= 0x03;  //Enable INT4 Autovectoring
  //SYNCDELAY;
  //GPIFIE = 0x03;  // Enable GPIFDONE and GPIFWF interrupt(s)
  //SYNCDELAY;
  //EIE |= 0x04;  // Enable INT4 ISR, EIE.2(EIEX4)=1

  // TODO: configure GPIF interrupt(s) to meet your needs here
     … … … … …

  // tell peripheral we're going into high speed xfr mode
  Peripheral_SetAddress( PERIPHCS );
  Peripheral_SingleByteWrite( P_HSMODE );

  // configure some GPIF registers
  Peripheral_SetAddress( BURSTMODE );
  Peripheral_SetEP8GPIFTC( HSPKTSIZE );
}
```

Figure 10-29. Initialization Code for FIFO-Read Transactions

```
void TD_Poll( void )
{
  … … … … …
  if( ibn_event_flag )
  { // host is asking for EP8 data
    Peripheral_FIFORead( GPIF_EP8 );
    ibn_event_flag = 0;
  }

  if( gpifdone_event_flag )
  { // GPIF currently pointing to EP8, last FIFO accessed
    if( !( EP2468STAT & 0x80 ) )
    { // EP8F=0 when buffer available
      INPKTEND = 0x08;     // Firmware commits pkt by writing 8 to INPKTEND
      gpifdone_event_flag = 0;
    }
  }
  … … … … …
}
```

Figure 10-30. FIFO-Read w/ AUTOIN = 0, Committing Packets via INPKTEND w/SKIP=0

```
void TD_Poll( void )
{
  … … … … …
  if( !( EP68FIFOFLGS & 0x10 ) )
  { // EP8FF=0 when buffer available
    // host is taking EP8 data fast enough
    Peripheral_FIFORead( GPIF_EP8 );
  }

  if( gpifdone_event_flag )
  { // GPIF currently pointing to EP8, last FIFO accessed
    if( !( EP2468STAT & 0x80 ) )
    { // EP8F=0 when buffer available
      // modify the data
      EP8FIFOBUF[ 0 ] = 0x02;  // <STX>, packet start of text msg
      EP8FIFOBUF[ 7 ] = 0x03;  // <ETX>, packet end of text msg
      SYNCDELAY;
      EP8BCH = 0x00;
      SYNCDELAY;
      EP8BCL = 0x08;  // pass buffer on to host
    }
  }
  … … … … …
}
```

Figure 10-31. FIFO-Read w/ AUTOIN = 0, Committing Packets via EPxBCL

10.4.6 Firmware Access to IN packet(s), (AUTOIN=1)

The only difference between auto (AUTOIN=1) and manual (AUTOIN=0) modes for IN packet(s) is the packet length feature (EPxAUTOINLENH/L).

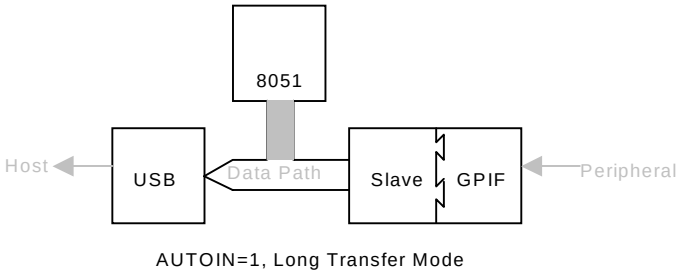


Figure 10-32. AUTOIN=1, GPIF FIFO Read Transactions, AUTOIN = 1

```
TD_Init():

    EP8CFG = 0xE0;  // EP8 is DIR=IN, TYPE=BULK
    SYNCDELAY;
    EP8FIFOCFG = 0x0C;  // EP8 is AUTOOUT=0, AUTOIN=1, ZEROLEN=1, WORDWIDE=0
    SYNCDELAY;
    EP8AUTOINLENH = 0x02;  // if AUTOIN=1, auto commit 512 byte packets
    SYNCDELAY;
    EP8AUTOINLENL = 0x00;


TD_Poll():

    // no code necessary to xfr data from master to host!
    // AUTOIN=1 and EP8AUTOINLEN=512 auto commits packets,
    // in 512 byte chunks.
```

Figure 10-33. FIFO-Read Transaction Code, AUTOIN = 1

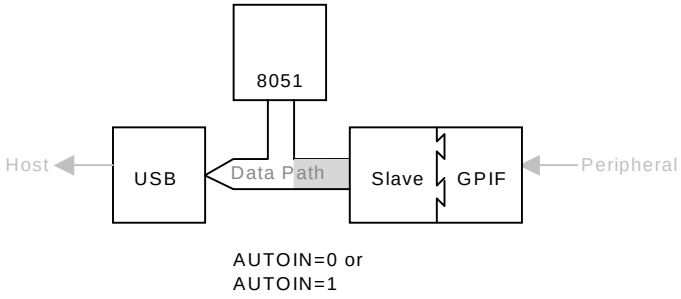


Figure 10-34. Firmware intervention, AUTOIN = 0/1

10.4.7 Firmware Access to IN Packet(s), (AUTOIN = 0)

In manual IN mode (AUTOIN=0), the firmware has the following options:

1. It can commit (“pass-on”) packet(s) sent from the master to the host when a buffer is available, by writing the INPKTEND register with the corresponding EPx number and SKIP=0 (see Figure 10-35).
2. It can skip a packet by writing to INPKTEND with SKIP=1. See Figure 10-36.
3. It can source or edit a packet (i.e., write directly to EPxFIFOBUF) then write the EPxBCL. See Figure 10-37.

```
TD_Poll():
… … … … …
if( master_finished_longxfr( ) )
{  // master currently points to EP8, last FIFO accessed
  if( !( EP68FIFOFLGS & 0x10 ) )
  { // EP8FF=0 when buffer available
    INPKTEND = 0x08;  // Firmware commits pkt
                      // by writing #8 to INPKTEND
    release_master( EP8 );
  }
}
… … … … …
```

Figure 10-35. Committing a Packet by Writing INPKTEND with EPx Number (w/SKIP=0)

```
TD_Poll():
… … … … …
if( master_finished_longxfr( ) )
{  // master currently points to EP8, last FIFO accessed
  if( !( EP68FIFOFLGS & 0x10 ) )
  { // EP8FF=0 when buffer available
    INPKTEND = 0x88;  // Firmware commits pkt
                      // by writing 88 to INPKTEND
    release_master( EP8 );
  }
}
… … … … …
```

Figure 10-36. Skipping a Packet by Writing to INPKTEND w/SKIP=1

```
TD_Poll():
… … … … …
if( source_pkt_event )
{  // 100msec background timer fired
  if( holdoff_master( ) )
  {  // signaled “busy” to master successful
    while( !( EP68FIFOFLGS & 0x20 ) )
    {  // EP8EF=0, when buffer not empty
      ;  // wait ‘til host takes entire FIFO data
    }

    // Reset FIFO 8.

    FIFORESET = 0x80;  // Activate NAK-All to avoid race conditions.
    SYNCDELAY;
    FIFORESET = 0x08;  // Reset FIFO 8.
    SYNCDELAY;
    FIFORESET = 0x00;  // Deactivate NAK-All.

    EP8FIFOBUF[ 0 ] = 0x02;  // <STX>, packet start of text msg
    EP8FIFOBUF[ 1 ] = 0x06;  // <ACK>
    EP8FIFOBUF[ 2 ] = 0x07;  // <HEARTBEAT>
    EP8FIFOBUF[ 3 ] = 0x03;  // <ETX>, packet end of text msg
    SYNCDELAY;
    EP8BCH = 0x00;
    SYNCDELAY;
    EP8BCL = 0x04;  // pass src’d buffer on to host
  }
  else
  {
    history_record( EP8, BAD_MASTER );
  }
}
… … … … …
```

Figure 10-37. Sourcing an IN Packet by writing to EPxBCH:L

10.4.7.1 Performing a FIFO-Write Transaction

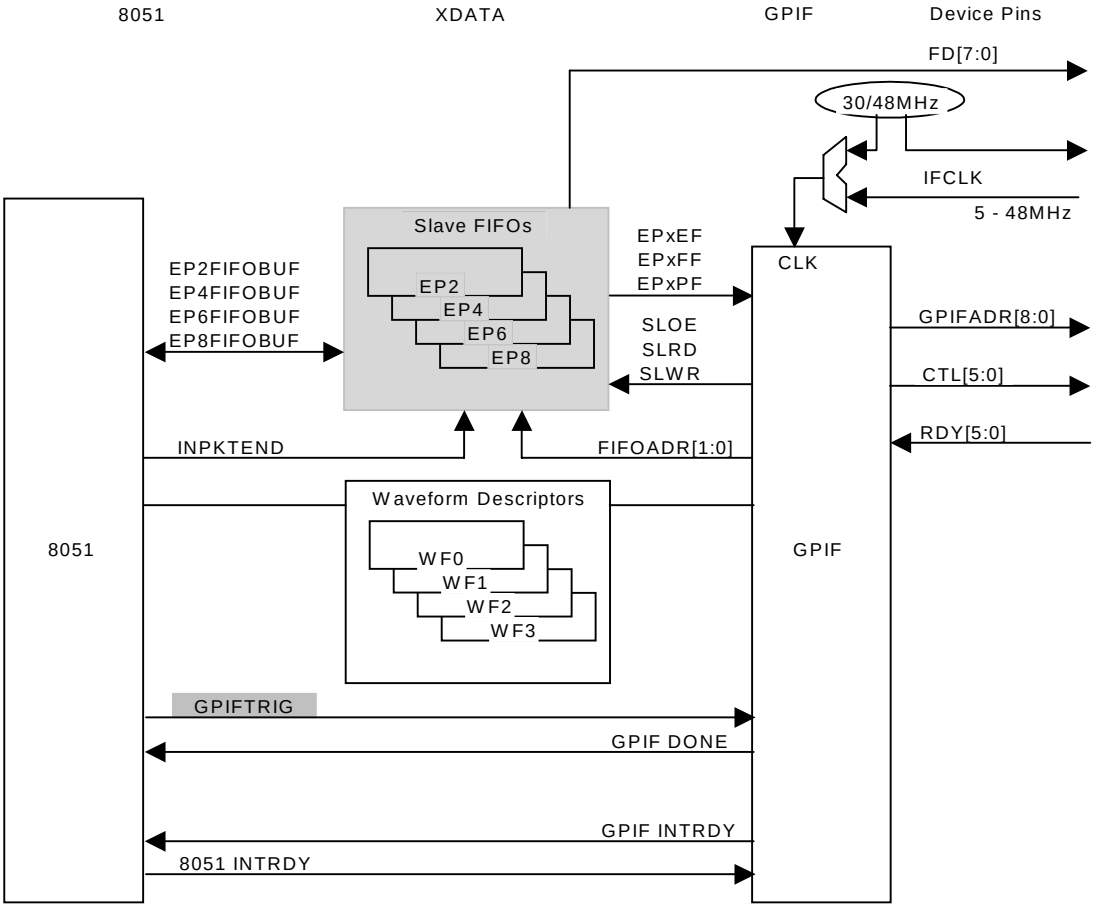


Figure 10-38. Firmware Launches a FIFO-Write Waveform

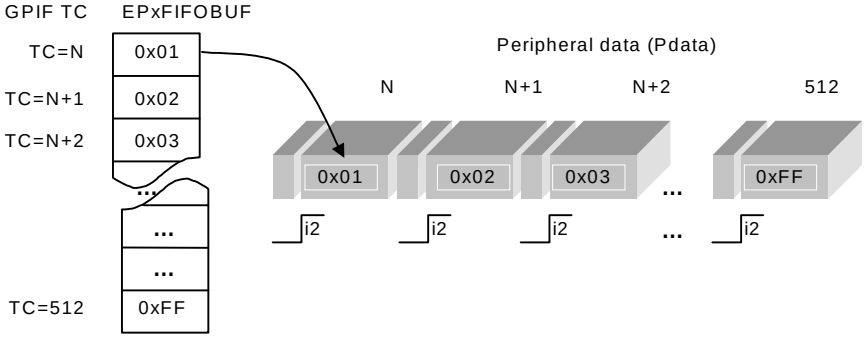


Figure 10-39. Example FIFO-Write Transaction

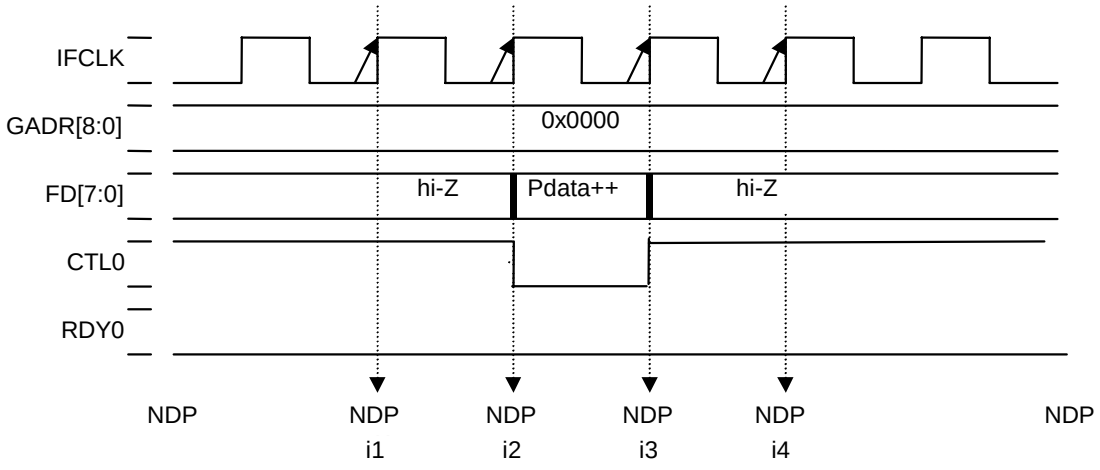


Figure 10-40. FIFO-Write Transaction Waveform

The above waveform executes until the Transaction Counter expires (until it counts to 512, in this example). The Transaction Counter is decremented and sampled on each pass through the Idle State.

Each iteration of the waveform writes a data value from the FIFO to the FIFO Data bus, then decrements and checks the Transaction Counter. When it expires, the DONE bit is set to 1 and the GPIFDONE interrupt request is asserted.

State	0	1	2	3	4	5	6	7
AddrMode	Same Val	Same Val	Same Val	Same Val	Same Val	Same Val	Same Val	
DataMode	No Data	No Data	Activate	NO Data	NO Data	NO Data	NO Data	
NextData	SameData	SameData	SameData	SameData	SameData	SameData	NextData	
Int Trig	No Int	No Int	No Int	No Int	No Int	No Int	No Int	
IF/Wait	Wait 4	Wait 1	Wait 1	Wait 1	Wait 1	Wait 1	Wait 1	
Term A								
LFUNC								
Term B								
Branch1								
Branch0								
Re-execute								
CTL0	1	1	0	1	1	1	1	1
CTL1	1	1	1	1	1	1	1	1
CTL2	1	1	1	1	1	1	1	1
CTL3	1	1	1	1	1	1	1	1
CLT4	1	1	1	1	1	1	1	1
CTL5	1	1	1	1	1	1	1	1

Figure 10-41. GPIFTool Setup for the Waveform of Figur e10-40

Typically, when performing a FIFO-Write, only one “NextData” is needed in the waveform, since each execution of “NextData” increments the FIFO pointer.

To perform a FIFO-Write Transaction:

1. In the GPIFTRIG register, set the RW bit to 0 and load EP1:0 with the appropriate value for the FIFO which is to receive the data.
2. Program the FX2 to detect completion of the transaction. As with all GPIF Transactions, bit 7 of the GPIFTRIG register (the DONE bit) signals when the Transaction is complete.
3. Program the FX2 to commit (“pass-on”) the data from the endpoint to the FIFO. The data can be transferred by either of the following methods:

   - AUTOOUT=1: CPU is not in the data path; the FX2 automatically commits data from the USB to the FIFO Data bus.
   - AUTOOUT=0: Firmware must manually commit data to the FIFO Data bus by writing EPxBCL.7=0 (firmware can choose to skip the current packet by writing EPxBCL.7=1).

   The following C program fragments (Figures 10-42 through 10-44) illustrate how to perform a FIFO-Read transaction in 8-bit mode (WORDWIDE = 0) with AUTOOUT = 0:

```
#define GPIFTRIGWR 0

#define GPIF_EP2 0
#define GPIF_EP4 1
#define GPIF_EP6 2
#define GPIF_EP8 3

#define BURSTMODE 0x0000
#define HSPKTSIZE 512

… … … … …

// write byte(s) to PERIPHERAL, using GPIF and EPxFIFO
void Peripheral_FIFOWrite( BYTE FIFO_EpNum )
{
  while( !( GPIFTRIG & 0x80 ) )  // poll GPIFTRIG.7 Done bit
  {
     ;
  }

  // trigger FIFO write transaction(s), using SFR
  GPIFTRIG = FIFO_EpNum;  // R/W=0, EP[1:0]=FIFO_EpNum for EPx write(s)
}

// Set EP2GPIF Transaction Count
void Peripheral_SetEP2GPIFTC( WORD xfrcnt)
{
  EP2GPIFTCH = xfrcnt >> 8;  // setup transaction count
  EP2GPIFTCL = ( BYTE )xfrcnt;
}
… … … … …
```

Figure 10-42. FIFO-Write Transaction Functions

```
void TD_Init( void )
{
  … … … … …
  GpifInit();  // Configures GPIF from GPIFTool generated waveform data

  // TODO: configure other endpoints, etc. here
  EP2CFG = 0xA2;  // EP2 is DIR=OUT, TYPE=BULK, SIZE=512, BUF=2x
  SYNCDELAY;
  EP2FIFOCFG = 0x00;  // EP2 is AUTOOUT=0, AUTOIN=0, ZEROLEN=0, WORDWIDE=0
  SYNCDELAY;
  // "all" EP2 buffers automatically arm when AUTOOUT=1

  // TODO: arm OUT buffer(s) here
  EP2BCL = 0x80; // write BCL w/skip=1
  SYNCDELAY;
  EP2BCL = 0x80; // write BCL w/skip=1
  SYNCDELAY;

  // setup INT4 as internal source for GPIF interrupts
  // using INT4CLR (SFR), automatically enabled
  //INTSETUP |= 0x03;  //Enable INT4 Autovectoring
  //GPIFIE = 0x03;  // Enable GPIFDONE and GPIFWF interrupt(s)
  //EIE |= 0x04;  // Enable INT4 ISR, EIE.2(EIEX4)=1

  // TODO: configure GPIF interrupt(s) to meet your needs here
     … … … … …

  // tell peripheral we're going into high speed xfr mode
  Peripheral_SetAddress( PERIPHCS );
  Peripheral_SingleByteWrite( P_HSMODE );

  // configure some GPIF control registers
  Peripheral_SetAddress( BURSTMODE );
}
```

Figure 10-43. Initialization Code for FIFO-Write Transactions

```
void TD_Poll( void )
{
  … … … … …
  if( !( EP2468STAT & 0x01 ) )
  { // EP2EF=0 when FIFO "not" empty, host sent pkt.
    EP2BCL = 0x00;  // SKIP=0, pass buffer on to master

    if( gpifdone_event_flag )
    {
      Peripheral_SetEP2GPIFTC( HSPKTSIZE );
      Peripheral_FIFOWrite( GPIF_EP2 );
      gpifdone_event_flag = 0;
    }
  }
  … … … … …
}
```

Figure 10-44. FIFO-Write w/ AUTOOUT = 0, Committing Packets via EPxBCL

10.4.8 Firmware access to OUT packets, (AUTOOUT=1)

To achieve the maximum USB 2.0 bandwidth, the host and master are directly connected when AOUTOOUT=1; the CPU is bypassed and the OUT FIFO is automatically committed to the host:

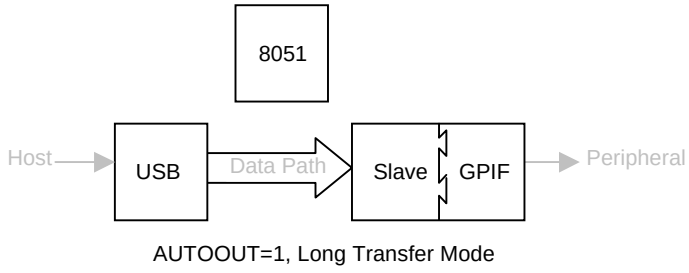


Figure 10-45. CPU not in data path, AUTOOUT=1

```
TD_Init():
… … … … …
REVCTL = 0x03;       // MUST set REVCTL.0 and REVCTL.1 to 1
SYNCDELAY;
EP2CFG = 0xA2;       // EP2 is DIR=OUT, TYPE=BULK, SIZE=512, BUF=2x
SYNCDELAY;
FIFORESET = 0x80;    // Reset the FIFO
SYNCDELAY;
FIFORESET = 0x02;
SYNCDELAY;
FIFORESET = 0x00;
SYNCDELAY;
EP2FIFOCFG = 0x10;   // EP2 is AUTOOUT=1, AUTOIN=0, ZEROLEN=0, WORDWIDE=0
SYNCDELAY;
OUTPKTEND = 0x82;    // Arm both EP2 buffers to “prime the pump”
SYNCDELAY;
OUTPKTEND = 0x82;
… … … … …
```

Figure 10-46. TD_Init Example: Configuring AUTOOUT = 1

```
TD_Poll():
… … … … …
// no code necessary to xfr data from host to master!
// AUTOOUT=1 and SIZE=0 auto commits packets,
// in 512 byte chunks.
… … … … …
```

Figure 10-47. FIFO-Write Transaction Code, AUTOOUT = 1

10.4.9 Firmware access to OUT packets, (AUTOOUT = 0)

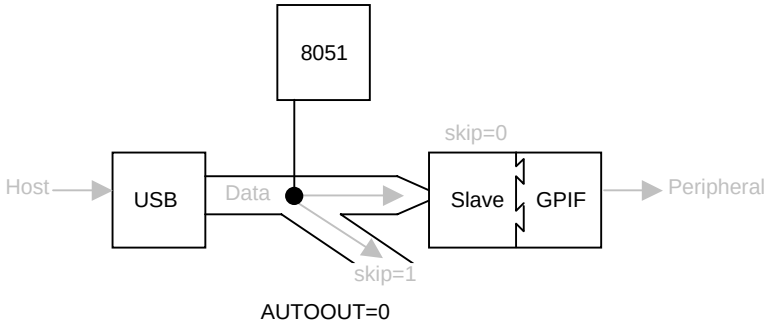


Figure 10-48. Firmware can Skip or Commit, AUTOOUT = 0

```
TD_Init():
… … … … …
EP2CFG = 0xA2;  // EP2 is DIR=OUT, TYPE=BULK, SIZE=512, BUF=2x
SYNCDELAY;
EP2FIFOCFG = 0x00;  // EP2 is AUTOOUT=0, AUTOIN=0, ZEROLEN=0, WORDWIDE=0
SYNCDELAY;
// OUT endpoints do NOT come up armed
EP2BCL = 0x80;  // arm first buffer by writing BC w/skip=1
SYNCDELAY;
EP2BCL = 0x80;  // arm second buffer by writing BC w/skip=1
… … … … …
```

Figure 10-49. Initialization Code for AUTOOUT = 0

In manual OUT mode (AUTOOUT = 0), the firmware has the following options:

1. It can commit (“pass-on”) packet(s) sent from the host to the master when a buffer is available, by writing the OUTPKTEND register with the SKIP bit (OUTPKTEND.7) cleared to 0 (see Figure 10-50).

```
TD_Poll():
… … … … …
if( !( EP24FIFOFLGS & 0x02 ) )
{ // EP2EF=0 when FIFO “not” empty, host sent pkt.
  OUTPKTEND = 0x02;  // SKIP=0, pass buffer on to master
}
… … … … …
```

Figure 10-50. Committing an OUT Packet by Writing OUTPKTEND w/SKIP=0

2. It can skip packet(s) sent from the host to the master by writing the EPxBCL register with the SKIP bit (EPxBCL.7) set to 1 (see Figure 10-51).

```
TD_Poll():
… … … … …
if( !( EP24FIFOFLGS & 0x02 ) )
{ // EP2EF=0 when FIFO “not” empty, host sent pkt.
  OUTPKTEND = 0x82;  // SKIP=1, do NOT pass buffer on to master
}
… … … … …
```

Figure 10-51. Skipping an OUT Packet by Writing OUTPKTEND w/SKIP=1

3. It can *edit* the packet (or *source* an entire OUT packet) by writing to the FIFO buffer directly, then writing the length of the packet to EPxBCH:L. The write to EPxBCL commits the edited packet, so EPxBCL should be written *after* writing EPxBCH (Figure10-52).

In all cases, the OUT buffer automatically re-arms so it can receive the next packet.

See Section 8.6.2.4 for a detailed description of the SKIP bit.

```
TD_Poll():
… … … … …
if( EP24FIFOFLGS & 0x02 )
{
SYNCDELAY;                //
FIFORESET = 0x80;         // nak all OUT pkts. from host
SYNCDELAY;                //
FIFORESET = 0x02;         // advance all EP2 buffers to cpu domain
SYNCDELAY;                //
EP2FIFOBUF[0] = 0xAA;     // create newly sourced pkt. data
SYNCDELAY;                //
EP2BCH = 0x00;
SYNCDELAY;                //
EP2BCL = 0x01;            // commit newly sourced pkt. to interface fifo

// beware of "left over" uncommitted buffers

SYNCDELAY;                //
OUTPKTEND = 0x82;         // skip uncommitted pkt. (second pkt.)
// note: core will not allow pkts. to get out of sequence
SYNCDELAY;                //
FIFORESET = 0x00;         // release "nak all"
}
… … … … …
```

Figure 10-52. Sourcing an OUT Packet (AUTOOUT = 0)

The master is not notified when a packet has been skipped by the firmware.

The OUT FIFO is not committed to the host during a power-on-reset. In its initialization routine, therefore, the firmware should skip *n* packets (where *n* = 2, 3, or 4 depending on the buffering depth) in order to ensure that the entire FIFO is committed to the host. See Figure 10-53.

```
TD_Init():
    … … … … …
    EP2CFG = 0xA2;  // EP2 is DIR=OUT, TYPE=BULK, SIZE=512, BUF=2x
    SYNCDELAY;
    EP2FIFOCFG = 0x00;  // EP2 is AUTOOUT=0, AUTOIN=0, ZEROLEN=0, WORDWIDE=0
    SYNCDELAY;
    // OUT endpoints do NOT come up armed
    EP2BCL = 0x80;  // arm first buffer by writing BC w/skip=1
    SYNCDELAY;
    EP2BCL = 0x80;  // arm second buffer by writing BC w/skip=1
    … … … … …
```

Figure 10-53. Ensuring that the FIFO is Clear after Power-On-Reset

10.4.10 Burst FIFO Transactions

The GPIF can be configured to repeat transactions automatically, with no firmware intervention. These “Burst” transactions (which must always be FIFO-Read or -Write transactions) may be controlled by the Transaction Counter, the GPIF_PF flag, or the GPIFABORT register.

The following C program fragments (Figures 10-54 through 10-57) illustrate how to perform Burst FIFO-Read transactions using GPIF_PF in 8-bit mode (WORDWIDE=0) and AUTOIN=0:

```
#define GPIFTRIGRD 4

#define GPIF_EP2 0
#define GPIF_EP4 1
#define GPIF_EP6 2
#define GPIF_EP8 3

#define BURSTMODE 0x0000
#define HSPKTSIZE 512

… … … … …

// read(s) from PERIPHERAL, using GPIF and EPxFIFO
void Peripheral_FIFORead( BYTE FIFO_EpNum )
{
  while( !( GPIFTRIG & 0x80 ) ) // poll GPIFTRIG.7 GPIF Done bit
  {
     ;
  }

  // trigger FIFO read transaction(s), using SFR
  GPIFTRIG = GPIFTRIGRD | FIFO_EpNum;   // R/W=1, EP[1:0]=FIFO_EpNum
                                        // for EPx read(s)
}

// Set EP8GPIF Transaction Count
void Peripheral_SetEP8GPIFTC( WORD xfrcnt)
{
  EP8GPIFTCH = xfrcnt >> 8;  // setup transaction count
  EP8GPIFTCL = ( BYTE )xfrcnt;
}

… … … … …
```

Figure 10-54. Burst FIFO-Read Transaction Functions

```
void TD_Init( void )
{
  … … … … …
  GpifInit();  // Configures GPIF from GPIFTool generated waveform data

  // TODO: configure other endpoints, etc. here
  EP8CFG = 0xE0;  // EP8 is DIR=IN, TYPE=BULK
  SYNCDELAY;
  EP8FIFOCFG = 0x04;  // EP8 is AUTOOUT=0, AUTOIN=0, ZEROLEN=1, WORDWIDE=0
  SYNCDELAY;

  // TODO: arm OUT buffer(s) here

  // setup INT4 as internal source for GPIF interrupts
  // using INT4CLR (SFR), automatically enabled
  //INTSETUP |= 0x03;  //Enable INT4 Autovectoring
  //SYNCDELAY;
  //GPIFIE = 0x03;  // Enable GPIFDONE and GPIFWF interrupt(s)
  //SYNCDELAY;
  //EIE |= 0x04;  // Enable INT4 ISR, EIE.2(EIEX4)=1

  // TODO: configure GPIF interrupt(s) to meet your needs here
     … … … … …

  // tell peripheral we're going into high speed xfr mode
  Peripheral_SetAddress( PERIPHCS );
  Peripheral_SingleByteWrite( P_HSMODE );

  // configure some GPIF registers
  Peripheral_SetAddress( BURSTMODE );
}
```

Figure 10-55. Initialization for Burst FIFO-Read Transactions

```
void TD_Poll( void )
{
  … … … … …
  if( ibn_event_flag )
  { // host is asking for EP8 data
    Peripheral_SetEP8GPIFTC( HSPKTSIZE );
    Peripheral_FIFORead( GPIF_EP8 );
    ibn_event_flag = 0;
  }

  if( gpifdone_event_flag )
  { // GPIF currently pointing to EP8, last FIFO accessed
    if( !( EP2468STAT & 0x80 ) )
    { // EP8F=0 when buffer available
      INPKTEND = 0x08;  // Firmware commits pkt
                        // by writing #8 to INPKTEND
      gpifdone_event_flag = 0;
    }
  }

  // decide how GPIF transitions to DONE for FIFO Transactions
  if( gpif_pf_event_flag )
  {
    EP8GPIFPFSTOP = 0x01;  // set bit0=1 to use GPIF_PF
  }
  else
  {
    EP8GPIFPFSTOP = 0x00;  // set bit0=0 to use TC
  }
  … … … … …
}
```

Figure 10-56. Burst FIFO-Read Transaction Example, Writing INPKTEND w/SKIP=0 to Commit

```
void TD_Poll( void )
{
  … … … … …
  if( !( EP68FIFOFLGS & 0x10 ) )
  { // EP8FF=0 when buffer available
  // host is taking EP8 data fast enough
    Peripheral_SetEP8GPIFTC( HSPKTSIZE );
    Peripheral_FIFORead( GPIF_EP8 );
  }

  if( gpifdone_event_flag )
  { // GPIF currently pointing to EP8, last FIFO accessed
    if( !( EP2468STAT & 0x80 ) )
    { // EP8F=0 when buffer available
      // modify the data
      EP8FIFOBUF[ 0 ] = 0x02;  // <STX>, packet start of text msg
      EP8FIFOBUF[ 7 ] = 0x03;  // <ETX>, packet end of text msg
      SYNCDELAY;
      EP8BCH = 0x00;
      SYNCDELAY;
      EP8BCL = 0x08;  // pass buffer on to host
    }
  }

 // decide how GPIF transitions to DONE for FIFO Transactions
  if( gpif_pf_event_flag )
  {
    EP8GPIFPFSTOP = 0x01;  // set bit0=1 to use GPIF_PF
  }
  else
  {
    EP8GPIFPFSTOP = 0x00;  // set bit0=0 to use TC
  }
  … … … … …
}
```

Figure 10-57. Burst FIFO-Read Transaction Example, Writing EPxBCL to Commit

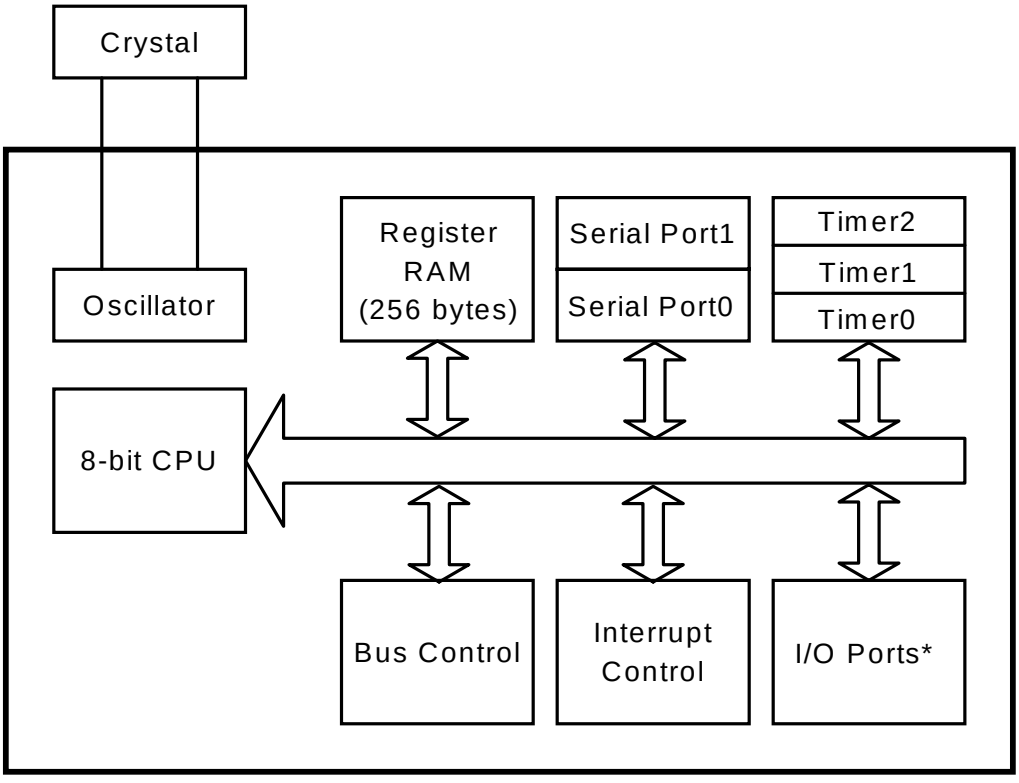
10.5 UDMA Interface

The FX2 has additional GPIF registers specifically for implementing a UDMA (Ultra-ATA) interface. For more information, please contact the Cypress Semiconductor Applications Department.

Chapter 11 CPU Introduction

11.1 Introduction

The FX2's CPU, an enhanced 8051, is fully described in *Chapter 12, "Instruction Set"*, *Chapter 13, "Input/Output"*, and *Chapter 14, "Timers/Counters and Serial Interface"*. This chapter introduces the processor, its interface to the FX2 logic, and describes architectural differences from a standard 8051. Figure 11-1 is a block diagram of the FX2's 8051-based CPU.



* The EZ-USB family implements I/O ports differently than in the standard 8051

Figure 11-1. FX2 CPU Features

11.2 8051 Enhancements

The FX2 uses the standard 8051 instruction set, so it's supported by industry-standard 8051 compilers and assemblers. Instructions execute faster on the FX2 than on the standard 8051:

- Wasted bus cycles are eliminated; an instruction cycle uses only four clocks, rather than the standard 8051's 12 clocks.
- The FX2's CPU clock runs at 12MHz, 24MHz, or 48MHz —up to four times the clock speed of the standard 8051.

In addition to speed improvements, the FX2 includes the following architectural enhancements to the CPU:

- A second data pointer
- A second USART
- A third, 16-bit timer (TIMER2)
- A high-speed external memory interface with a non-multiplexed 16-bit address bus
- Eight additional interrupts (INT2-INT6, WAKEUP, T2, and USART1)
- Variable MOVX timing to accommodate fast and slow RAM peripherals
- Two Autopointers (auto-incrementing data pointers)
- Vectored USB and FIFO/GPIF interrupts
- Baud rate timer for 115K/230K baud USART operation
- Sleep mode with three wakeup sources
- An I²C-compatible bus controller that runs at 100 or 400 KHz
- FX2-specific SFRs
- Separate buffers for the SETUP and DATA portions of a USB CONTROL transfer
- A hardware pointer for SETUP data, plus logic to process entire CONTROL transfers automatically
- CPU clock-rate selection of 12, 24 or 48MHz
- Breakpoint facility
- I/O Port C read and write strobes

11.3 Performance Overview

The FX2 has been designed to offer increased performance by executing instructions in a 4-clock bus cycle, as opposed to the 12-clock bus cycle in the standard 8051 (see Figure 11-2). This shortened bus timing improves the instruction execution rate for most instructions by a factor of three over the standard 8051 architectures.

Some instructions require a different number of instruction cycles on the FX2 than they do on the standard 8051. In the standard 8051, all instructions except for MUL and DIV take one or two instruction cycles to complete. In the FX2, instructions can take between one and five instruction cycles to complete. However, due to the shortened bus timing of the FX2, every instruction executes faster than on a standard 8051, and the average speed improvement over the entire instruction set is approximately 2.5×. Table 11-1 catalogs the speed improvements.

Table 11-1. FX2 Speed Compared to Standard 8051

Of the 246 FX2 opcodes...	
150 execute at	3.0× standard speed
51 execute at	1.5× standard speed
43 execute at	2.0× standard speed
2 execute at	2.4× standard speed
Average Improvement:	**2.5×**

Note: Comparison is between FX2 and standard 8051 running at the same clock frequency.

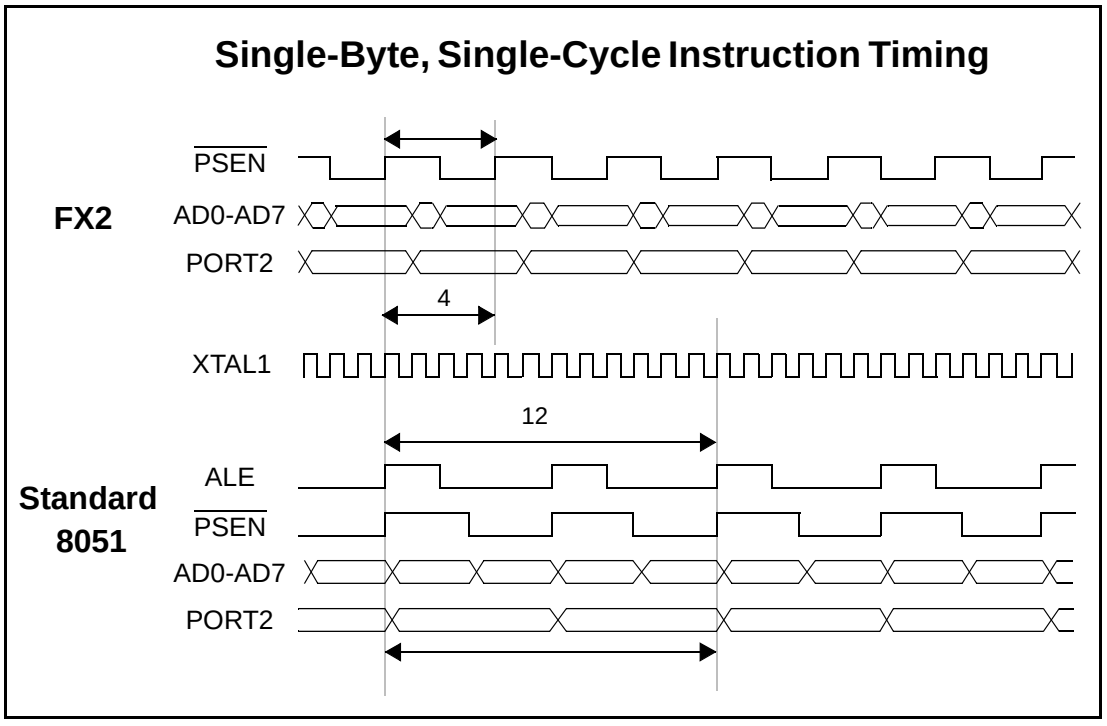


Figure 11-2. FX2 to Standard 8051 Timing Comparison

11.4 Software Compatibility

The FX2 is object-code-compatible with the industry-standard 8051 microcontroller. That is, object code compiled with an industry-standard 8051 compiler or assembler executes on the FX2 and is functionally equivalent. However, because the FX2 uses a different instruction timing than the standard 8051, existing code with timing loops may require modification.

The FX2 instruction timing is identical to that of the Dallas Semiconductor DS80C320.

11.5 803x/805x Feature Comparison

Table 11-2 provides a feature-by-feature comparison between the FX2 and several common 803x/805x devices.

Table 11-2. Comparison Between FX2 and Other 803x/805x Devices

Feature	Intel				Dallas DS80C320	Cypress FX2
	8031	8051	80C32	80C52		
Clocks per instruction cycle	12	12	12	12	4	4
Program / Data Memory	-	4 KB ROM	-	8 KB ROM	-	8 KB RAM
Internal RAM	128 bytes	128 bytes	256 bytes	256 bytes	256 bytes	256 bytes
Data Pointers	1	1	1	1	2	2
Serial Ports	1	1	1	1	2	2
16-bit Timers	2	2	3	3	3	3
Interrupt sources (internal and external)	5	5	6	6	13	13
Stretch data-memory cycles	no	no	no	no	yes	yes

11.6 FX2/DS80C320 Differences

Although the FX2 is similar to the DS80C320 in terms of hardware features and instruction cycle timing, there are some important differences between the FX2 and the DS80C320.

11.6.1 Serial Ports

The FX2 does not implement serial port framing-error detection and does not implement slave address comparison for multiprocessor communications. Therefore, the FX2 also does not implement the following SFRs: SADDR0, SADDR1, SADEN0, and SADEN1.

11.6.2 Timer 2

The FX2 does not implement Timer 2 downcounting mode or the downcount enable bit (TMOD2, Bit 0). Also, the FX2 does not implement Timer 2 output enable (T2OE) bit (TMOD2, Bit 1). Therefore, the TMOD2 SFR is also not implemented in the FX2.

The FX2 Timer 2 overflow output is active for one clock cycle. In the DS80C320, the Timer 2 overflow output is a square wave with a 50% duty cycle.

Although the T2OE bit is not present in the FX2, Timer 2 output can still be enabled or disabled via the PORTECFG.2 bit, since the T2OUT pin is multiplexed with PORTE.2.

PORTECFG.2=0 configures the pin as a general-purpose I/O pin and disabled Timer 2 output; PORTECFG.2=1 configures the pin as the T2OUT pin and enables Timer 2 output.

11.6.3 Timed Access Protection

The FX2 does not implement timed access protection and, therefore, does not implement the TA SFR.

11.6.4 Watchdog Timer

The FX2 does not implement a watchdog timer.

11.6.5 Power Fail Detection

The FX2 does not implement a power fail detection circuit.

11.6.6 Port I/O

The FX2's port I/O implementation is significantly different from that of the DS80C320, mainly because of the alternate functions shared with most of the I/O pins. See *Chapter 13, "Input/Output"*.

11.6.7 Interrupts

Although the basic interrupt structure of the FX2 is similar to that of the DS80C320, five of the interrupt sources are different:

Table 11-3. Differences between FX and DS80C320 Interrupts

Interrupt Priority	Dallas DS80C320	Cypress FX2
0	Power Fail	RESUME (USB Wakeup)
8	External Interrupt 2	USB
9	External Interrupt 3	I²C-Compatible Bus
10	External Interrupt 4	GPIF/FIFOs
12	Watchdog Timer	External Interrupt 6

For more information, refer to *Chapter 14, "Timers/Counters and Serial Interface"*.

11.7 EZ-USB FX2 Register Interface

The FX2 peripheral logic (USB, GPIF, FIFOs, etc.) is controlled via a set of memory mapped registers and buffers at addresses 0xE400 through 0xFFFF. These registers and buffers are grouped as follows:

- GPIF Waveform Descriptor Tables
- General configuration
- Endpoint configuration
- Interrupts
- Input/Output
- USB Control
- Endpoint operation
- GPIF/FIFOs
- Endpoint buffers

These registers and their functions are described throughout this manual. A full description of every FX2 register appears in *Chapter 15, "Registers"*

11.8 EZ-USB FX2 Internal RAM

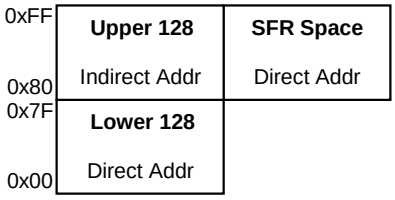


Figure 11-1. FX2 Internal Data RAM

Like the standard 8051, the FX2 contains 128 bytes of Internal Data RAM at addresses 0x00-0x7F and a partially populated SFR space at addresses 0x80-0xFF. An additional 128 indirectly-addressed bytes of Internal Data RAM (sometimes called “IDATA”) are also available at addresses 0x80-0xFF.

All other on-chip FX2 RAM (program/data memory, endpoint buffer memory, and the FX2 control registers) is addressed as though it were *off-chip* 8051 memory. FX2 firmware reads or writes these bytes as data using the MOVX (“move external”) instruction, even though the FX2 RAM and register set is actually inside the EZ-USB FX2 chip. Off-chip memory attached to the FX2 address and data buses (CY7C68013-128NC only) can also be accessed by the MOVX instruction. FX2 logic encodes its memory strobe and select signals ($\overline{RD}$, $\overline{WR}$, $\overline{CS}$, $\overline{OE}$, and $\overline{PSEN}$) to eliminate the need for external logic to separate the on-chip and off-chip memory spaces; see *Chapter 5, "Memory"*.

11.9 I/O Ports

The FX2 implements I/O ports differently than a standard 8051, as described in *Chapter 13, "Input/Output"*.

The FX2 has up to five 8-bit wide, bidirectional I/O ports. Each port is associated with a pair of registers:

- An “OEx” register, which sets the input/output direction of each of the 8 port pins (0 = input, 1 = output).
- An “IOx” register. Values written to IOx appear on the pins configured as outputs; values read from IOx indicate the states of the 8 pins, regardless of input/output configuration.

Most I/O pins have alternate functions which are selected using configuration registers. When an alternate configuration is selected for an I/O pin, the corresponding OEx bit is ignored (see *Section 13.2*). The default (power-on reset) state of all I/O ports is: alternate configurations *off*, all I/O pins configured as *inputs*.

11.10 Interrupts

All standard 8051 interrupts, plus additional interrupts, are supported by the FX2. Tabl e11-4 lists the FX2 interrupts.

Table 11-4. EZ-USB FX2 Interrupts

Standard 8051 Interrupts	Additional FX2 Interrupts	Source
INT0		Pin PA0 / $\overline{\text{INT0}}$
INT1		Pin PA1 / $\overline{\text{INT1}}$
Timer 0		Internal, Timer 0
Timer 1		Internal, Timer 1
Tx0 & Rx0		Internal, USART0
	INT2	Internal, USB
	INT3	Internal, I²C-Compatible Bus Controller
	INT4	Pin INT4 (100- and 128-pin only) **OR** Internal, GPIF/FIFOs
	INT5	Pin $\overline{\text{INT5}}$ (100- and 128-pin only)
	INT6	Pin INT6 (100- and 128-pin only)
	WAKEUP	Pin WAKEUP or Pin RA3/WU2
	Tx1 & Rx1	Internal, USART1
	Timer 2	Internal, Timer 2

The FX2 uses INT2 for 27 different USB interrupts. To help determine which interrupt is active, the FX2 provides a feature called Autovectoring, which dynamically changes the address pointed to by the “jump” instruction at the INT2 vector address. This second level of vectoring automatically transfers control to the appropriate USB interrupt service routine (ISR). The FX2 interrupt system, including a full description of the Autovector mechanism, is the subject of *Chapter 4, "Interrupts"*.

11.11 Power Control

The FX2 implements a low-power mode that allows it to be used in USB bus-powered devices (which are required by the USB specification to draw no more than 500 µA when suspended) and other low-power applications. The mechanism by which the FX2 enters and exits this low-power mode is described in detail in *Chapter 6, "Power Management"*.

11.12 Special Function Registers (SFR)

The FX2 was designed to keep coding as standard as possible, to allow easy integration of existing 8051 software development tools. The FX2 SFR registers are summarized in Tabl e11-5. Standard 8051 SFRs are shown in normal type and FX2-added SFRs are shown in bold type. Full details of the SFRs can be found in *Chapter 15, "Registers"*.

Table 11-5. FX2 Special Function Registers (SFR)

x	8x	9x	Ax	Bx	Cx	Dx	Ex	Fx
0	**IOA**	**IOB**	**IOC**	**IOD**	**SCON1**	PSW	ACC	B
1	SP	**EXIF**	**INT2CLR**	**IOE**	**SBUF1**			
2	DPL0	**MPAGE**	**INT4CLR**	**OEA**				
3	DPH0			**OEB**				
4	**DPL1**			**OEC**				
5	**DPH1**			**OED**				
6	**DPS**			**OEE**				
7	PCON							
8	TCON	SCON0	**IE**	**IP**	**T2CON**	**EICON**	**EIE**	**EIP**
9	TMOD	SBUF0						
A	TL0	**AUTOPTRH1**	**EP2468STAT**	**EP01STAT**	**RCAP2L**			
B	TL1	**AUTOPTRL1**	**EP24FIFOFLGS**	**GPIFTRIG**	**RCAP2H**			
C	TH0		**EP68FIFOFLGS**		**TL2**			
D	TH1	**AUTOPTRH2**		**GPIFSGLDATH**	**TH2**			
E	**CKCON**	**AUTOPTRL2**		**GPIFSGLDATLX**				
F			**AUTOPTRSETUP**	**GPIFSGLDATLNOX**				

All unlabed SFRs are reserved.

11.13 External Address/Data Buses

The 128-pin version of the FX2 provides external, non-multiplexed 16-bit address and 8-bit data buses. This differs from the standard 8051, which multiplexes eight pins among three sources: I/O port 0, the external data bus, and the low byte of the external address bus.

A standard 8051 system with external memory requires a demultiplexing address latch, strobed by the 8051 ALE (Address Latch Enable) pin. The external latch is not required by the FX2 chip, and no ALE signal is provided. In addition to eliminating the need for this external latch, the non-multiplexed FX2 bus saves one cycle per memory-fetch and allows external memory to be connected without sacrificing I/O pins.

The FX2 is the sole master of the bus, providing read and write signals to the off-chip memory. The address bus is output-only, and cannot be floated.

11.14 Reset

The various FX2 resets and their effects are described in *Chapter 7, "Resets"*.

Chapter 12 Instruction Set

12.1 Introduction

This chapter provides a technical overview and description of the FX2's assembly-language instruction set.

All FX2 instructions are binary-code-compatible with the standard 8051. The FX2 instructions affect bits, flags, and other status functions just as the 8051 instructions do. Instruction timing, however, is different both in terms of the number of clock cycles per instruction cycle and the number of instruction cycles used by each instruction.

Table 12-2 lists the FX2 instruction set and the number of instruction cycles required to complete each instruction. Table 12-1 defines the symbols and mnemonics used in Table 12-2.

Table 12-1. Legend for Instruction Set Table

Symbol	Function
A	Accumulator
Rn	Register (R0–R7, in the bank selected by RS1:RS0)
direct	Internal RAM location (0x00 - 0x7F in the "Lower 128", or 0x80 - 0xFF in "SFR" space)
@Ri	Internal RAM location (0x00 - 0x7F in the "Lower 128", or 0x80 - 0xFF in the "Upper 128") pointed to by R0 or R1
rel	Program-memory offset (-128 to +127 bytes relative to the first byte of the following instruction). Used by conditional jumps and SJMP.
bit	Bit address (0x20 - x2F in the "Lower 128," and SFRs 0x80, 0x88, ..., 0xF0, 0xF8)
#data	8-bit constant (0 - 255)
#data16	16-bit constant (0 - 65535)
addr16	16-bit destination address; used by LCALL and LJMP, which branch anywhere in program memory
addr11	11-bit destination address; used by ACALL and AJMP, which branch only within the current 2K page of program memory (i.e., the upper 5 address bits are copied from the PC)
PC	Program Counter; holds the address of the currently-executing instruction. For the purposes of "ACALL", "AJMP", and "MOVC A,@A+PC" instructions, the PC holds the address of the first byte of the instruction *following* the currently-executing instruction.

Table 12-2. FX2 Instruction Set

Mnemonic	Description	Bytes	Cycles	PSW Flags Affected	Opcode (Hex)
Arithmetic					
ADD A, Rn	Add register to A	1	1	CY OV AC	28-2F
ADD A, direct	Add direct byte to A	2	2	CY OV AC	25
ADD A, @Ri	Add data memory to A	1	1	CY OV AC	26-27
ADD A, #data	Add immediate to A	2	2	CY OV AC	24
ADDC A, Rn	Add register to A with carry	1	1	CY OV AC	38-3F
ADDC A, direct	Add direct byte to A with carry	2	2	CY OV AC	35
ADDC A, @Ri	Add data memory to A with carry	1	1	CY OV AC	36-37
ADDC A, #data	Add immediate to A with carry	2	2	CY OV AC	34
SUBB A, Rn	Subtract register from A with borrow	1	1	CY OV AC	98-9F
SUBB A, direct	Subtract direct byte from A with borrow	2	2	CY OV AC	95
SUBB A, @Ri	Subtract data memory from A with borrow	1	1	CY OV AC	96-97
SUBB A, #data	Subtract immediate from A with borrow	2	2	CY OV AC	94
INC A	Increment A	1	1		04
INC Rn	Increment register	1	1		08-0F
INC direct	Increment direct byte	2	2		05
INC @ Ri	Increment data memory	1	1		06-07
DEC A	Decrement A	1	1		14
DEC Rn	Decrement Register	1	1		18-1F
DEC direct	Decrement direct byte	2	2		15
DEC @Ri	Decrement data memory	1	1		16-17
INC DPTR	Increment data pointer	1	3		A3
MUL AB	Multiply A and B (unsigned; product in B:A)	1	5	CY=0 OV	A4
DIV AB	Divide A by B (unsigned; quotient in A, remainder in B)	1	5	CY=0 OV	84
DA A	Decimal adjust A	1	1	CY	D4
Logical					
ANL, Rn	AND register to A	1	1		58-5F
ANL A, direct	AND direct byte to A	2	2		55
ANL A, @Ri	AND data memory to A	1	1		56-57
ANL A, #data	AND immediate to A	2	2		54
ANL direct, A	AND A to direct byte	2	2		52
ANL direct, #data	AND immediate data to direct byte	3	3		53
ORL A, Rn	OR register to A	1	1		48-4F
ORL A, direct	OR direct byte to A	2	2		45
ORL A, @Ri	OR data memory to A	1	1		46-47
ORL A, #data	OR immediate to A	2	2		44

Table 12-2. FX2 Instruction Set (Continued)

Mnemonic	Description	Bytes	Cycles	PSW Flags Affected	Opcode (Hex)
ORL direct, A	OR A to direct byte	2	2		42
ORL direct, #data	OR immediate data to direct byte	3	3		43
XRL A, Rn	Exclusive-OR register to A	1	1		68-6F
XRL A, direct	Exclusive-OR direct byte to A	2	2		65
XRL A, @Ri	Exclusive-OR data memory to A	1	1		66-67
XRL A, #data	Exclusive-OR immediate to A	2	2		64
XRL direct, A	Exclusive-OR A to direct byte	2	2		62
XRL direct, #data	Exclusive-OR immediate to direct byte	3	3		63
CLR A	Clear A	1	1		E4
CPL A	Complement A	1	1		F4
SWAP A	Swap nibbles of a	1	1		C4
RL A	Rotate A left	1	1		23
RLC A	Rotate A left through carry	1	1	CY	33
RR A	Rotate A right	1	1		03
RRC A	Rotate A right through carry	1	1	CY	13
Data Transfer					
MOV A, Rn	Move register to A	1	1		E8-EF
MOV A, direct	Move direct byte to A	2	2		E5
MOV A, @Ri	Move data byte at Ri to A	1	1		E6-E7
MOV A, #data	Move immediate to A	2	2		74
MOV Rn, A	Move A to register	1	1		F8-FF
MOV Rn, direct	Move direct byte to register	2	2		A8-AF
MOV Rn, #data	Move immediate to register	2	2		78-7F
MOV direct, A	Move A to direct byte	2	2		F5
MOV direct, Rn	Move register to direct byte	2	2		88-8F
MOV direct, direct	Move direct byte to direct byte	3	3		85
MOV direct, @Ri	Move data byte at Ri to direct byte	2	2		86-87
MOV direct, #data	Move immediate to direct byte	3	3		75
MOV @Ri, A	MOV A to data memory at address Ri	1	1		F6-F7
MOV @Ri, direct	Move direct byte to data memory at address Ri	2	2		A6-A7
MOV @Ri, #data	Move immediate to data memory at address Ri	2	2		76-77
MOV DPTR, #data16	Move 16-bit immediate to data pointer	3	3		90
MOVC A, @A+DPTR	Move code byte at address DPTR+A to A	1	3		93
MOVC A, @A+PC	Move code byte at address PC+A to A	1	3		83
MOVX A, @Ri	Move external data at address Ri to A	1	2-9*		E2-E3
MOVX A, @DPTR	Move external data at address DPTR to A	1	2-9*		E0

Table 12-2. FX2 Instruction Set (Continued)

Mnemonic	Description	Bytes	Cycles	PSW Flags Affected	Opcode (Hex)
MOVX @Ri, A	Move A to external data at address Ri	1	2-9*		F2-F3
MOVX @DPTR, A	Move A to external data at address DPTR	1	2-9*		F0
PUSH direct	Push direct byte onto stack	2	2		C0
POP direct	Pop direct byte from stack	2	2		D0
XCH A, Rn	Exchange A and register	1	1		C8-CF
XCH A, direct	Exchange A and direct byte	2	2		C5
XCH A, @Ri	Exchange A and data memory at address Ri	1	1		C6-C7
XCHD A, @Ri	Exchange the low-order nibbles of A and data memory at address Ri	1	1		D6-D7
** Number of cycles is user-selectable. See Section 12.1.2, "Stretch Memory Cycles (Wait States)".*					
Boolean					
CLR C	Clear carry	1	1	CY=0	C3
CLR bit	Clear direct bit	2	2		C2
SETB C	Set carry	1	1	CY=1	D3
SETB bit	Set direct bit	2	2		D2
CPL C	Complement carry	1	1	CY	B3
CPL bit	Complement direct bit	2	2		B2
ANL C, bit	AND direct bit to carry	2	2	CY	82
ANL C, /bit	AND inverse of direct bit to carry	2	2	CY	B0
ORL C, bit	OR direct bit to carry	2	2	CY	72
ORL C, /bit	OR inverse of direct bit to carry	2	2	CY	A0
MOV C, bit	Move direct bit to carry	2	2	CY	A2
MOV bit, C	Move carry to direct bit	2	2		92
Branching					
ACALL addr11	Absolute call to subroutine	2	3		11-F1
LCALL addr16	Long call to subroutine	3	4		12
RET	Return from subroutine	1	4		22
RETI	Return from interrupt	1	4		32
AJMP addr11	Absolute jump unconditional	2	3		01-E1
LJMP addr16	Long jump unconditional	3	4		02
SJMP rel	Short jump (relative address)	2	3		80
JC rel	Jump if carry = 1	2	3		40
JNC rel	Jump if carry = 0	2	3		50
JB bit, rel	Jump if direct bit = 1	3	4		20
JNB bit, rel	Jump if direct bit = 0	3	4		30
JBC bit, rel	Jump if direct bit = 1, then clear the bit	3	4		10
JMP @ A+DPTR	Jump indirect to address DPTR+A	1	3		73

Table 12-2. FX2 Instruction Set (Continued)

Mnemonic	Description	Bytes	Cycles	PSW Flags Affected	Opcode (Hex)
JZ rel	Jump if accumulator = 0	2	3		60
JNZ rel	Jump if accumulator is non-zero	2	3		70
CJNE A, direct, rel	Compare A to direct byte; jump if not equal	3	4	CY	B5
CJNE A, #d, rel	Compare A to immediate; jump if not equal	3	4	CY	B4
CJNE Rn, #d, rel	Compare register to immediate; jump if not equal	3	4	CY	B8-BF
CJNE @ Ri, #d, rel	Compare data memory to immediate; jump if not equal	3	4	CY	B6-B7
DJNZ Rn, rel	Decrement register; jump if not zero	2	3		D8-DF
DJNZ direct, rel	Decrement direct byte; jump if not zero	3	4		D5
Miscellaneous					
NOP	No operation	1	1		00
There is an additional reserved opcode (A5) that performs the same function as NOP. All mnemonics are copyright 1980, Intel Corporation.					

12.1.1 Instruction Timing

Instruction cycles in the FX2 are 4 clock cycles in length, as opposed to the 12 clock cycles per instruction cycle in the standard 8051. For full details of the instruction-cycle timing differences between the FX2 and the standard 8051, see *Section 11.3, "Performance Overview"*.

In the standard 8051, all instructions except for MUL and DIV take one or two instruction cycles to complete. In the FX2, instructions can take between one and five instruction cycles to complete. For calculating the timing of software loops, etc., use the “Cycles” column from Table 12-2. The “Bytes” column indicates the number of bytes occupied by each instruction.

By default, the FX2’s timer/counters run at 12 clock cycles per increment so that timer-based events have the same timing as with the standard 8051. The timers can also be configured to run at 4 clock cycles per increment to take advantage of the higher speed of the FX2’s CPU.

12.1.2 Stretch Memory Cycles (Wait States)

The FX2 can execute a MOVX instruction in as few as 2 instruction cycles. However, it is sometimes desirable to stretch this value (for example to access slow memory or slow memory-mapped peripherals such as USARTs or LCDs). The FX2’s “stretch memory cycle” feature enables FX2 firmware to adjust the speed of *data memory* accesses (program-memory code fetches are not affected).

The three LSBs of the Clock Control Register (CKCON, at SFR location 0x8E) control the stretch value; stretch values between zero and seven may be used. A stretch value of zero adds zero instruction cycles, resulting in MOVX instructions which execute in two instruction cycles. A stretch value of seven adds seven instruction cycles, resulting in MOVX instructions which execute in nine instruction cycles. The stretch value can be changed dynamically under program control.

At power-on-reset, the stretch value defaults to one (three-cycle MOVX); for the fastest data memory access, FX2 software must explicitly set the stretch value to zero. The stretch value affects only data memory access (*not* program memory).

The stretch value affects the width of the read/write strobe and all related timing. Using a higher stretch value results in a wider read/write strobe, which allows the memory or peripheral more time to respond.

Table 12-3 lists the data memory access speeds for stretch values zero through seven. MD2-0 are the three LSBs of the Clock Control Register (CKCON.2-0). The strobe width timing shown is typical.

CPUCS.4:3 sets the basic clock reference for the FX2. These bits can be modified by FX2 firmware at any time. At power-on-reset, CPUCS.4:3 is set to ‘00’ (12 Mhz).

Table 12-3. Data Memory Stretch Values

MD2	MD1	MD0	MOVX Instruction Cycles	Read/Write Strobe Width (Clocks)	Strobe Width @ 12MHz CPUCS.4:3 = 00	Strobe Width @ 24MHz CPUCS.4:3 = 01	Strobe Width @ 48MHz CPUCS.4:3 = 10
0	0	0	2	2	167 ns	83.3 ns	41.7 ns
0	0	1	3 (default)	4	333 ns	167 ns	83.3 ns
0	1	0	4	8	667 ns	333 ns	167 ns
0	1	1	5	12	1000 ns	500 ns	250 ns
1	0	0	6	16	1333 ns	667 ns	333 ns
1	0	1	7	20	1667 ns	833 ns	417 ns
1	1	0	8	24	2000 ns	1000 ns	500 ns
1	1	1	9	28	2333 ns	1167 ns	583 ns

12.1.3 Dual Data Pointers

The FX2 employs dual data pointers to accelerate data memory block moves. The standard 8051 data pointer (DPTR) is a 16-bit pointer used to address external data RAM or peripherals. The FX2 maintains the standard data pointer as DPTR0 at the standard SFR locations 0x82 (DPL0) and 0x83 (DPH0); it is not necessary to modify existing code to use DPTR0.

The FX2 adds a second data pointer (DPTR1) at SFR locations 0x84 (DPL1) and 0x85 (DPH1). The SEL bit (bit 0 of the DPTR Select Register, DPS, at SFR 0x86), selects the active pointer. When SEL = 0, instructions that use the DPTR will use DPL0:DPH0. When SEL = 1, instructions that use the DPTR will use DPL1:DPH1. No other bits of the DPS SFR are used.

All DPTR-related instructions use the data pointer selected by the SEL Bit. Switching between the two data pointers by toggling the SEL bit relieves FX2 firmware from the burden of saving source and destination addresses when doing a block move; therefore, using dual data pointers provides significantly increased efficiency when moving large blocks of data.

The fastest way to toggle the SEL bit between the two data pointers is via the “INC DPS” instruction, which toggles bit 0 of DPS between 0 and 1.

The SFR locations related to the dual data pointers are:

0x82	DPL0	DPTR0 low byte
0x83	DPH0	DPTR0 high byte
0x84	DPL1	DPTR1 low byte
0x85	DPH1	DPTR1 high byte
0x86	DPS	DPTR Select (Bit 0)

12.1.4 Special Function Registers

The four SFRs listed below are related to CPU operation and program execution. Except for the Stack Pointer SP, each of the registers is bit addressable.

0x81	SP	Stack Pointer
0xD0	PSW	Program Status Word
0xE0	ACC	Accumulator Register
0xF0	B	B Register

Table 12-4 lists the functions of the PSW bits.

Table 12-4. PSW Register - SFR 0xD0

Bit	Function
PSW.7	**CY** - Carry flag. This is the **unsigned** carry bit. The CY flag is set when an arithmetic operation results in a carry from bit 7 to bit 8, and cleared otherwise. In other words, it acts as a virtual bit 8. The CY flag is cleared on multiplication and division. See the “PSW Flags Affected” column in Table 12-2.
PSW.6	**AC** - Auxiliary carry flag. Set to 1 when the last arithmetic operation resulted in a carry into (during addition) or borrow from (during subtraction) the high order nibble, otherwise cleared to 0 by all arithmetic operations. See the “PSW Flags Affected” column in Table 12-2.
PSW.5	**F0** - User flag 0. Available to FX2 firmware for general purpose.
PSW.4 PSW.3	**RS1** - Register bank select bit 1. **RS0** - Register bank select bit 0. RS1:RS0 select a register bank in internal RAM: RS1 RS0 Bank Selected 0 0 Register bank 0, addresses 0x00-0x07 0 1 Register bank 1, addresses 0x08-0x0F 1 0 Register bank 2, addresses 0x10-0x17 1 1 Register bank 3, addresses 0x18-0x1F
PSW.2	**OV** - Overflow flag. This is the **signed** carry bit. The OV flag is set when a positive sum exceeds 0x7F or a negative sum (in two’s complement notation) exceeds 0x80. After a multiply, OV = 1 if the result of the multiply is greater than 0xFF. After a divide, OV = 1 if a divide-by-0 occurred. See the “PSW Flags Affected” column in Table 12-2.
PSW.1	**F1** - User flag 1. Available to FX2 firmware for general purpose.
PSW.0	**P** - Parity flag. Contains the modulo-2 sum of the 8 bits in the accumulator (i.e., set to 1 when the accumulator contains an odd number of “1” bits, set to 0 when the accumulator contains an even number of “1” bits).

Chapter 13 Input/Output

13.1 Introduction

The 56-pin FX2 package provides two input-output systems:

- A set of programmable I/O pins
- A programmable I²C-compatible bus controller

The 100- and 128-pin packages additionally provide two programmable USARTs, which are fully described in *Chapter 14, "Timers/Counters and Serial Interface."*

The I/O pins may be configured either for general-purpose I/O or for alternate functions (GPIF address and data; FIFO data; USART, timer, and interrupt signals; etc.). This chapter describes the usage of the pins in the general-purpose configuration, and the methods by which the pins may be configured for alternate functions.

This chapter also provides both the programming information for the I²C-compatible interface and the operating details of the EEPROM boot loader. The role of the boot loader is described in *Chapter 3, "Enumeration and ReNumeration™"*.

13.2 I/O Ports

The FX2's I/O ports are implemented differently than those of a standard 8051.

The FX2 has up to five eight-pin bidirectional I/O ports, labeled A, B, C, D, and E. Individual I/O pins are labeled P*x.n*, where *x* is the port (A, B, C, D, or E) and *n* is the pin number (0 to 7).

The 100- and 128-pin FX2 packages provide all five ports; the 56-pin package provides only ports A, B, and D.

Each port is associated with a pair of registers:

- An OE*x* register (where *x* is A, B, C, D, or E), which sets the input/output direction of each of the 8 pins (0 = input, 1 = output). See Figure 13-2.
- An IO*x* register (where *x* is A, B, C, D, or E). Values written to IO*x* appear on the pins which are configured as outputs; values read from IO*x* indicate the states of the 8 pins, regardless of input/output configuration. See Figure 13-3.

Most I/O pins have alternate functions which may be selected using configuration registers (see Tables 13-1 through 13-9). Each alternate function is unidirectional; the FX2 “knows” whether the function is an input or an output, so when an alternate configuration is selected for an I/O pin, the corresponding OE*x* bit is ignored (see Figures 13-4 and 13-5).

The default (power-on reset) state of all I/O ports is:

- Alternate configurations *off*
- All I/O pins configured as *inputs*

Figure 13-1 shows the basic structure of an FX2 I/O pin.

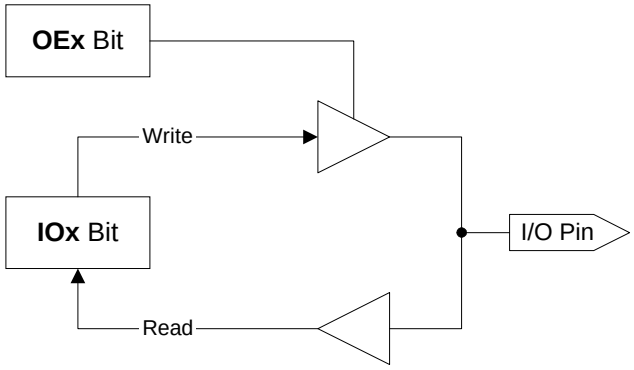


Figure 13-1. FX2 I/O Pin

OEA	Port A Output Enable						SFR 0xB2
b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

OEB	Port B Output Enable						SFR 0xB3
b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

OEC	Port C Output Enable						SFR 0xB4
b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

OED	Port D Output Enable						SFR 0xB5
b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

OEE	Port E Output Enable						SFR 0xB6
b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Figure 13-2. I/O Port Output-Enable Registers

IOA **Port A (Bit-Addressable)** **SFR 0x80**

b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

IOB **Port B (Bit-Addressable)** **SFR 0x90**

b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

IOC **Port C (Bit-Addressable)** **SFR 0xA0**

b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

IOD **Port D (Bit-Addressable)** **SFR 0xB0**

b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

IOE **Port E** **SFR 0xB1**

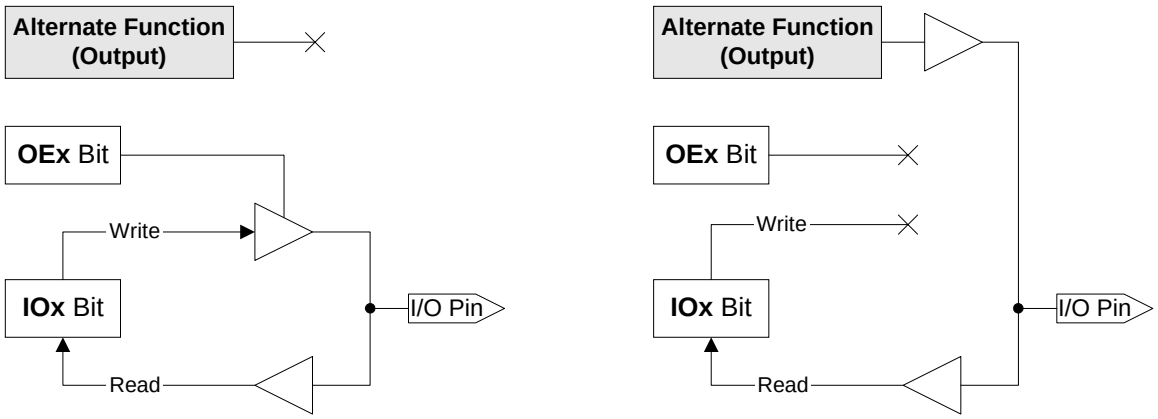
b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

Figure 13-3. I/O Port Data Registers

13.3 I/O Port Alternate Functions

Each I/O pin may be configured for an *alternate* (i.e., non-general-purpose I/O) function. These alternate functions are selected through various configuration registers, as described in the following sections.

The I/O-pin logic for alternate-function outputs is slightly different than for alternate-function inputs, as shown in Figures 13-4 (output) and 13-5 (input).



a) General-Purpose I/O Configuration

b) Alternate-Function Configuration

Figure 13-4. I/O-Pin Logic when Alternate Function is an OUTPUT

Figure 13-4 shows an I/O pin whose alternate function is always an *output*.

In Figure 13-4a, the I/O pin is configured for general-purpose I/O. In this configuration, the alternate function is disconnected and the pin functions normally.

In Figure 13-4b, the I/O pin is configured as an alternate-function output. In this configuration, the IOx/OEx output buffer is disconnected from the I/O pin, so writes to IOx and OEx have no effect on the I/O pin. *Reads* from IOx, however, continue to work normally; the state of the I/O pin (and, therefore, the state of the alternate function) is always available.

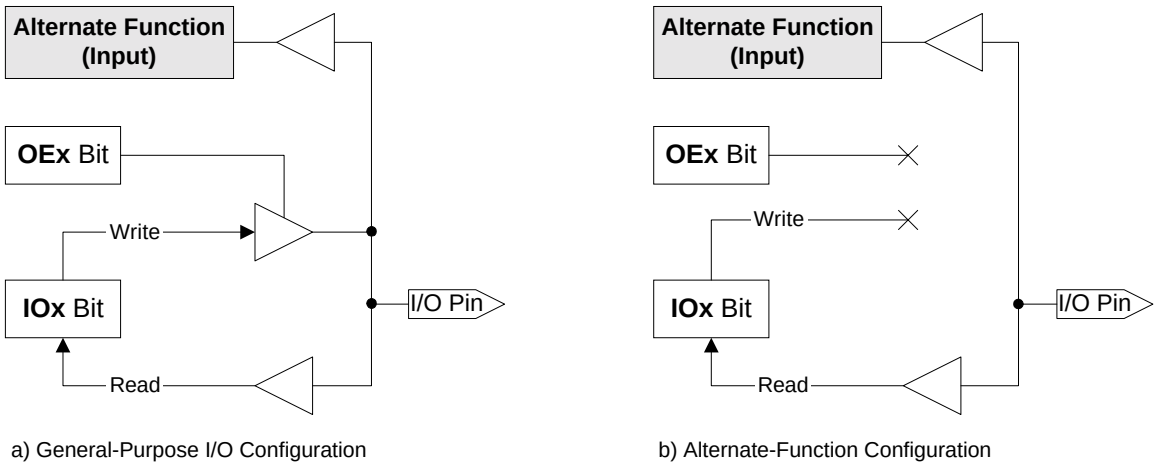


Figure 13-5. I/O-Pin Logic when Alternate Function is an INPUT

Figure 13-5 shows an I/O pin whose alternate function is always an *input*.

In Figure 13-5a, the I/O pin is configured for general-purpose I/O. There's an important difference between alternate-function *inputs* and the alternate-function *outputs* shown earlier in Figure 13-4: *Alternate-function inputs are never disconnected; they're always listening.*

If the alternate function's interrupt is enabled, signals on the I/O pin may trigger that interrupt. If the pin is to be used only for general-purpose I/O, the alternate function's interrupt must be disabled.

For example, suppose the PE5/INT6 pin is configured for general-purpose I/O. Since the INT6 function is an input, the pin signal is also routed to the FX2's internal INT6 logic. If the INT6 interrupt is enabled, traffic on the PE5 pin will trigger an INT6 interrupt. If this is undesirable, the INT6 interrupt should be disabled.

Of course, this side-effect can be useful in certain situations. In the case of PE5/INT6, for example, PE5 can trigger an INT6 interrupt even if the I/O pin is configured as an output (i.e., OEE.5 = 1), so the FX2's firmware can directly generate "external" interrupts.

In Figure 13-5b, the I/O pin is configured as an alternate-function input. Just as with alternate-function outputs, the IOx/OEx output buffer is disconnected from the I/O pin, so writes to IOx and OEx have no effect on the I/O pin. *Reads* from IOx, however, continue to work normally; the state of the I/O pin (and, therefore, the input to the alternate function) is always available.

13.3.1 Port A Alternate Functions

Alternate functions for the Port A pins are selected by bits in three registers, as shown in Tables 13-1 and 13-2.

Table 13-1. Register Bits Which Select Port A Alternate Functions

	b7	b6	b5	b4	b3	b2	b1	b0
PORTACFG (0xE670)	**FLAGD**	**SLCS[1]**	0	0	0	0	**INT1**	**INT0**
IFCONFIG (0xE601)	IFCLKSRC	3048MHZ	IFCLKOE	IFCLKPOL	ASYNC	GSTATE	**IFCFG1**	**IFCFG0**
WAKEUPCS (0xE682)	WU2	WU	WU2POL	WUPOL	0	DPEN	**WU2EN**	WUEN

Note 1: Although the SLCS alternate function is selected by bit 6 of PORTACFG, that function does not appear on pin PA6. Instead, the SLCS function appears on pin PA7 (see Table13-2).

Table 13-2. Port A Alternate-Function Configuration

Port A Pin	Alternate Function	Alternate Function is Selected By...	Alternate Function is Described in...
PA.0	INT0	PORTACFG.0 = 1	Chapter 4
PA.1	INT1	PORTACFG.1 = 1	Chapter 4
PA.2	SLOE	IFCFG1:0 = 11	Chapter 9
PA.3	WU2[1]	WU2EN = 1	Chapter 6
PA.4	FIFOADR0	IFCFG1:0 = 11	Chapter 9
PA.5	FIFOADR1	IFCFG1:0 = 11	Chapter 9
PA.6	PKTEND	IFCFG1:0 = 11	Chapter 9
PA.7	FLAGD[2]	PORTACFG.7 = 1	Chapter 9
	SLCS[3]	PORTACFG.6 = 1 **and** IFCFG1:0 = 11	Chapter 9

Note 1: When PA.3 is configured for alternate function WU2, it continues to function as a general-purpose input pin as well. See Section 6.4.1, "WU2 Pin" for more information.
Note 2: Although PA.7's alternate function FLAGD is selected via the PORTACFG register, the state of the FLAGD output is undefined unless IFCFG1:0 = 11.
Note 3: FLAGD takes priority over SLCS if PORTACFG.6 and PORTACFG.7 are both set to 1.

13.3.2 Port B and Port D Alternate Functions

When IFCFG1 = 1, all eight Port B pins are configured for an alternate configuration (FIFO Data 7:0).

If *any* of the FIFOs are set to 16-bit mode (via the WORDWIDE bits in the EPxFIFOCFG registers), all eight Port D pins are also configured for an alternate configuration (FIFO Data 15:8). See Tables 13-3, 13-4, and 13-5.

*If **all** WORDWIDE bits are cleared to 0 (i.e., if all four FIFOs are operating in 8-bit mode), the eight Port D pins may be used as general-purpose I/O pins even if IFCFG1 = 1.*

Table 13-3. Register Bits Which Select Port B and Port D Alternate Functions

	b7	b6	b5	b4	b3	b2	b1	b0
IFCONFIG (0xE601)	IFCLKSRC	3048MHZ	IFCLKOE	IFCLKPOL	ASYNC	GSTATE	**IFCFG1**	IFCFG0
EP2FIFOCFG (0xE618)	0	INFM2	OEP2	AUTOOUT	AUTOIN	ZEROLENIN	0	**WORDWIDE**
EP4FIFOCFG (0xE619)	0	INFM4	OEP4	AUTOOUT	AUTOIN	ZEROLENIN	0	**WORDWIDE**
EP6FIFOCFG (0xE61A)	0	INFM6	OEP6	AUTOOUT	AUTOIN	ZEROLENIN	0	**WORDWIDE**
EP8FIFOCFG (0xE61B)	0	INFM8	OEP8	AUTOOUT	AUTOIN	ZEROLENIN	0	**WORDWIDE**

Table 13-4. Port B Alternate-Function Configuration

Port B Pin	Alternate Function	Alternate Function is Selected By...	Alternate Function is Described in...
PB.7:0	FD[7:0]	IFCFG1 = 1	Chapter 9

Table 13-5. Port D Alternate-Function Configuration

Port D Pin	Alternate Function	Alternate Function is Selected By...	Alternate Function is Described in...
PD.7:0	FD[15:8]	IFCFG1 = 1 **and** any WORDWIIDE bit = 1	Chapter 9

13.3.3 Port C Alternate Functions

Each Port C pin may be individually configured for an alternate function by setting a bit in the PORTCCFG register, as shown in Tables 13-6 and 13-7.

Table 13-6. Register Bits Which Select Port C Alternate Functions

	b7	b6	b5	b4	b3	b2	b1	b0
PORTCCFG (0xE671)	**GPIFA7**	**GPIFA6**	**GPIFA5**	**GPIFA4**	**GPIFA3**	**GPIFA2**	**GPIFA1**	**GPIFA0**

Table 13-7. Port C Alternate-Function Configuration

Port C Pin	Alternate Function	Alternate Function is Selected By...	Alternate Function is Described in...
PC.0	GPIFA0[1]	PORTCCFG.0 = 1	Chapter 10
PC.1	GPIFA1[1]	PORTCCFG.1 = 1	Chapter 10
PC.2	GPIFA2[1]	PORTCCFG.2 = 1	Chapter 10
PC.3	GPIFA3[1]	PORTCCFG.3 = 1	Chapter 10
PC.4	GPIFA4[1]	PORTCCFG.4 = 1	Chapter 10
PC.5	GPIFA5[1]	PORTCCFG.5 = 1	Chapter 10
PC.6	GPIFA6[1]	PORTCCFG.6 = 1	Chapter 10
PC.7	GPIFA7[1]	PORTCCFG.7 = 1	Chapter 10

Note 1: Although the Port C alternate functions GPIFA0:7 are selected via the PORTCCFG register, the states of the GPIFA0:7 outputs are undefined unless IFCFG1:0 = 10.

13.3.4 Port E Alternate Functions

Each Port E pin may be individually configured for an alternate function by setting a bit in the PORTECFG register.

If the GSTATE bit in the IFCONFIG register is set to 1, the PE.2:0 pins are automatically configured as GPIF Status pins GSTATE[2:0], regardless of the PORTECFG.2:0 settings. In other words, GSTATE overrides PORTECFG.2:0. See Tables 13-8 and 13-9.

Table 13-8. Register Bits Which Select Port E Alternate Functions

	b7	b6	b5	b4	b3	b2	b1	b0
PORTECFG (0xE671)	**GPIFA8**	**T2EX**	**INT6**	**RXD1OUT**	**RXD0OUT**	**T2OUT**	**T1OUT**	**T0OUT**
IFCONFIG (0xE601)	**IFCLKSRC**	**3048MHZ**	**IFCLKOE**	**IFCLKPOL**	**ASYNC**	**GSTATE**	**IFCFG1**	**IFCFG0**

Table 13-9. Port E Alternate-Function Configuration

Port E Pin	Alternate Function	Alternate Function is Selected By...	Alternate Function is Described in...
PE.0	T0OUT[1]	PORTECFG.0 = 1 **and** GSTATE = 0	Chapter 14
PE.1	T1OUT[1]	PORTECFG.1 = 1 **and** GSTATE = 0	Chapter 14
PE.2	T2OUT[1]	PORTECFG.2 = 1 **and** GSTATE = 0	Chapter 14
PE.3	RXD0OUT	PORTECFG.3 = 1	Chapter 14
PE.4	RXD1OUT	PORTECFG.4 = 1	Chapter 14
PE.5	INT6	PORTECFG.5 = 1	Chapter 4
PE.6	T2EX	PORTECFG.6 = 1	Chapter 14
PE.7	GPIFA8[2]	PORTECFG.7 = 1	Chapter 10

Note 1: If GSTATE is set to 1, these settings are overridden and PE.2:0 are all automatically configured as GPIF Status pins (see Chapter 10).

Note 2: Although the PE.7 alternate function GPIFA8 is selected via the PORTECFG register, the state of the GPIFA8 output is undefined unless IFCFG1:0 = 10.

Table 13-10. IFCFG Selection of Port I/O Pin Functions

IFCFG1:0 = 00 (Ports)	IFCFG1:0 = 10 (GPIF Master)	IFCFG1:0 = 11 (Slave FIFO)
PD7	FD[15]	FD[15]
PD6	FD[14]	FD[14]
PD5	FD[13]	FD[13]
PD4	FD[12]	FD[12]
PD3	FD[11]	FD[11]
PD2	FD[10]	FD[10]
PD1	FD[9]	FD[9]
PD0	FD[8]	FD[8]
PB7	FD[7]	FD[7]
PB6	FD[6]	FD[6]
PB5	FD[5]	FD[5]
PB4	FD[4]	FD[4]
PB3	FD[3]	FD[3]
PB2	FD[2]	FD[2]
PB1	FD[1]	FD[1]
PB0	FD[0]	FD[0]
$\overline{\text{INT0}}$ / PA0	**$\overline{\text{INT0}}$ / PA0**	**$\overline{\text{INT0}}$ / PA0**
$\overline{\text{INT1}}$ / PA1	**$\overline{\text{INT1}}$ / PA1**	**$\overline{\text{INT1}}$ / PA1**
PA2	PA2	SLOE
WU2 / PA3	**WU2 / PA3**	**WU2 / PA3**
PA4	PA4	FIFOADR0
PA5	PA5	FIFOADR1
PA6	PA6	PKTEND
PA7	PA7	PA7 / FLAGD / $\overline{\text{SLCS}}$
PC7:0	**PC7:0**	**PC7:0**
PE7:0	**PE7:0**	**PE7:0**

Note: Signals shown in bold type do not change with IFCFG; they are shown for completeness.

13.4 I²C-Compatible Bus Controller

The I²C-compatible bus controller uses the SCL (Serial Clock) and SDA (Serial Data) pins, and performs two functions:

- General-purpose interfacing to I²C peripherals
- Boot loading from a serial EEPROM

Pullup resistors are required on the SDA and SCL lines, ***even if nothing is connected to the I²C-compatible bus****. Each line should be pulled up to Vcc through a 2.2K ohm resistor.*

The bus frequency defaults to approximately 100 KHz for compatibility; it can be configured to run four times faster for devices that support the higher speed.

13.4.1 Interfacing to I²C Peripherals

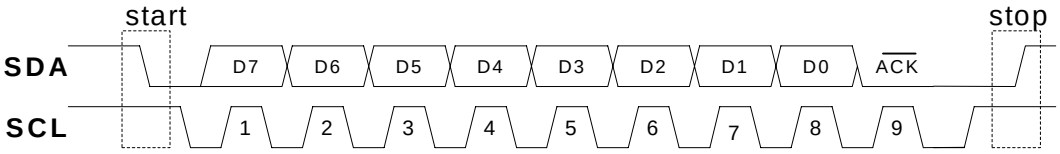


Figure 13-6. General I²C Transfer

Figure 13-6 illustrates the waveforms for an I²C transfer. SCL and SDA are open-drain FX2 pins, which must be pulled up to Vcc with external resistors. The FX2 is a bus master only, meaning that it synchronizes data transfers by generating clock pulses on SCL. Once the master drives SCL low, external slave devices can hold SCL low to extend clock-cycle times.

To synchronize I²C data, serial data (SDA) is permitted to change state only while SCL is low, and must be valid while SCL is high. Two exceptions to this rule are used to generate START and STOP conditions: a START condition is defined as a high-to-low transition on SDA while SCL is high, and a STOP condition is defined as a low-to-high transition on SDA while SCL is high. Data is sent MSB first. During the last bit time (clock #9 in Figur e13-6), the master floats the SDA line to allow the slave to acknowledge the transfer by pulling SDA low.

Multiple Bus Masters —	*The FX2 acts only as a bus master, never as a slave. Conflicts with a second master can be detected, however, by checking for BERR=1 (see Section 13.4.2.2, "Status Bits").*

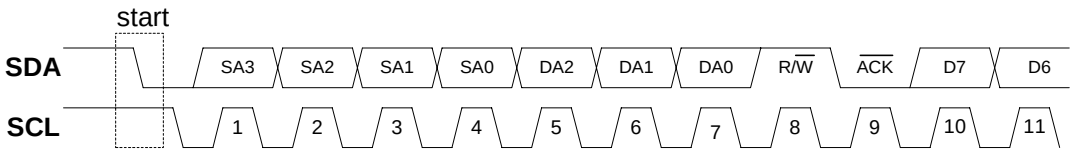


Figure 13-7. Addressing an I²C Peripheral

Each peripheral (slave) device on the I²C bus has a unique address. The first byte of an I²C transaction contains the address of the desired peripheral. Figure 13-7 shows the format for this first byte, which is sometimes called a *control* byte.

The FX2 sends the bit sequence shown in Figure 13-7 to select the peripheral at a particular address, to establish the transfer direction (using R/$\overline{W}$), and to determine if the peripheral is present by testing for $\overline{ACK}$.

The four most significant bits (SA3:0) are the peripheral chip's slave address. I²C devices are preassigned slave addresses by device type. Slave address 1010, for example, is assigned to EEPROMs. The next three bits (DA2:0) usually reflect the states of the peripheral's device address pins. Devices with three address pins can be strapped to allow eight distinct addresses for the same device type, which allows, for example, up to eight identical serial EEPROMs to be individually addressed.

The eighth bit (R/$\overline{W}$) sets the direction for the ensuing data transfer (1 = master read, 0 = master write). Most address transfers are followed by one or more data transfers, with the STOP condition generated after the last data byte is transferred.

In Figure 13-7, a READ transfer follows the address byte (at clock 8, the master sets the R/$\overline{W}$ bit high, indicating READ). At clock 9, the peripheral device responds to its address by asserting $\overline{ACK}$. At clock 10, the master floats SDA and issues SCL pulses to clock in SDA data supplied by the slave.

13.4.2 Registers

The three registers shown in Figur e13-8 are used to conduct transfers over the I²C-compatible bus.

Data is transferred to and from the bus through the I2DAT register. The I2CS register controls the transfers and reports various status conditions. I2CTL configures the bus.

I2CS **I²C-Compatible Bus Control and Status** **E678**

b7	b6	b5	b4	b3	b2	b1	b0
START	**STOP**	**LASTRD**	**ID1**	**ID0**	**BERR**	**ACK**	**DONE**
R/W	R/W	R/W	R	R	R	R	R
0	0	0	x	x	0	0	0

I2DAT **I²C-Compatible Bus Data** **E679**

b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

I2CTL **I²C-Compatible Bus Mode** **E67A**

b7	b6	b5	b4	b3	b2	b1	b0
0	**0**	**0**	**0**	**0**	**0**	**STOPE**	**400KHZ**
R	R	R	R	R	R	R/W	R/W
0	0	0	0	0	0	0	0

Figure 13-8. I²C-Compatible Registers

13.4.2.1 Control Bits

START

When START = 1, the next write to I2DAT generates the START condition followed by the serialized byte of data in I2DAT. The START bit is automatically cleared to 0 during the ACK interval (clock 9 in Figure 13-6).

STOP

When STOP = 1, a stop condition is generated. If the bus is idle when the STOP bit is set, the STOP condition is generated immediately; otherwise, the STOP condition is generated after the ACK phase of the current transfer. The STOP bit is automatically cleared after completing the STOP condition.

While the I²C-Compatible Bus controller is generating the “stop” condition, it ignores accesses to the I2CS and I2DAT registers. Firmware should therefore check the STOP Bit for zero before writing new data to I2CS or I2DAT.

An interrupt request is available to signal that the STOP condition is complete.

LASTRD

The master reads data by floating the SDA line and issuing clock pulses on the SCL line; after every eight bits, it drives SDA low for one clock to indicate ACK. To signal the last byte of a multi-byte transfer, the master *floats* SDA at ACK time to instruct the slave to stop sending.

When LASTRD = 1, the FX2 will float the SDA line after the next read transfer. The LASTRD bit is automatically cleared at the end of the transfer (at ACK time).

Setting LASTRD does not automatically generate a STOP condition. At the end of a read transfer, the STOP bit should also be set.

13.4.2.2 Status Bits

After a byte transfer, the FX2 updates the three status bits DONE, ACK, and BERR. If no STOP condition was transmitted, they are updated at ACK time; if a STOP condition was transmitted, they are updated after the STOP.

DONE

The FX2 sets this bit whenever it completes a byte transfer. The FX2 also generates an interrupt request when it sets the DONE bit. The DONE bit is automatically cleared when the I2DAT register is read or written, and the interrupt request bit is automatically cleared whenever the I2CS or I2DAT registers are read or written.

ACK

Every ninth SCL of a write transfer, the slave indicates reception of the byte by asserting ACK. The FX2 floats SDA during this time, samples the SDA line, and updates the ACK bit with the complement of the detected value. ACK=1 indicates acknowledge, and ACK=0 indicates not-acknowledge. The ACK bit should be ignored for read transfers on the bus.

BERR

This bit indicates a bus error. BERR=1 indicates that there was bus contention, which results when an outside device drives the bus when it shouldn’t, or when another bus master wins arbitration and takes control of the bus. When a bus error is detected, the current transfer is immediately cancelled, the FX2 floats the SCL and SDA lines, and the bus controller is disabled until a STOP con-

dition is detected on the bus. BERR is automatically cleared when the firmware reads or writes the I2DAT register.

Clearing the BERR bit (by accessing I2DAT) does not automatically re-enable the bus controller. Once a bus error occurs, the bus controller remains disabled until a STOP condition is detected.

ID1, ID0

These bits are automatically set by the boot loader to indicate the Boot EEPROM's addressing mode. They're normally used only for debug purposes; for full details, see Section 13.5.

13.4.3 Sending Data

To send a multiple-byte data record, follow these steps:

1. Set START=1.
2. Write the peripheral address and direction=0 (for write) to I2DAT.
3. Wait for DONE=1*. If BERR=1 or ACK=0, go to step 7.
4. Load I2DAT with a data byte.
5. Wait for DONE=1*. If BERR=1 or ACK=0 go to step 7.
6. Repeat steps 4 and 5 for each byte until all bytes have been transferred.
7. Set STOP=1.

* If INT3 is enabled, each "Wait for DONE=1" step can be interrupt-driven and handled by an interrupt service routine. See *Chapter 4, "Interrupts"* for more details.

13.4.4 Receiving Data

To read a multiple-byte data record, follow these steps:

1. Set START=1.
2. Write the peripheral address and direction=1 (for read) to I2DAT.
3. Wait for DONE=1*. If BERR=1 or ACK=0, terminate by setting STOP=1.
4. Read I2DAT and discard the data. This initiates the first burst of nine SCL pulses to clock in the first byte from the slave.
5. Wait for DONE=1*. If BERR=1, terminate by setting STOP=1.
6. Read the data from I2DAT. This initiates another read transfer.
7. Repeat steps 5 and 6 for each byte until ready to read the second-to-last byte.
8. Before reading the second-to-last I2DAT byte, set LASTRD=1.
9. Read the data from I2DAT. With LASTRD=1, this initiates the final byte read on the bus.
10. Wait for DONE=1*. If BERR=1, terminate by setting STOP=1.

11. Set STOP=1.
12. Read the last byte from I2DAT immediately (the next instruction) after setting the STOP bit. This retrieves the last data byte without initiating an extra read transaction (nine more SCL pulses) on the I²C-compatible bus.

* If INT3 is enabled, each “Wait for DONE=1” step can be interrupt-driven and handled by an interrupt service routine. See *Chapter 4, "Interrupts"* for more details.

13.5 EEPROM Boot Loader

Whenever the FX2 is taken out of reset via the reset pin, its boot loader checks for the presence of an EEPROM on the I²C-compatible bus. If an EEPROM is detected, the loader reads the first EEPROM byte to determine how to enumerate (specifically, whether to supply hard-wired ID information or read the ID from the EEPROM). The various enumeration modes are described in *Chapter 3, "Enumeration and ReNumeration™"*.

The FX2 boot loader supports two I²C-compatible EEPROM types:

- EEPROMs with slave address 1010 that use an 8-bit internal address (e.g., 24LC00, 24LC01/B, 24LC02/B).
- EEPROMs with slave address 1010 that use a 16-bit internal address (e.g., 24AA64, 24LC128, 24AA256).

EEPROMs with densities up to 256 bytes require only a single address byte; larger EEPROMs require two address bytes. The FX2 must determine which EEPROM type is connected — one or two address bytes — so that it can properly read the EEPROM.

The FX2 uses the EEPROM device-address pins A2, A1, and A0 to determine whether to send out one or two bytes of address. As shown in Table 13-11, single-byte-address EEPROMs must be strapped to address 000, while double-byte-address EEPROMs must be strapped to address 001.

Table 13-11. Strap Boot EEPROM Address Lines to These Values

Bytes	Example EEPROM	A2	A1	A0
16	24LC00*	N/A	N/A	N/A
128	24LC01	0	0	0
256	24LC02	0	0	0
4K	24LC32	0	0	1
8K	24LC64	0	0	1

* This EEPROM does not have device-address pins

After determining whether a one- or two-byte-address EEPROM is attached, the FX2 reports its results in the ID1 and ID0 bits, as shown in Table 13-12.

Table 13-12. Results of Power-On-Reset EEPROM Test

ID1	ID0	Meaning
0	0	No EEPROM detected
0	1	One-byte-address load EEPROM detected
1	0	Two-byte-address load EEPROM detected
1	1	Not used

Additional EEPROM devices (with slave address of 1010) can be attached to the I²C-compatible bus for general-purpose use, as long as they are strapped for device addresses other than 000 or 001.

The 24LC00 EEPROM is a special case, because it responds to all eight device addresses. If a 24LC00 is used for boot loading, no other EEPROMS with device address 1010 may be used.

Chapter 14 Timers/Counters and Serial Interface

14.1 Introduction

The FX2's timer/counters and serial interface are very similar to the standard 8051's, with some differences and enhancements. This chapter provides technical information on configuring and using the timer/counters and serial interface.

14.2 Timers/Counters

The FX2 includes three timer/counters (Timer 0, Timer 1, and Timer 2). Each timer/counter can operate either as a timer with a clock rate based on the FX2's internal clock (CLKOUT) or as an event counter clocked by the T0 pin (Timer 0), T1 pin (Timer 1), or the T2 pin (Timer 2). Timers 1 and 2 may be used for baud clock generation for the serial interface (see Section 14.3 for details of the serial interface).

The FX2 can be configured to operate at 12, 24, or 48 MHz. In "timer" mode, the timer/counters run at the same speed as the FX2, and they are not affected by the CLKOE and CLKINV configuration bits (CPUCS.1 and CPUCS.2).

Each timer/counter consists of a 16-bit register that is accessible to software as two SFRs:

- Timer 0 — TH0 and TL0
- Timer 1 — TH1 and TL1
- Timer 2 — TH2 and TL2

14.2.1 803x/805x Compatibility

The implementation of the timers/counters is similar to that of the Dallas Semiconductor DS80C320. Table 14-1 summarizes the differences in timer/counter implementation between the Intel 8051, the Dallas Semiconductor DS80C320, and the FX2.

Table 14-1. Timer/Counter Implementation Comparison

Feature	Intel 8051	Dallas DS80C320	FX2
Number of timers	2	3	3
Timer 0/1 overflow available as output signals	No	No	Yes; T0OUT, T1OUT (one CLKOUT pulse)
Timer 2 output enable	n/a	Yes	Yes
Timer 2 down-count enable	n/a	Yes	No
Timer 2 overflow available as output signal	n/a	Yes	Yes; T2OUT (one CLKOUT pulse)

14.2.2 Timers 0 and 1

Timers 0 and 1 operate in four modes, as controlled through the TMOD SFR (Tabl e14-2) and the TCON SFR (Table 14-3). The four modes are:

- 13-bit timer/counter (mode 0)
- 16-bit timer/counter (mode 1)
- 8-bit counter with auto-reload (mode 2)
- Two 8-bit counters (mode 3, Timer 0 only)

14.2.2.1 Mode 0, 13-Bit Timer/Counter — Timer 0 and Timer 1

Mode 0 operation is illustrated in Figure 14-1.

In mode 0, the timer is configured as a 13-bit counter that uses bits 0-4 of TL0 (or TL1) and all 8 bits of TH0 (or TH1). The timer enable bit (TR0/TR1) in the TCON SFR starts the timer. The C/$\overline{T}$ Bit selects the timer/counter clock source: either CLKOUT or the T0/T1 pins.

The timer counts transitions from the selected source as long as the GATE Bit is 0, or the GATE Bit is 1 and the corresponding interrupt pin ($\overline{INT0}$ or $\overline{INT1}$) is 1.

When the 13-bit count increments from 0x1FFF (all ones), the counter rolls over to all zeros, the TF0 (or TF1) Bit is set in the TCON SFR, and the T0OUT (or T1OUT) pin goes high for one clock cycle.

The upper 3 bits of TL0 (or TL1) are indeterminate in mode 0 and should be ignored.

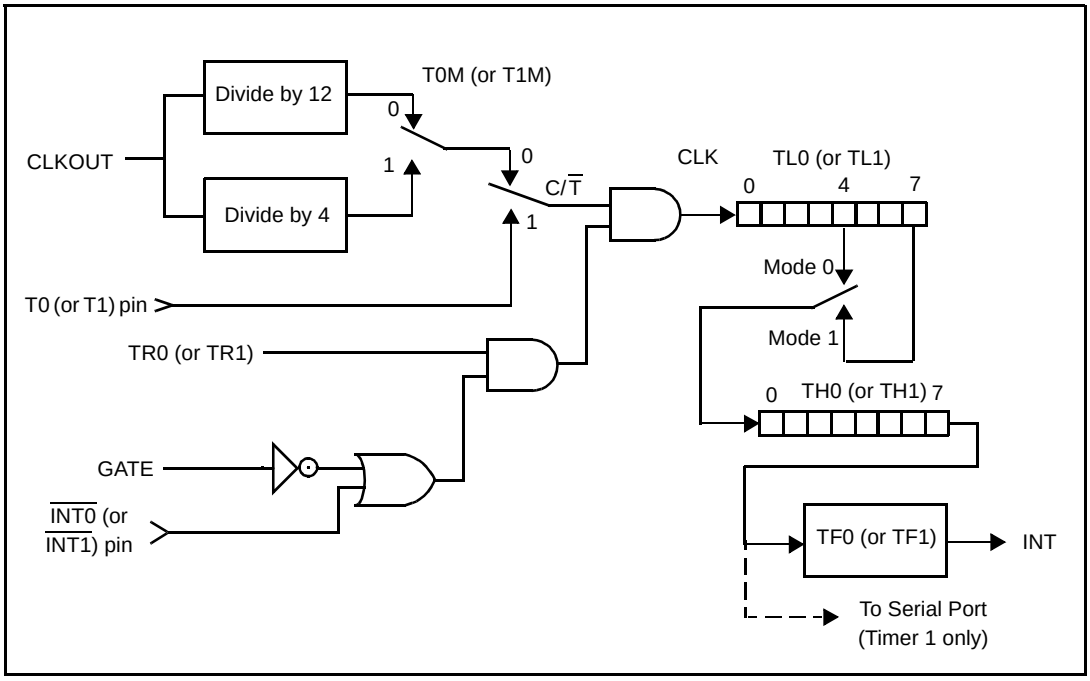


Figure 14-1. Timer 0/1 - Modes 0 and 1

14.2.2.2 Mode 1, 16-Bit Timer/Counter — Timer 0 and Timer 1

In mode 1, the timer is configured as a 16-bit counter. As illustrated in Figure 14-1, all 8 bits of the LSB Register (TL0 or TL1) are used. The counter rolls over to all zeros when the count increments from 0xFFFF. Otherwise, mode 1 operation is the same as mode 0.

Table 14-2. TMOD Register — SFR 0x89

Bit	Function
TMOD.7	**GATE1** - Timer 1 gate control. When GATE1 = 1, Timer 1 will clock only when $\overline{INT1}$ = 1 and TR1 (TCON.6) = 1. When GATE1 = 0, Timer 1 will clock only when TR1 = 1, regardless of the state of INT1.
TMOD.6	**C/$\overline{T}$1** - Counter/Timer select. When C/$\overline{T}$1 = 0, Timer 1 is clocked by CLKOUT/4 or CLKOUT/12, depending on the state of T1M (CKCON.4). When C/$\overline{T}$1 = 1, Timer 1 is clocked by high-to-low transitions on the T1 pin.
TMOD.5 TMOD.4	**M1** - Timer 1 mode select bit 1. **M0** - Timer 1 mode select bit 0. M1 M0 Mode 0 0 Mode 0 : 13-bit counter 0 1 Mode 1 : 16-bit counter 1 0 Mode 2 : 8-bit counter with auto-reload 1 1 Mode 3 : Timer 1 stopped
TMOD.3	**GATE0** - Timer 0 gate control, When GATE0 = 1, Timer 0 will clock only when $\overline{INT0}$ = 1 and TR0 (TCON.4) = 1. When GATE0 = 0, Timer 0 will clock only when TR0 = 1, regardless of the state of INT0.
TMOD.2	**C/$\overline{T}$0** - Counter/Timer select. When C/$\overline{T}$0 = 0, Timer 0 is clocked by CLKOUT/4 or CLKOUT/12, depending on the state of T0M (CKCON.3). When C/$\overline{T}$0 = 1, Timer 0 is clocked by high-to-low transitions on the T0 pin.
TMOD.1 TMOD.0	**M1** - Timer 0 mode select bit 1. **M0** - Timer 0 mode select bit 0. M1 M0 Mode 0 0 Mode 0 : 13-bit counter 0 1 Mode 1 : 16-bit counter 1 0 Mode 2 : 8-bit counter with auto-reload 1 1 Mode 3 : Two 8-bit counters

Table 14-3. TCON Register — SRF 0x88

Bit	Function
TCON.7	**TF1** - Timer 1 overflow flag. Set to 1 when the Timer 1 count overflows; automatically cleared when the FX2 vectors to the interrupt service routine.
TCON.6	**TR1** - Timer 1 run control. 1 = Enable counting on Timer 1.
TCON.5	**TF0** - Timer 0 overflow flag. Set to 1 when the Timer 0 count overflows; automatically cleared when the FX2 vectors to the interrupt service routine.
TCON.4	**TR0** - Timer 0 run control. 1 = Enable counting on Timer 0.
TCON.3	**IE1** - Interrupt 1 edge detect. If external interrupt 1 is configured to be edge-sensitive (IT1 = 1), IE1 is set when a negative edge is detected on the $\overline{INT1}$ pin and is automatically cleared when the FX2 vectors to the corresponding interrupt service routine. In this case, IE1 can also be cleared by software. If external interrupt 1 is configured to be level-sensitive (IT1 = 0), IE1 is set when the $\overline{INT1}$ pin is 0 and automatically cleared when the $\overline{INT1}$ pin is 1. In level-sensitive mode, software cannot write to IE1.
TCON.2	**IT1** - Interrupt 1 type select. $\overline{INT1}$ is detected on falling edge when IT1 = 1; $\overline{INT1}$ is detected as a low level when IT1 = 0.
TCON.1	**IE0** - Interrupt 0 edge detect. If external interrupt 0 is configured to be edge-sensitive (IT0 = 1), IE0 is set when a negative edge is detected on the $\overline{INT0}$ pin and is automatically cleared when the FX2 vectors to the corresponding interrupt service routine. In this case, IE0 can also be cleared by software. If external interrupt 0 is configured to be level-sensitive (IT0 = 0), IE0 is set when the $\overline{INT0}$ pin is 0 and automatically cleared when the $\overline{INT0}$ pin is 1. In level-sensitive mode, software cannot write to IE0.
TCON.0	**IT0** - Interrupt 0 type select. $\overline{INT0}$ is detected on falling edge when IT0 = 1; $\overline{INT0}$ is detected as a low level when IT0 = 0.

14.2.2.3 Mode 2, 8-Bit Counter with Auto-Reload — Timer 0 and Timer 1

In mode 2, the timer is configured as an 8-bit counter, with automatic reload of the start value on overflow. TL0 (or TL1) is the counter, and TH0 (or TH1) stores the reload value.

As illustrated in Figure 14-2, mode 2 counter control is the same as for mode 0 and mode 1. When TL0/1 increments from 0xFF, the value stored in TH0/1 is reloaded into TL0/1.

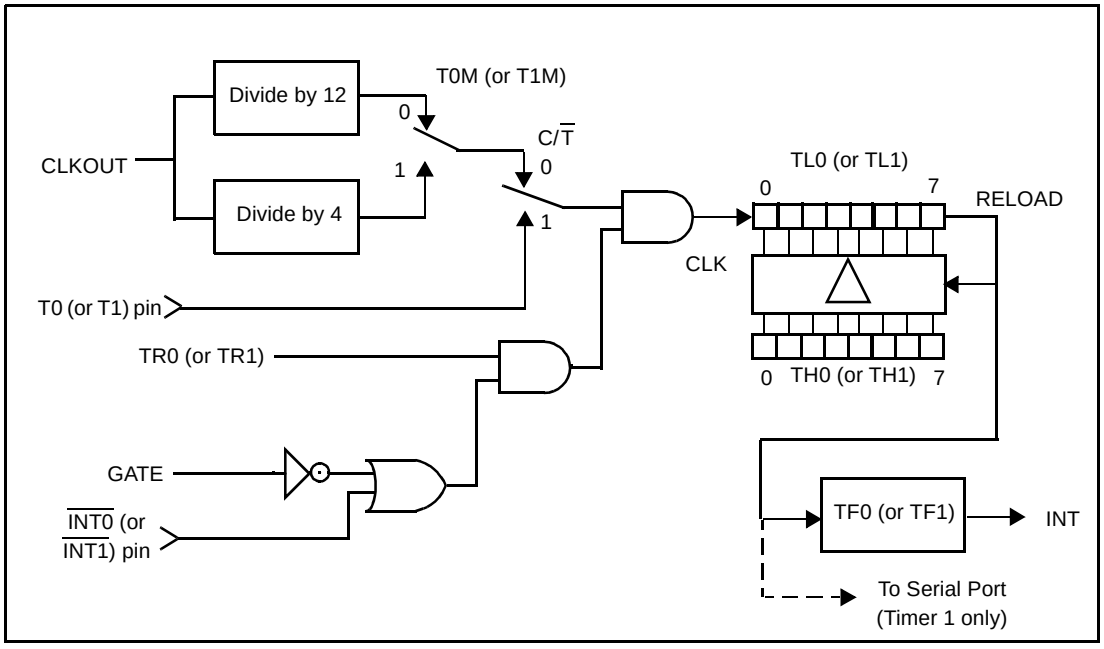


Figure 14-2. Timer 0/1 - Mode 2

14.2.2.4 Mode 3, Two 8-Bit Counters — Timer 0 Only

In mode 3, Timer 0 operates as two 8-bit counters. Selecting mode 3 for Timer 1 simply stops Timer 1.

As shown in Figur e14-3, TL0 is configured as an 8-bit counter controlled by the normal Timer 0 control bits. TL0 can either count CLKOUT cycles (divided by 4 or by 12) or high-to-low transitions on the T0 pin, as determined by the C/$\overline{T}$ Bit. The GATE function can be used to give counter enable control to the $\overline{INT0}$ pin.

TH0 functions as an independent 8-bit counter. However, TH0 can only count CLKOUT cycles (divided by 4 or by 12). The Timer 1 control and flag bits (TR1 and TF1) are used as the control and flag bits for TH0.

When Timer 0 is in mode 3, Timer 1 has limited usage because Timer 0 uses the Timer 1 control bit (TR1) and interrupt flag (TF1). Timer 1 can still be used for baud rate generation and the Timer 1 count values are still available in the TL1 and TH1 Registers.

Control of Timer 1 when Timer 0 is in mode 3 is through the Timer 1 mode bits. To turn Timer 1 on, set Timer 1 to mode 0, 1, or 2. To turn Timer 1 off, set it to mode 3. The Timer 1 C/$\overline{T}$ Bit and T1M Bit are still available to Timer 1. Therefore, Timer 1 can count CLKOUT/4, CLKOUT/12, or high-to-low transitions on the T1 pin. The Timer 1 GATE function is also available when Timer 0 is in mode 3.

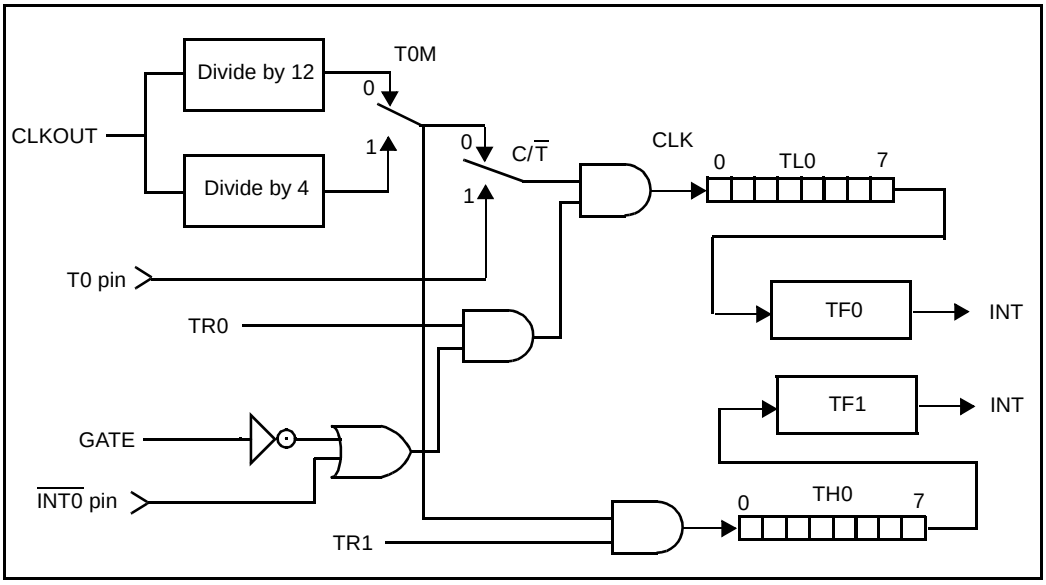


Figure 14-3. Timer 0 - Mode 3

14.2.3 Timer Rate Control

By default, the FX2 timers increment every 12 CLKOUT cycles, just as in the standard 8051. Using this default rate allows existing application code with real-time dependencies, such as baud rate, to operate properly.

Applications that require fast timing can set the timers to increment every 4 CLKOUT cycles instead, by setting bits in the Clock Control Register (CKCON) at SFR location 0x8E. (See Table 14-4).

Each timer's rate can be set independently. These settings have no effect in counter mode.

Table 14-4. CKCON (SFR 0x8E) Timer Rate Control Bits

Bit	Function
CKCON.5	**T2M** - Timer 2 clock select. When T2M = 0, Timer 2 uses CLKOUT/12 (for compatibility with standard 8051); when T2M = 1, Timer 2 uses CLKOUT/4. This bit has no effect when Timer 2 is configured for baud rate generation.
CKCON.4	**T1M** - Timer 1 clock select. When T1M = 0, Timer 1 uses CLKOUT/12 (for compatibility with standard 8051); when T1M = 1, Timer 1 uses CLKOUT/4.
CKCON.3	**T0M** - Timer 0 clock select. When T0M = 0, Timer 0 uses CLKOUT/12 (for compatibility with standard 8051); when T0M = 1, Timer 0 uses CLKOUT/4.

14.2.4 Timer 2

Timer 2 runs only in 16-bit mode and offers several capabilities not available with Timers 0 and 1. The modes available for Timer 2 are:

- 16-bit timer/counter
- 16-bit timer with capture
- 16-bit timer/counter with auto-reload
- Baud rate generator

The SFRs associated with Timer 2 are:

- T2CON (SFR 0xC8) — Timer/Counter 2 Control register, (see Table 14-5).
- RCAP2L (SFR 0xCA) — Used to capture the TL2 value when Timer 2 is configured for capture mode, or as the LSB of the 16-bit reload value when Timer 2 is configured for auto-reload mode.
- RCAP2H (SFR 0xCB) — Used to capture the TH2 value when Timer 2 is configured for capture mode, or as the MSB of the 16-bit reload value when Timer 2 is configured for auto-reload mode.
- TL2 (SFR 0xCC) — Lower 8 bits of the 16-bit count.
- TH2 (SFR 0xCD) — Upper 8 bits of the 16-bit count.

Table 14-5. T2CON Register — SFR 0xC8

Bit	Function
T2CON.7	**TF2** - Timer 2 overflow flag. Hardware will set TF2 when the Timer 2 overflows from 0xFFFF. TF2 must be cleared to 0 by the software. TF2 will only be set to a 1 if RCLK and TCLK are both cleared to 0. Writing a 1 to TF2 forces a Timer 2 interrupt if enabled.
T2CON.6	**EXF2** - Timer 2 external flag. Hardware will set EXF2 when a reload or capture is caused by a high-to-low transition on the T2EX pin, and EXEN2 is set. EXF2 must be cleared to 0 by software. Writing a 1 to EXF2 forces a Timer 2 interrupt if enabled.
T2CON.5	**RCLK** - Receive clock flag. Determines whether Timer 1 or Timer 2 is used for Serial Port 0 timing of received data in serial mode 1 or 3. RCLK=1 selects Timer 2 overflow as the receive clock; RCLK=0 selects Timer 1 overflow as the receive clock.
T2CON.4	**TCLK** - Transmit clock flag. Determines whether Timer 1 or Timer 2 is used for Serial Port 0 timing of transmit data in serial mode 1 or 3. TCLK=1 selects Timer 2 overflow as the transmit clock; TCLK=0 selects Timer 1 overflow as the transmit clock.
T2CON.3	**EXEN2** - Timer 2 external enable. EXEN2=1 enables capture or reload to occur as a result of a high-to-low transition on the T2EX pin, if Timer 2 is not generating baud rates for the serial port. EXEN2=0 causes Timer 2 to ignore all external events on the T2EX pin.
T2CON.2	**TR2** - Timer 2 run control flag. TR2=1 starts Timer 2; TR2=0 stops Timer 2.
T2CON.1	**C/$\overline{T}$2** - Counter/Timer select. When C/$\overline{T}$2 = 1, Timer 2 is clocked by high-to-low transitions on the T2 pin.When C/$\overline{T}$2 = 0 in modes 0, 1, or 2, Timer 2 is clocked by CLKOUT/4 or CLKOUT/12, depending on the state of T2M (CKCON.5). When C/$\overline{T}$2 = 0 in mode 3, Timer 2 is clocked by CLKOUT/2, regardless of the state of CKCON.5.
T2CON.0	**CP/$\overline{RL}$2** - Capture/reload flag. When CP/$\overline{RL}$2=1, Timer 2 captures occur on high-to-low transitions of the T2EX pin, if EXEN2 = 1. When CP/$\overline{RL}$2 = 0, auto-reloads occur when Timer 2 overflows or when high-to-low transitions occur on the T2EX pin, if EXEN2 = 1. If either RCLK or TCLK is set to 1, CP/$\overline{RL}$2 will not function and Timer 2 will operate in auto-reload mode following each overflow.

14.2.4.1 Timer 2 Mode Control

Table 14-6 summarizes how the T2CON bits determine the Timer 2 mode.

Table 14-6. Timer 2 Mode Control Summary

TR2	TCLK	RCLK	CP/$\overline{RL}$2	Mode
0	X	X	X	Timer 2 stopped
1	1	X	X	Baud rate generator
1	X	1	X	Baud rate generator
1	0	0	0	16-bit timer/counter with auto-reload
1	0	0	1	16-bit timer/counter with capture
X = Don't care				

14.2.5 Timer 2 — 16-Bit Timer/Counter Mode

Figure 14-4 illustrates how Timer 2 operates in timer/counter mode with the optional capture feature. The C/$\overline{T}$2 Bit determines whether the 16-bit counter counts CLKOUT cycles (divided by 4 or 12), or high-to-low transitions on the T2 pin. The TR2 Bit enables the counter. When the count increments from 0xFFFF, the TF2 flag is set and the T2OUT pin goes high for one CLKOUT cycle.

14.2.5.1 Timer 2 — 16-Bit Timer/Counter Mode with Capture

The Timer 2 capture mode (Figure 14-4) is the same as the 16-bit timer/counter mode, with the addition of the capture registers and control signals.

The CP/$\overline{RL}$2 Bit in the T2CON SFR enables the capture feature. When CP/$\overline{RL}$2 = 1, a high-to-low transition on the T2EX pin when EXEN2 = 1 causes the Timer 2 value to be loaded into the capture registers RCAP2L and RCAP2H.

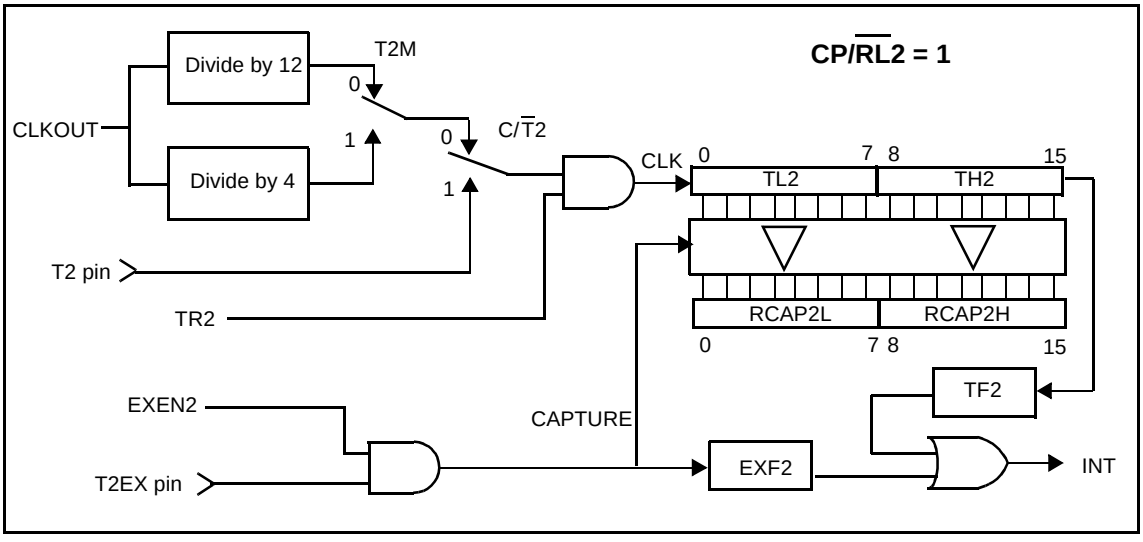


Figure 14-4. Timer 2 - Timer/Counter with Capture

14.2.6 Timer 2 — 16-Bit Timer/Counter Mode with Auto-Reload

When CP/$\overline{RL}$2 = 0, Timer 2 is configured for the auto-reload mode illustrated in Figur e14-5. Control of counter input is the same as for the other 16-bit counter modes. When the count increments from 0xFFFF, Timer 2 sets the TF2 flag and the starting value is reloaded into TL2 and TH2. Software must preload the starting value into the RCAP2L and RCAP2H registers.

When Timer 2 is in auto-reload mode, a reload can be forced by a high-to-low transition on the T2EX pin, if enabled by EXEN2 = 1.

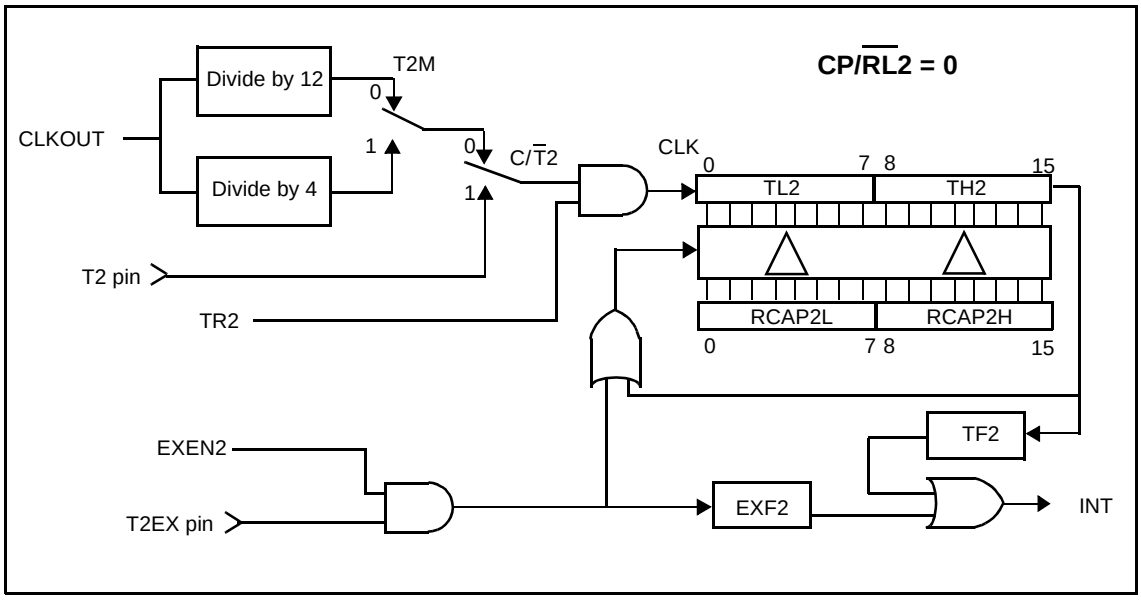


Figure 14-5. Timer 2 - Timer/Counter with Auto Reload

14.2.7 Timer 2 — Baud Rate Generator Mode

Setting either RCLK or TCLK to 1 configures Timer 2 to generate baud rates for Serial Port 0 in serial mode 1 or 3. Figure 14-6 is the functional diagram for the Timer 2 baud rate generator mode. In baud rate generator mode, Timer 2 functions in auto-reload mode. However, instead of setting the TF2 flag, the counter overflow is used to generate a shift clock for the serial port function. As in normal auto-reload mode, the overflow also causes the pre-loaded start value in the RCAP2L and RCAP2H Registers to be reloaded into the TL2 and TH2 Registers.

When either TCLK = 1 or RCLK = 1, Timer 2 is forced into auto-reload operation, regardless of the state of the CP/$\overline{RL2}$ Bit. Timer 2 is used as the receive baud clock source when RCLK=1, and as the transmit baud clock source when TCLK=1.

When operating as a baud rate generator, Timer 2 does not set the TF2 Bit. In this mode, a Timer 2 interrupt can only be generated by a high-to-low transition on the T2EX pin setting the EXF2 Bit, and only if enabled by EXEN2 = 1.

The counter time base in baud rate generator mode is CLKOUT/2. To use an external clock source, set C/$\overline{T2}$ to 1 and apply the desired clock source to the T2 pin.

The maximum frequency for an external clock source on the T2 pin is 3 MHz.

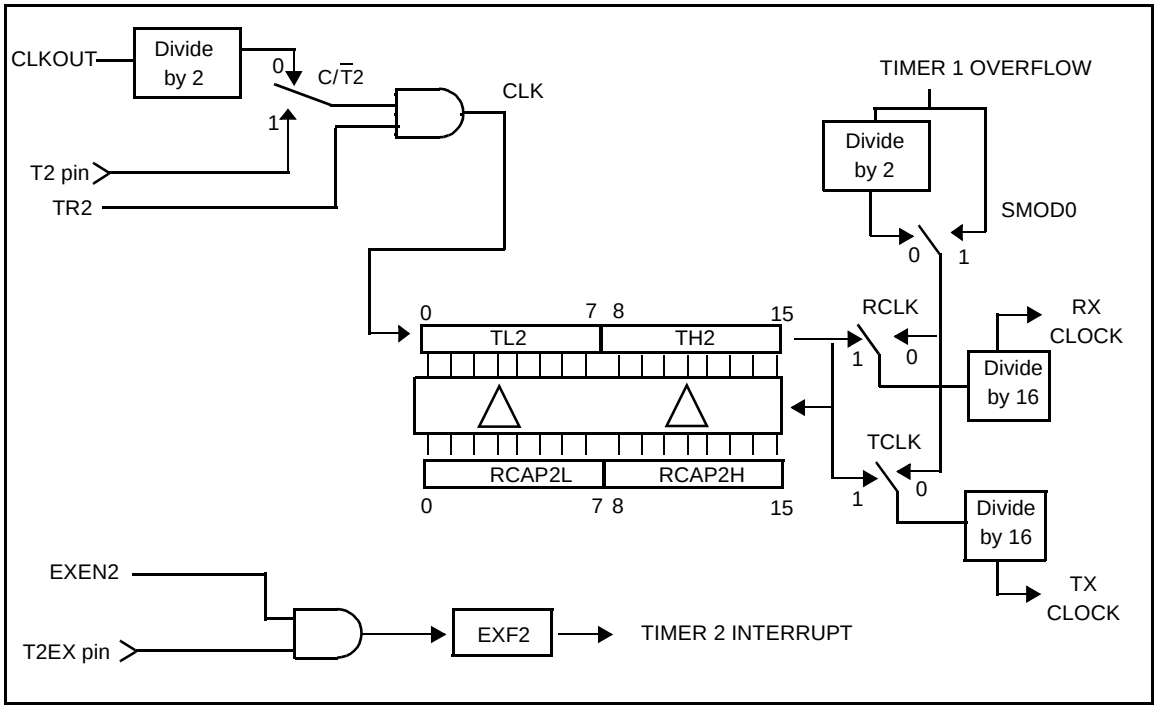


Figure 14-6. Timer 2 - Baud Rate Generator Mode

14.3 Serial Interface

The FX2 provides two serial ports. Serial Port 0 operates almost exactly as a standard 8051 serial port; depending on the configured mode (see Table 14-7), its baud-clock source can be CLKOUT/4 or CLKOUT/12, Timer 1, Timer 2, or the High-Speed Baud Rate Generator (see Section 14.3.2). Serial Port 1 is identical to Serial Port 0, except that it cannot use Timer 2 as its baud rate generator.

Each serial port can operate in synchronous or asynchronous mode. In synchronous mode, the FX2 generates the serial clock and the serial port operates in half-duplex mode. In asynchronous mode, the serial port operates in full-duplex mode. In all modes, the FX2 double-buffers the incoming data so that a byte of incoming data can be received while firmware is reading the previously-received byte.

Each serial port can operate in one of four modes, as outlined in Tabl e14-7.

Table 14-7. Serial Port Modes

Mode	Sync / Async	Baud-Clock Source	Data Bits	Start / Stop	9th Bit Function
0	Sync	CLKOUT/4 or CLKOUT/12	8	None	None
1	Async	Timer 1 (Ports 0 and 1), Timer 2 (Port 0 only), or High-Speed Baud Rate Generator (Ports 0 and 1)	8	1 start, 1 stop	None
2	Async	CLKOUT/32 or CLKOUT/64	9	1 start, 1 stop	0, 1, or parity
3	Async	Timer 1 (Ports 0 and 1), Timer 2 (Port 0 only), or High-Speed Baud Rate Generator (Ports 0 and 1)	9	1 start, 1 stop	0, 1, or parity
Note: The High-Speed Baud Rate Generator provides 115.2K or 230.4K baud rates (see Section 14.3.2).					

The registers associated with the serial ports are as follows. (Registers PCON and EICON also include some functionality which is not part of the Serial Interface).

- PCON (SFR 0x87) — Bit 7, Serial Port 0 rate control SMOD0 (Table 14-13).
- SCON0 (SFR 0x98) — Serial Port 0 control (Table 14-11).
- SBUF0 (SFR 0x99) — Serial Port 0 transmit/receive buffer.
- EICON (SFR 0xD8) — Bit 7, Serial Port 1 rate control SMOD1 (Table 14-12).
- SCON1 (SFR 0xC0) — Serial Port 1 control (Table 14-14).
- SBUF1 (SFR 0xC1) — Serial Port 1 transmit/receive buffer.
- T2CON (SFR 0xC8) — Baud clock source for modes 1 and 3 (RCLK and TCLK in Table 14-5).
- UART230 (0xE608) — High-Speed Baud Rate Generator enable (see Section 14.3.2, *"High-Speed Baud Rate Generator"*).

14.3.1 803x/805x Compatibility

The implementation of the serial interface is similar to that of the Dallas Semiconductor, DS80C320. Table 14-8 summarizes the differences in serial interface implementation between the Intel 8051, the Dallas Semiconductor DS80C320, and the FX2.

Table 14-8. Serial Interface Implementation Comparison

Feature	Intel 8051	Dallas DS80C320	FX2
Number of serial ports	1	2	2
Framing error detection	not implemented	implemented	not implemented
Slave address comparison for multiprocessor communication	not implemented	implemented	not implemented

14.3.2 High-Speed Baud Rate Generator

The FX2 incorporates a high-speed baud rate generator which can provide 115.2K and 230.4K baud rates for either or both serial ports, regardless of the FX2's internal clock frequency (12, 24, or 48 MHz).

The high-speed baud rate generator is enabled for Serial Port 0 by setting UART230.0 to 1; it's enabled for Serial Port 1 by setting UART230.1 to 1.

When enabled, the high-speed baud rate generator defaults to 115.2K baud.To select 230.4K baud for Serial Port 0, set SMOD0 (PCON.7) to 1; for Serial Port 1, set SMOD1 (EICON.7) to 1.

Table 14-9. UART230 Register — Address 0xE608

Bit	Function
UART230.7:2	**Reserved**
UART230.1	**230UART1** - Enable high-speed baud rate generator for serial port 1. When 230UART1 = 1, a 115.2K baud (if SMOD1 = 0) or 230.4K baud (if SMOD1 = 1) clock is provided to serial port 1. When 230UART1 = 0, serial port 1's baud clock is provided by one of the sources shown in Tabl e14-7.
UART230.0	**230UART0** - Enable high-speed baud rate generator for serial port 0. When 230UART0 = 1, a 115.2K baud (if SMOD0 = 0) or 230.4K baud (if SMOD0 = 1) clock is provided to serial port 0. When 230UART1 = 0, serial port 0's baud clock is provided by one of the sources shown in Tabl e14-7.

*When the High-Speed Baud Rate Generator is enabled for either serial port, **neither** port may use Timer 1 as its baud-clock source. Therefore, the allowable combinations of baud-clock sources for Modes 1 and 3 are:*

Table 14-10. Allowable Baud-Clock Combinations for Modes 1 and 3

Port 0	Port 1
Timer 1	Timer 1
Timer 2	Timer 1
Timer 2	High-Speed Baud Rate Generator
High-Speed Baud Rate Generator	High-Speed Baud Rate Generator

14.3.3 Mode 0

Serial mode 0 provides synchronous, half-duplex serial communication. For Serial Port 0, serial data output occurs on the RXD0OUT pin, serial data is received on the RXD0 pin, and the TXD0 pin provides the shift clock for both transmit and receive. For Serial Port 1, the corresponding pins are RXD1OUT, RXD1, and TXD1.

The serial mode 0 baud rate is either CLKOUT/12 or CLKOUT/4, depending on the state of the SM2_0 bit (or SM2_1 for Serial Port 1). When SM2_0 = 0, the baud rate is CLKOUT/12, when SM2_0 = 1, the baud rate is CLKOUT/4.

Mode 0 operation is identical to the standard 8051. Data transmission begins when an instruction writes to the SBUF0 (or SBUF1) SFR. The USART shifts the data, LSB first, at the selected baud rate, until the 8-bit value has been shifted out.

Mode 0 data reception begins when the REN_0 (or REN_1) bit is set and the RI_0 (or RI_1) bit is cleared in the corresponding SCON SFR. The shift clock is activated and the USART shifts data, LSB first, in on each rising edge of the shift clock until 8 bits have been received. One CLKOUT cycle after the 8th bit is shifted in, the RI_0 (or RI_1) bit is set and reception stops until the software clears the RI bit.

Figure 14-7 through Figure 14-10 illustrate Serial Port Mode 0 transmit and receive timing for both low-speed (CLKOUT/12) and high-speed (CLKOUT/4) operation. The figures show Port 0 signal names, RXD0, RXD0OUT, and TXD0. The timing is the same for Port 1 signals RXD1, RXD1OUT, and TXD1, respectively.

Table 14-11. SCON0 Register — SFR 98h

Bit	Function
SCON0.7	**SM0_0** - Serial Port 0 mode bit 0.
SCON0.6	**SM1_0** - Serial Port 0 mode bit 1, decoded as: SM0_0 SM1_0 Mode 0 0 0 0 1 1 1 0 2 1 1 3
SCON0.5	**SM2_0** - Multiprocessor communication enable. In modes 2 and 3, this bit enables the multiprocessor communication feature. If SM2_0 = 1 in mode 2 or 3, then RI_0 will not be activated if the received 9th bit is 0. If SM2_0=1 in mode 1, then RI_0 will only be activated if a valid stop is received. In mode 0, SM2_0 establishes the baud rate: when SM2_0=0, the baud rate is CLKOUT/12; when SM2_0=1, the baud rate is CLKOUT/4.
SCON0.4	**REN_0** - Receive enable. When REN_0=1, reception is enabled.
SCON0.3	**TB8_0** - Defines the state of the 9th data bit transmitted in modes 2 and 3.
SCON0.2	**RB8_0** - In modes 2 and 3, RB8_0 indicates the state of the 9th bit received. In mode 1, RB8_0 indicates the state of the received stop bit. In mode 0, RB8_0 is not used.
SCON0.1	**TI_0** - Transmit interrupt flag. Indicates that the transmit data word has been shifted out. In mode 0, TI_0 is set at the end of the 8th data bit. In all other modes, TI_0 is set when the stop bit is placed on the TXD0 pin. **TI_0 must be cleared by firmware.**
SCON0.0	**RI_0** - Receive interrupt flag. Indicates that serial data word has been received. In mode 0, RI_0 is set at the end of the 8th data bit. In mode 1, RI_0 is set after the last sample of the incoming stop bit, subject to the state of SM2_0. In modes 2 and 3, RI_0 is set at the end of the last sample of RB8_0. **RI_0 must be cleared by firmware.**

Table 14-12. EICON (SFR 0xD8) SMOD1 Bit

Bit	Function
EICON.7	**SMOD1** - Serial Port 1 baud rate doubler enable. When SMOD1 = 1 the baud rate for Serial Port is doubled.

Table 14-13. PCON (SFR 0x87) SMOD0 Bit

Bit	Function
PCON.7	**SMOD0** - Serial Port 0 baud rate double enable. When SMOD0 = 1, the baud rate for Serial Port 0 is doubled.

Table 14-14. SCON1 Register — SFR C0h

Bit	Function
SCON1.7	**SM0_1** - Serial Port 1 mode bit 0.
SCON1.6	**SM1_1** - Serial Port 1 mode bit 1, decoded as: SM0_1 SM1_1 Mode 0 0 0 0 1 1 1 0 2 1 1 3
SCON1.5	**SM2_1** - Multiprocessor communication enable. In modes 2 and 3, this bit enables the multiprocessor communication feature. If SM2_1 = 1 in mode 2 or 3, then RI_1 will not be activated if the received 9th bit is 0. If SM2_1=1 in mode 1, then RI_1 will only be activated if a valid stop is received. In mode 0, SM2_1 establishes the baud rate: when SM2_1=0, the baud rate is CLKOUT/12; when SM2_1=1, the baud rate is CLKOUT/4.
SCON1.4	**REN_1** - Receive enable. When REN_1=1, reception is enabled.
SCON1.3	**TB8_1** - Defines the state of the 9th data bit transmitted in modes 2 and 3.
SCON1.2	**RB8_1** - In modes 2 and 3, RB8_1 indicates the state of the 9th bit received. In mode 1, RB8_1 indicates the state of the received stop bit. In mode 0, RB8_1 is not used.
SCON1.1	**TI_1** - Transmit interrupt flag. Indicates that the transmit data word has been shifted out. In mode 0, TI_1 is set at the end of the 8th data bit. In all other modes, TI_1 is set when the stop bit is placed on the TXD1 pin. **TI_1 must be cleared by the software**.
SCON1.0	**RI_1** - Receive interrupt flag. Indicates that serial data word has been received. In mode 0, RI_1 is set at the end of the 8th data bit. In mode 1, RI_1 is set after the last sample of the incoming stop bit, subject to the state of SM2_1. In modes 2 and 3, RI_1 is set at the end of the last sample of RB8_1. **RI_1 must be cleared by the software**.

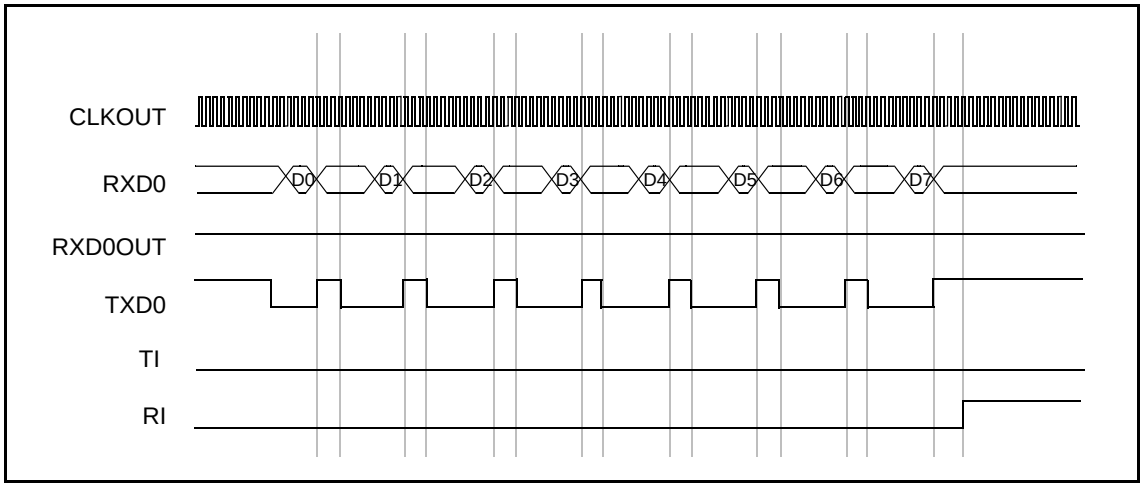


Figure 14-7. Serial Port Mode 0 Receive Timing - Low Speed Operation

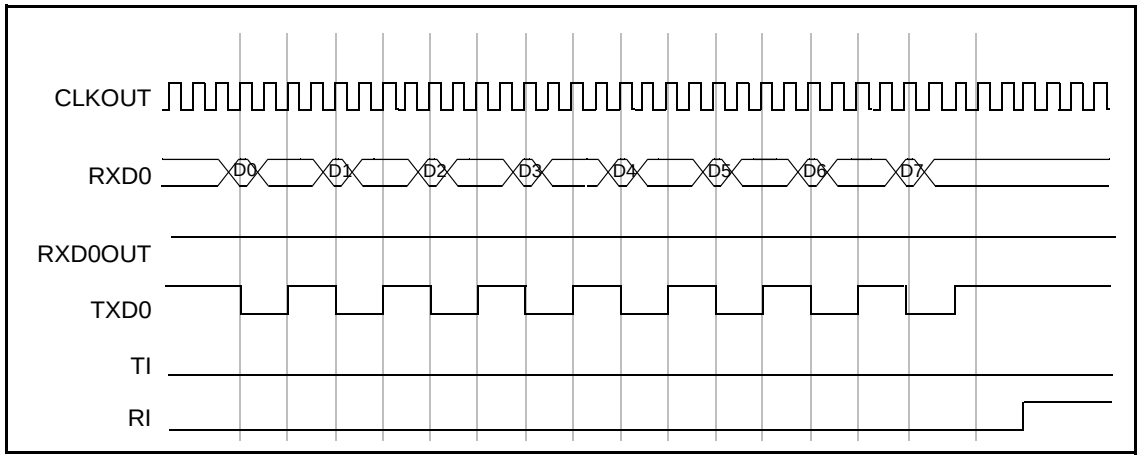


Figure 14-8. Serial Port Mode 0 Receive Timing - High Speed Operation

*At both low and high speed in Mode 0, data on RXD0 is sampled two CLKOUT cycles **before** the rising clock edge on TXD0.*

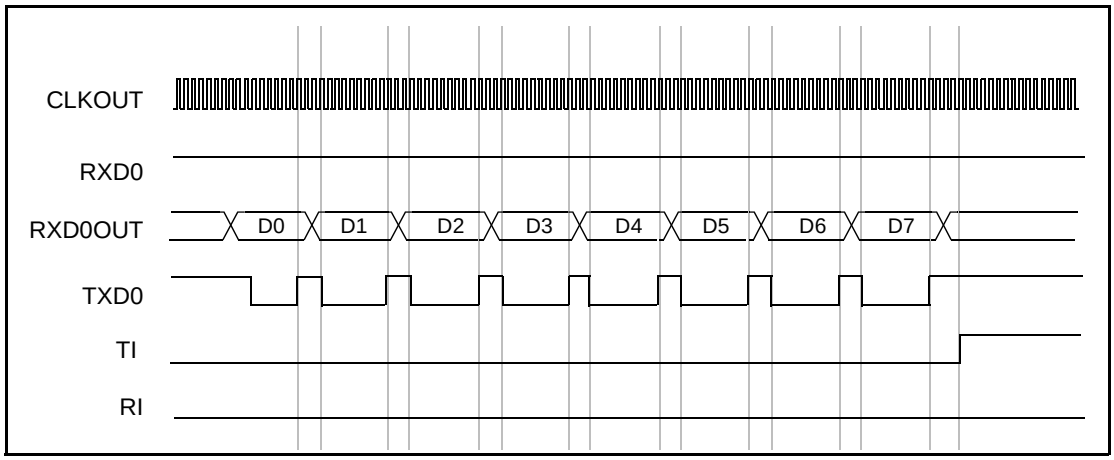


Figure 14-9. Serial Port Mode 0 Transmit Timing - Low Speed Operation

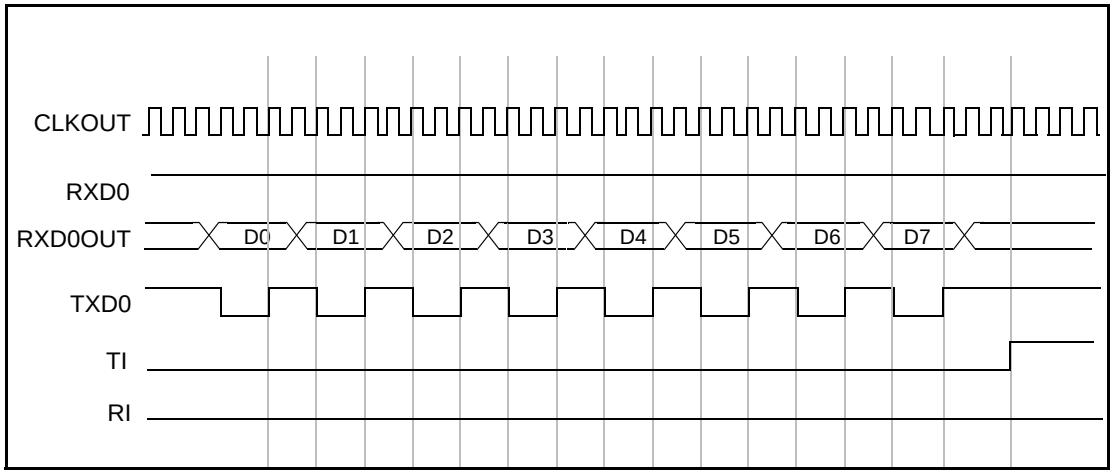


Figure 14-10. Serial Port Mode 0 Transmit Timing - High Speed Operation

14.3.4 Mode 1

Mode 1 provides standard asynchronous, full-duplex communication, using a total of 10 bits: 1 start bit, 8 data bits, and 1 stop bit. For receive operations, the stop bit is stored in RB8_0 (or RB8_1). Data bits are received and transmitted LSB first.

Mode 1 operation is identical to that of the standard 8051 when Timer 1 uses CLKOUT/12, (T1M=0, the default).

14.3.4.1 Mode 1 Baud Rate

The mode 1 baud rate is a function of timer overflow. Serial Port 0 can use either Timer 1 or Timer 2 to generate baud rates. Serial Port 1 can only use Timer 1. The two serial ports can run at the same baud rate if they both use Timer 1, or different baud rates if Serial Port 0 uses Timer 2 and Serial Port 1 uses Timer 1.

Each time the timer increments from its maximum count (0xFF for Timer 1 or 0xFFFF for Timer 2), a clock is sent to the baud rate circuit. That clock is then divided by 16 to generate the baud rate.

When using Timer 1, the SMOD0 (or SMOD1) Bit selects whether or not to divide the Timer 1 roll-over rate by 2. Therefore, when using Timer 1, the baud rate is determined by the equation:

$$\text{Baud Rate} = \frac{2^{\text{SMODx}}}{32} \times \text{Timer 1 Overflow}$$

When using Timer 2, the baud rate is determined by the equation:

$$\text{Baud Rate} = \frac{\text{Timer 2 Overflow}}{16}$$

To use Timer 1 as the baud rate generator, it is generally best to use Timer 1 mode 2 (8-bit counter with auto-reload), although any counter mode can be used. In mode 2, the Timer 1 reload value is stored in the TH1 register, which makes the complete formula for Timer 1:

$$\text{Baud Rate} = \frac{2^{\text{SMODx}}}{32} \times \frac{\text{CLKOUT}}{(12 - 8 \times \text{T1M}) \times (256 - \text{TH1})}$$

To derive the required TH1 value from a known baud rate when T1M=0, use the equation:

$$\text{TH1} = 256 - \frac{2^{\text{SMODx}} \times \text{CLKOUT}}{384 \times \text{Baud Rate}}$$

To derive the required TH1 value from a known baud rate when T1M=1, use the equation:

$$TH1 = 256 - \frac{2^{SMODx} \times CLKOUT}{128 \times \text{Baud Rate}}$$

Very low serial port baud rates may be achieved with Timer 1 by enabling the Timer 1 interrupt, configuring Timer 1 to mode 1, and using the Timer 1 interrupt to initiate a 16-bit software reload.

Table 14-15 lists sample reload values for a variety of common serial port baud rates, using Timer 1 operating in mode 2 (TMOD.5:4=10) with a CLKOUT/4 clock source (T1M=1) and the full timer rollover (SMOD1=1).

Table 14-15. Timer 1 Reload Values for Common Serial Port Mode 1 Baud Rates

Nominal Rate	CLKOUT = 12 MHz			CLKOUT = 24 MHz			CLKOUT = 48 MHz		
	TH1 Reload Value	Actual Rate	Error	TH1 Reload Value	Actual Rate	Error	TH1 Reload Value	Actual Rate	Error
57600	FD	62500	+8.50%	F9	53571	-6.99%	F3	57692	+0.16%
38400	FB	37500	-2.34%	F6	37500	-2.34%	EC	37500	-2.34%
28800	F9	26786	-6.99%	F3	28846	+0.16%	E6	28846	+0.16%
19200	F6	18750	-2.34%	EC	18750	-2.34%	D9	19230	+0.16%
9600	EC	9375	-2.34%	D9	9615	+0.16%	B2	9615	+0.16%
4800	D9	4807	+0.16%	B2	4807	+0.16%	64	4807	+0.16%
2400	B2	2403	+0.16%	64	2403	+0.16%	—	—	—
Settings: SMOD=1, C/$\overline{T}$=0, Timer1 Mode=2, T1M=1 ***Note:*** Using rates that are off by 2% or more will not work in all systems.									

More accurate baud rates may be achieved by using Timer 2 as the baud rate generator. To use Timer 2 as the baud rate generator, configure Timer 2 in auto-reload mode and set the TCLK and/or RCLK bits in the T2CON SFR. TCLK selects Timer 2 as the baud rate generator for the transmitter; RCLK selects Timer 2 as the baud rate generator for the receiver. The 16-bit reload value for Timer 2 is stored in the RCAP2L and RCA2H SFRs, which makes the equation for the Timer 2 baud rate:

$$\text{Baud Rate} = \frac{CLKOUT}{32 \times (65536 - 256 \times RCAP2H + RCAP2L)}$$

To derive the required RCAP2H and RCAP2L values from a known baud rate, use the equation:

$$RCAP2H:L = 65536 - \frac{CLKOUT}{32 \times Baud\ Rate}$$

When either RCLK or TCLK is set, the TF2 flag is not set on a Timer 2 rollover and the T2EX reload trigger is disabled.

Table 14-16 lists sample RCAP2H:L reload values for a variety of common serial baud rates.

Table 14-16. Timer 2 Reload Values for Common Serial Port Mode 1 Baud Rates

Nominal Rate	CLKOUT = 12 MHz			CLKOUT = 24 MHz			CLKOUT = 48 MHz		
	RCAP2H:L Reload Value	Actual Rate	Error	RCAP2H:L Reload Value	Actual Rate	Error	RCAP2H:L Reload Value	Actual Rate	Error
57600	FFF9	53571	-6.99%	FFF3	57692	+0.16%	FFE6	57692	+0.16%
38400	FFF6	37500	-2.34%	FFEC	37500	-2.34%	FFD9	38461	+0.16%
28800	FFF3	28846	+0.16%	FFE6	28846	+0.16%	FFCC	28846	+0.16%
19200	FFEC	18750	-2.34%	FFD9	19230	+0.16%	FFB2	19230	+0.16%
9600	FFD9	9615	+0.16%	FFB2	9615	+0.16%	FF64	9615	+0.16%
4800	FFB2	4807	+0.16%	FF64	4807	+0.16%	FEC8	4807	+0.16%
2400	FF64	2403	+0.16%	FEC8	2403	+0.16%	FD90	2403	+0.16%
Note: using rates that are off by 2.3% or more will not work in all systems.									

14.3.4.2 Mode 1 Transmit

Figure 14-11 illustrates the mode 1 transmit timing. In mode 1, the USART begins transmitting after the first rollover of the divide-by-16 counter after the software writes to the SBUF0 (or SBUF1) register. The USART transmits data on the TXD0 (or TXD1) pin in the following order: start bit, 8 data bits (LSB first), stop bit. The TI_0 (or TI_1) bit is set 2 CLKOUT cycles after the stop bit is transmitted.

14.3.5 Mode 1 Receive

Figure 14-12 illustrates the mode 1 receive timing. Reception begins at the falling edge of a start bit received on the RXD0 (or RXD1) pin, when enabled by the REN_0 (or REN_1) Bit. For this purpose, the RXD0 (or RXD1) pin is sampled 16 times per bit for any baud rate. When a falling edge

of a start bit is detected, the divide-by-16 counter used to generate the receive clock is reset to align the counter rollover to the bit boundaries.

For noise rejection, the serial port establishes the content of each received bit by a majority decision of 3 consecutive samples in the middle of each bit time. For the start bit, if the falling edge on the RXD0 (or RXD1) pin is not verified by a majority decision of 3 consecutive samples (low), then the serial port stops reception and waits for another falling edge on the RXD0 (or RXD1) pin.

At the middle of the stop bit time, the serial port checks for the following conditions:

- RI_0 (or RI_1) = 0
- If SM2_0 (or SM2_1) = 1, the state of the stop bit is 1
  (If SM2_0 (or SM2_1) = 0, the state of the stop bit doesn't matter.

If the above conditions are met, the serial port then writes the received byte to the SBUF0 (or SBUF1) Register, loads the stop bit into RB8_0 (or RB8_1), and sets the RI_0 (or RI_1) Bit. If the above conditions are not met, the received data is lost, the SBUF Register and RB8 Bit are not loaded, and the RI Bit is not set.

After the middle of the stop bit time, the serial port waits for another high-to-low transition on the (RXD0 or RXD1) pin.

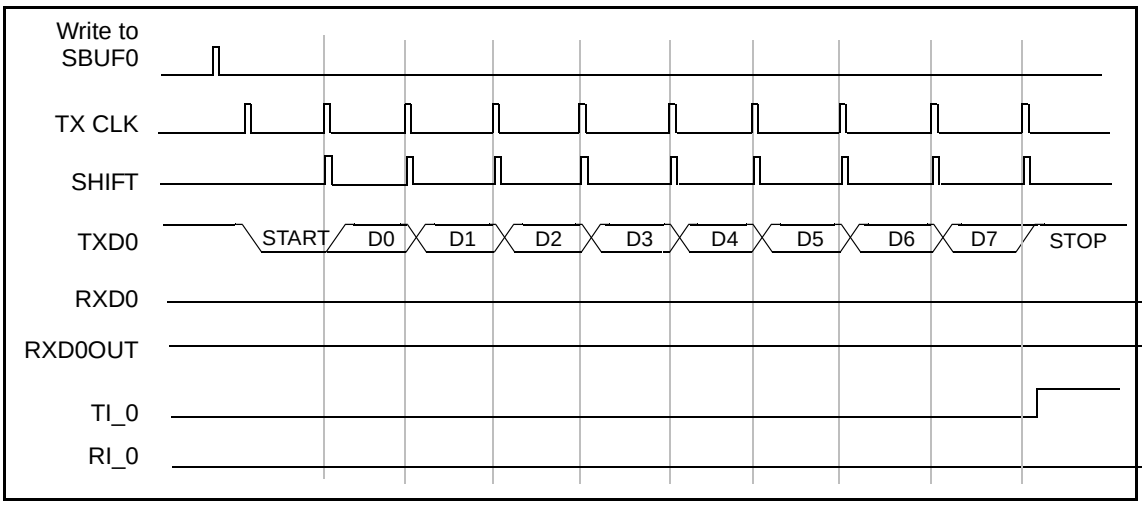


Figure 14-11. Serial Port 0 Mode 1 Transmit Timing

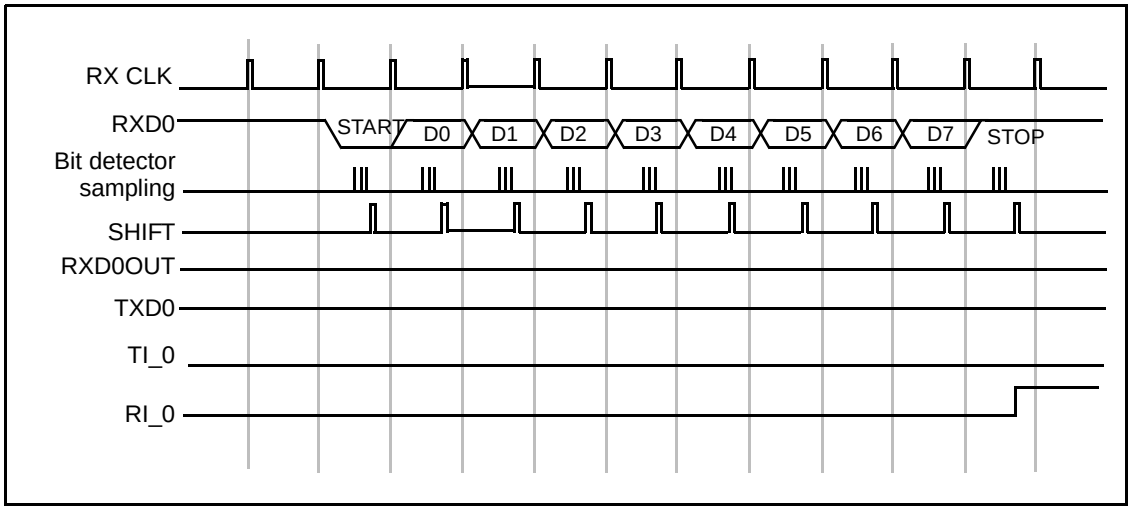


Figure 14-12. Serial Port 0 Mode 1 Receive Timing

14.3.6 Mode 2

Mode 2 provides asynchronous, full-duplex communication, using a total of 11 bits: 1 start bit, 8 data bits, a programmable 9th bit, and 1 stop bit. The data bits are transmitted and received LSB first. For transmission, the 9th bit is determined by the value in TB8_0 (or TB8_1). To use the 9th bit as a parity bit, move the value of the P bit (SFR PSW.0) to TB8_0 (or TB8_1).

The Mode 2 baud rate is either CLKOUT/32 or CLKOUT/64, as determined by the SMOD0 (or SMOD1) bit. The formula for the mode 2 baud rate is:

$$\text{Baud Rate} = \frac{2^{\text{SMODx}} \times \text{CLKOUT}}{64}$$

Mode 2 operation is identical to the standard 8051.

14.3.6.1 Mode 2 Transmit

Figure 14-13 illustrates the mode 2 transmit timing. Transmission begins after the first rollover of the divide-by-16 counter following a software write to SBUF0 (or SBUF1). The USART shifts data out on the TXD0 (or TXD1) pin in the following order: start bit, data bits (LSB first), 9th bit, stop bit. The TI_0 (or TI_1) Bit is set when the stop bit is placed on the TXD0 (or TXD1) pin.

14.3.6.2 Mode 2 Receive

Figure 14-14 illustrates the mode 2 receive timing. Reception begins at the falling edge of a start bit received on the RXD0 (or RXD1) pin, when enabled by the REN_0 (or REN_1) Bit. For this purpose, the RXD0 (or RXD1) pin is sampled 16 times per bit for any baud rate. When a falling edge of a start bit is detected, the divide-by-16 counter used to generate the receive clock is reset to align the counter rollover to the bit boundaries.

For noise rejection, the serial port establishes the content of each received bit by a majority decision of 3 consecutive samples in the middle of each bit time. For the start bit, if the falling edge on the RXD0 (or RXD1) pin is not verified by a majority decision of 3 consecutive samples (low), then the serial port stops reception and waits for another falling edge on the RXD0 (or RXD1) pin.

At the middle of the stop bit time, the serial port checks for the following conditions:

- RI_0 (or RI_1) = 0
- If SM2_0 (or SM2_1) = 1, the state of the stop bit is 1.
  (If SM2_0 (or SM2_1) = 0, the state of the stop bit doesn't matter.)

If the above conditions are met, the serial port then writes the received byte to the SBUF0 (or SBUF1) Register, loads the stop bit into RB8_0 (or RB8_1), and sets the RI_0 (or RI_1) Bit. If the above conditions are not met, the received data is lost, the SBUF Register and RB8 Bit are not loaded, and the RI Bit is not set. After the middle of the stop bit time, the serial port waits for another high-to-low transition on the RXD0 *(*or RXD1) pin.

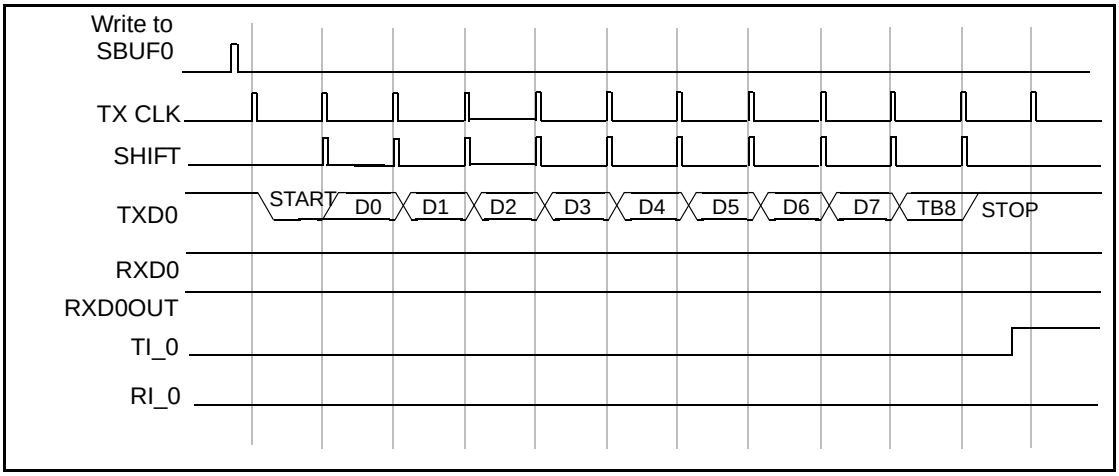


Figure 14-13. Serial Port 0 Mode 2 Transmit Timing

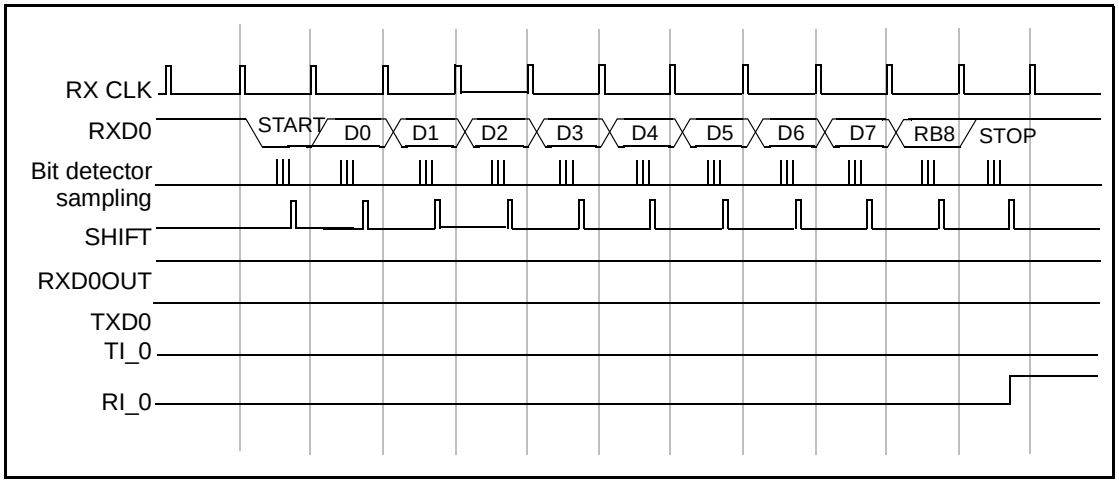


Figure 14-14. Serial Port 0 Mode 2 Receive Timing

14.3.7 Mode 3

Mode 3 provides asynchronous, full-duplex communication, using a total of 11 bits: 1 start bit, 8 data bits, a programmable 9th bit, and 1 stop bit. The data bits are transmitted and received LSB first.

The mode 3 transmit and operations are identical to mode 2. The mode 3 baud rate generation is identical to mode 1. That is, mode 3 is a combination of mode 2 protocol and mode 1 baud rate. Figure 14-15 illustrates the mode 3 transmit timing. Figure 14-16 illustrates the mode 3 receive timing.

Mode 3 operation is identical to that of the standard 8051 when Timer 1 uses CLKOUT/12, (T1M=0, the default).

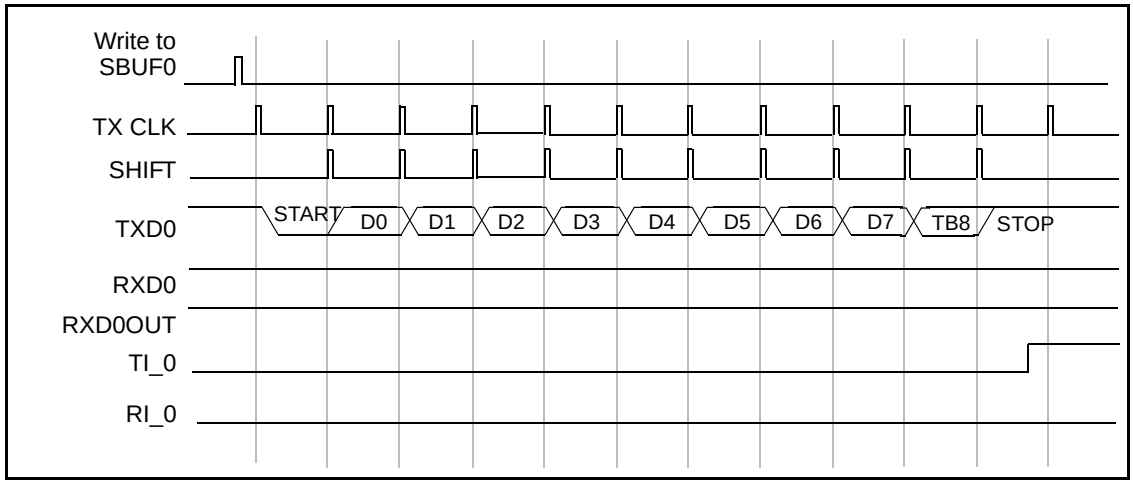


Figure 14-15. Serial Port 0 Mode 3 Transmit Timing

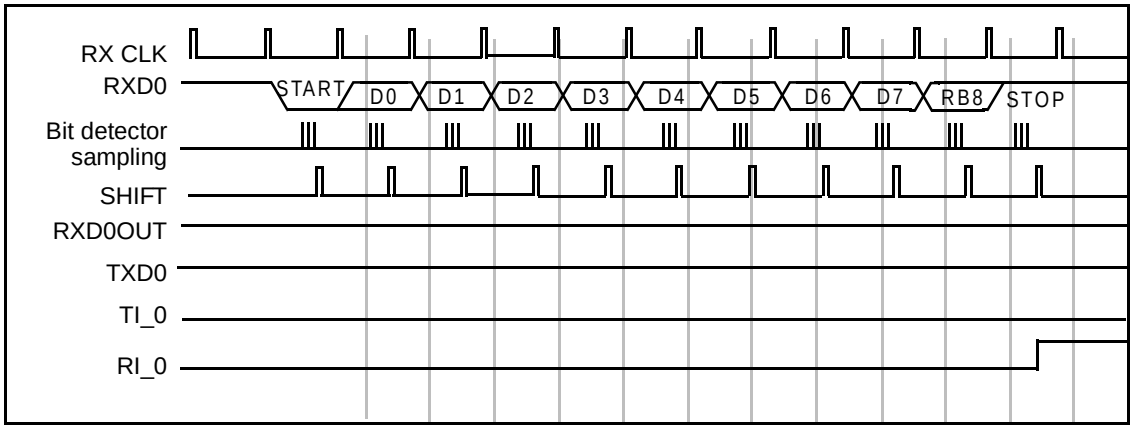


Figure 14-16. Serial Port 0 Mode 3 Receive Timing

Chapter 15 Registers

15.1 Introduction

This section describes the EZ-USB FX2 registers in the order they appear in the EZ-USB FX2 memory map, see Figure 5-4. The registers are named according to the following conventions.

Most registers deal with endpoints. The general register format is **DDDnFFF**, where:

DDD is endpoint direction, IN or OUT with respect to the USB host.

n is the endpoint number, where:

- "ISO" indicates isochronous endpoints as a group.

FFF is the function, where:

- CS is a control and status register
- IRQ is an Interrupt Request bit
- IE is an Interrupt Enable bit
- BC, BCL, and BCH are byte count registers. BC is used for single byte counts, and BCH/BCL are used as the high and low bytes of 16-bit byte counts.
- DATA is a single-register access to a FIFO.
- BUF is the start address of a buffer.

15.1.1 Example Register Formats

- EP1INBC is the Endpoint 1 IN byte count.

15.1.2 Other Conventions

USB Indicates a global (not endpoint-specific) USB function.

ADDR Is an address.

VAL Means valid.

FRAME Is a frame count.

PTR Is an address pointer.

Register Name	Register Function	Address

b7	b6	b5	b4	b3	b2	b1	b0
bitname	**bitname**	**bitname**	**bitname**	**bitname**	**bitname**	**bitname**	**bitname**
R, W access	R, W access	R, W access	R, W access	R, W access	R, W access	R, W access	R, W access
Default val	Default val	Default val	Default val	Default val	Default val	Default val	Default val

Figure 15-1. Register Description Format

Figure 15-1 illustrates the register description format used in this chapter.

- The top line shows the register name, functional description, and address in the EZ-USB FX2 memory.
- The second line shows the bit position in the register.
- The third line shows the name of each bit in the register.
- The fourth line shows CPU accessibility: R(ead), W(rite), or R/W.
- The fifth line shows the default value. These values apply after a Power-On-Reset (POR).

15.2 Special Function Registers (SFR)

FX2 implements many control registers as SFRs (Special Function Registers). These SFRs are shown in Table 15-1. Bold type indicates SFRs which are not in the standard 8051, but are included in the FX2.

Table 15-1. FX2 Special Function Registers (SFR)

x	8x	9x	Ax	Bx	Cx	Dx	Ex	Fx
0	**IOA**	**IOB**	**IOC**	**IOD**	**SCON1**	PSW	ACC	B
1	SP	**EXIF**	**INT2CLR**	**IOE**	**SBUF1**			
2	DPL0	**MPAGE**	**INT4CLR**	**OEA**				
3	DPH0			**OEB**				
4	**DPL1**			**OEC**				
5	**DPH1**			**OED**				
6	**DPS**			**OEE**				
7	PCON							
8	TCON	SCON0	**IE**	**IP**	**T2CON**	**EICON**	**EIE**	**EIP**
9	TMOD	SBUF0						
A	TL0	**AUTOPTRH1**	**EP2468STAT**	**EP01STAT**	**RCAP2L**			
B	TL1	**AUTOPTRL1**	**EP24FIFOFLGS**	**GPIFTRIG**	**RCAP2H**			
C	TH0		**EP68FIFOFLGS**		**TL2**			
D	TH1	**AUTOPTRH2**		**GPIFSGL-DATH**	**TH2**			
E	**CKCON**	**AUTOPTRL2**		**GPIFSGL-DATLX**				
F			**AUTOPTR-SETUP**	**GPIFSGL-DATLNOX**				

All unlabeled SFRs are reserved.

15.3 About SFRS

Because the SFRs are directly-addressable internal registers, firmware can access them quickly, without the overhead of loading the data pointer and performing a MOVX instruction. For example, the firmware reads the FX2 Port B pins using a single instruction, as shown in Figure 15-2.

```
mov    a,IOB
```

Figure 15-2. Single Instruction to Read Port B

Similarly, firmware writes the value 0x55 to Port C using only one MOV instruction, as shown in Figure 15-3.

```
mov    IOC,#55h
```

Figure 15-3. Single Instruction to Write to Port C

SFRs in Table 15-1 rows 0 and 8 are bit-addressable; individual bits of the registers may be efficiently set, cleared, or toggled using special bit-addressing instructions (e.g., **setb IOB.2** sets bit 2 of the IOB register).

IOA **Port A (bit addressable)** **SFR 0x80**

b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

IOB — Port B (bit addressable) — SFR 0x90

b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

AUTOPTRH1 — Autopointer 1 Address HIGH — SFR 0x9A

b7	b6	b5	b4	b3	b2	b1	b0
A15	**A14**	**A13**	**A12**	**A11**	**A10**	**A9**	**A8**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

AUTOPTRL1 — Autopointer 1 Address LOW — SFR 0x9B

b7	b6	b5	b4	b3	b2	b1	b0
A7	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

AUTOPTRH2 — Autopointer 2 Address HIGH — SFR 0x9D

b7	b6	b5	b4	b3	b2	b1	b0
A15	**A14**	**A13**	**A12**	**A11**	**A10**	**A9**	**A8**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

AUTOPTRL2 Autopointer 2 Address LOW SFR 0x9E

b7	b6	b5	b4	b3	b2	b1	b0
A7	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

IOC Port C (bit addressable) SFR 0xA0

b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

INT2CLR Interrupt 2 Clear SFR 0xA1

b7	b6	b5	b4	b3	b2	b1	b0
x	**x**	**x**	**x**	**x**	**x**	**x**	**x**
W	W	W	W	W	W	W	W
x	x	x	x	x	x	x	x

INT4CLR Interrupt 4 Clear SFR 0xA2

b7	b6	b5	b4	b3	b2	b1	b0
x	**x**	**x**	**x**	**x**	**x**	**x**	**x**
W	W	W	W	W	W	W	W
x	x	x	x	x	x	x	x

Writing any value to INT2CLR or INT4CLR clears the INT2 or INT4 interrupt request bit for the INT2/INT4 interrupt currently being serviced.

Writing to one of these registers has the same effect as clearing the appropriate interrupt request bit in the FX2 external register space. For example, suppose the EP2 Empty Flag interrupt is asserted. The FX2 automatically sets bit 1 of the EP2FIFOIRQ register (in External Data memory space, at 0xE651), and asserts the INT4 interrupt request.

Using autovectoring, the FX2 automatically calls (vectors to) the EP2_FIFO_EMPTY 2 Interrupt Service Routine (ISR). The first task in the ISR is to clear the interrupt request bit, EP2FIFOIRQ.1.

The firmware can do this either by accessing the EP2FIFOIRQ register (at 0xE651) and writing a 1 to bit 1, or simply by writing any value to INT4CLR. The first method requires the use of the data pointer, which must be saved and restored along with the accumulator in an ISR. The second method is much faster and does not require saving the data pointer, so it is preferred.

EP2468STAT Endpoint(s) 2,4,6,8 Status Flags SFR 0xAA

b7	b6	b5	b4	b3	b2	b1	b0
EP8F	**EP8E**	**EP6F**	**EP6E**	**EP4F**	**EP4E**	**EP2F**	**EP2E**
R	R	R	R	R	R	R	R
0	1	0	1	1	0	1	0

The bits in EP2468STAT correspond to Endpoint Status bits in the FX2 register file, as follows:

Table 15-2. SFR and FX2 Register File Correspondences

Bit	EPSTAT SFR	FX2 Register.Bit	FX2 Register File address
7	EP8 Full flag	EP8CS.3	E6A6
6	EP8 Empty flag	EP8CS.2	E6A6
5	EP6 Full flag	EP6CS.3	E6A5
4	EP6 Empty flag	EP6CS.2	E6A5
3	EP4 Full flag	EP4CS.3	E6A4
2	EP4 Empty flag	EP4CS.2	E6A4
1	EP2 Full flag	EP2CS.3	E6A3
0	EP2 Empty flag	EP2CS.2	E6A3

The Endpoint status bits represent the Packet Status.

EP24FIFOFLGS Endpoint(s) 2, 4 Slave FIFO Status Flags SFR 0xAB

b7	b6	b5	b4	b3	b2	b1	b0
0	**EP4PF**	**EP4EF**	**EP4FF**	**0**	**EP2PF**	**EP2EF**	**EP2FF**
R	R	R	R	R	R	R	R
0	0	1	0	0	0	1	0

EP68FIFOFLGS Endpoint(s) 6, 8 Slave FIFO Status Flags SFR 0xAC

b7	b6	b5	b4	b3	b2	b1	b0
0	**EP8PF**	**EP8EF**	**EP8FF**	**0**	**EP6PF**	**EP6EF**	**EP6FF**
R	R	R	R	R	R	R	R
0	1	1	0	0	1	1	0

AUTOPTRSETUP Autopointer(s) 1 & 2 Setup SFR 0xAF

b7	b6	b5	b4	b3	b2	b1	b0
0	**0**	**0**	**0**	**0**	**APTR2INC**	**APTR1INC**	**APTREN**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	1	0

FX2 provides two identical autopointers. They are similar to the internal “DPTR” data pointers, but with an additional feature: each can automatically increment after every memory access. Using one or both of the autopointers, FX2 firmware can perform very fast block memory transfers.

The AUTOPTRSETUP register is configured as follows:

- Set APTRnINC=0 to freeze the address pointer, APTRnINC=1 to automatically increment it for every read or write of an XAUTODATn register. This bit defaults to 1, enabling the auto-increment feature.
- To enable the autopointer, set APTREN=1. Enabling the Autopointers has one side-effect: Any *code* access (an instruction fetch, for instance) from addresses 0xE67B and 0xE67C will return the AUTODATA values, rather than the code-memory values at these two addresses. This introduces a two-byte “hole” in the code memory.

The firmware then writes a 16-bit address to AUTOPTRHn/Ln. Then, for every read or write of an XAUTODATn register, the address pointer automatically increments (if APTRnINC=1).

IOD Port D (bit addressable) SFR 0xB0

b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

FX2 I/O ports PORTA-PORTD appear as bit-addressable SFRS. Reading a register or bit returns the logic level of the port pin that's two CLKOUT-clocks old. Writing a register bit writes the port latch. Whether or not the port latch value appears on the I/O pin depends on the state of the pin's OE (Output Enable) bit. The I/O pins may also be assigned alternate function values, in which case the IOx and OEx bit values are overridden on a bit-by-bit basis.

IOD is bit-addressable; see Figure 15-4.

```
setb    IOD.2           ; set bit 2 of IOD SFR
```

Figure 15-4. Use Bit 2 to set PORTD - Single Instruction

IOE Port E SFR 0xB1

b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

IO port PORTE is also accessed using an SFR, but unlike the PORTA-PORTD SFRs, it is not bit-addressable; see Figure 15-5.

```
mov     a,IOE
or      a,#00001000b      ; set bit 3
mov     IOE,a
```

Figure 15-5. Use OR to Set Bit 3

OEA Port A Output Enable SFR 0xB2

b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

OEB Port B Output Enable SFR 0xB3

b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

OEC Port C Output Enable SFR 0xB4

b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

OED Port D Output Enable SFR 0xB5

b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

OEE Port E Output Enable SFR 0xB6

b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

The bits in 0EA - 0EE turn on the output buffers for the five IO Ports PORTA-PORTE. Setting a bit to 1 turns on the output buffer, setting it to 0 turns the buffer off.

EP01STAT Endpoint 0 and 1 Status SFR 0xBA

b7	b6	b5	b4	b3	b2	b1	b0
0	**0**	**0**	**0**	**0**	**EP1INBSY**	**EP1OUTBSY**	**EP0BSY**
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

GPIFTRIG Endpoint 2,4,6,8 GPIF Slave FIFO Trigger SFR 0xBB

see Section 15.14

b7	b6	b5	b4	b3	b2	b1	b0
DONE	**0**	**0**	**0**	**0**	**R/W**	**EP1**	**EP0**
R/W	R	R	R	R	R/W	R/W	R/W
1	0	0	0	0	x	x	x

GPIFSGLDATH GPIF Data HIGH (16-bit mode only) SFR 0xBD

b7	b6	b5	b4	b3	b2	b1	b0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

GPIFSGLDATLX GPIF Data LOW w/Trigger SFR 0xBE

b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

GPIFSGLDATLNOX GPIF Data LOW w/No Trigger SFR 0xBF

b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R	R	R	R	R	R	R	R
x	x	x	x	x	x	x	x

Most of these SFR registers are also accessible in external RAM space, at the addresses shown in Table 15-3.

Table 15-3. SFR Registers and External Ram Equivalent

SFR Register Name	Hex	External Ram Register Address and Name	
EP2468STAT	AA	E6A3-E6A6	EPxCS
EP24FIFOFLGS	AB	E6A7-E6AA	EPxFIFOFLGS
EP68FIFOFLGS	AC		
EP01STAT	BA	E6A0-E6A2	EP0CS, EP1OUTCS, EP1INCS
GPIFTRIG	BB	E6D4, E6DC, E6E4, E6EC	EPxGPIFTRIG
GPIFSGLDATH	BD	E6F0	XGPIFSGLDATH
GPIFSGLDATLX	BE	E6F1	XGPIFSGLDATLX
GPIFSGLDATLNOX	BF	E6F2	XGPIFSGLDATLNOX

15.4 GPIF Waveform Memories

15.4.1 GPIF Waveform Descriptor Data

WAVEDATA	GPIF Waveform Descriptor 0, 1, 2, 3 Data	E400-E47F*

b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

*Accessible only when IFCFG1:0 = 10.

Figure 15-6. GPIF Waveform Descriptor Data

The four GPIF waveform descriptor tables are stored in this space. See *Chapter 10 "General Programmable Interface (GPIF)"* for details.

15.5 General Configuration Registers

15.5.1 CPU Control and Status

CPUCS	CPU Control and Status	E600

b7	b6	b5	b4	b3	b2	b1	b0
0	**0**	**PORTCSTB**	**CLKSPD1**	**CLKSPD0**	**CLKINV**	**CLKOE**	**0**
R	R	R/W	R/W	R/W	R/W	R/W	R
0	0	0	0	0	0	1	0

Figure 15-7. CPU Control and Status

Bit 5 **PORTCSTB** *PORTC access generates $\overline{RD}$ and $\overline{WR}$ strobes*

The 100- and 128-pin FX2 packages have two output pins, $\overline{RD}$ and $\overline{WR}$, that can be used to synchronize data transfers on I/O PORTC. When PORTCSTB=1, this feature is enabled. Any read of PORTC activates a $\overline{RD}$ strobe, and any write to PORTC activates a $\overline{WR}$ strobe.

The $\overline{RD}$ and $\overline{WR}$ strobes are asserted for two CLKOUT cycles; the $\overline{WR}$ strobe asserts two CLKOUT cycles after the PORTC pins are updated.

If a design uses the 128-pin FX2 and connects off-chip memory to the address and data buses, this bit should be set to zero. This is because the $\overline{RD}$ and $\overline{WR}$ pins are also the standard strobes used to read and write off-chip memory, so normal reads/writes to I/O Port C would disrupt normal accesses to that memory.

Bit 4-3 **CLKSPD1:0** *CPU Clock Speed*

Table 15-4. CPU Clock Speeds

CLKSPD1	CLKSPD0	CPU Clock
0	0	12 MHz (Default)
0	1	24 MHz
1	0	48 MHz
1	1	Reserved

These bits set the CPU clock speed. At power-on-reset, these bits default to 00 (12 MHz). Firmware may modify these bits at any time.

Bit 2 **CLKINV** *Invert CLKOUT Signal*

CLKINV=0: CLKOUT signal not inverted (as shown in all timing diagrams).

CLKINV=1: CLKOUT signal inverted.

Bit 1 **CLKOE** *Drive CLKOUT Pin*

CLKOE=1: CLKOUT pin driven.

CLKOE=0: CLKOUT pin floats.

15.5.2 Interface Configuration (Ports, GPIF, slave FIFOs)

IFCONFIG **Interface Configuration(Ports, GPIF, slave FIFOs)** **E601**

b7	b6	b5	b4	b3	b2	b1	b0
IFCLKSRC	**3048MHZ**	**IFCLKOE**	**IFCLKPOL**	**ASYNC**	**GSTATE**	**IFCFG1**	**IFCFG0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	0	0	0	0	0	0

Figure 15-8. Interface Configuration (Ports, GPIF, slave FIFOs)

Bit 7 **IFCLKSRC** *FIFO/GPIF Clock Source*

This bit selects the clock source for both the FIFOS and GPIF. If IFCLKSRC=0, the external clock on the IFCLK pin is selected. If IFCLKSRC=1 (default), an internal 30- or 48-MHz (default) clock is used.

Bit 6 **3048MHZ** *Internal FIFO/GPIF Clock Frequency*

Table 15-5. Internal FIFO/GPIF Clock Frequency

3048MHZ	FIFO & GPIF Clock
0	30 MHz
1	48 MHz(default)

This bit selects the internal FIFO & GPIF clock frequency.

Bit 5 **IFCLKOE** *IFCLK pin output enable*

0=Tri-state

1=Drive

Bit 4 **IFCLKPOL** *Invert the IFCLK signal*

This bit indicates that the IFCLK signal is inverted.

When IFCLKPOL=0, the clock has the polarity shown in all the timing diagrams in this manual. When IFCLKPOL=1, the clock is inverted.

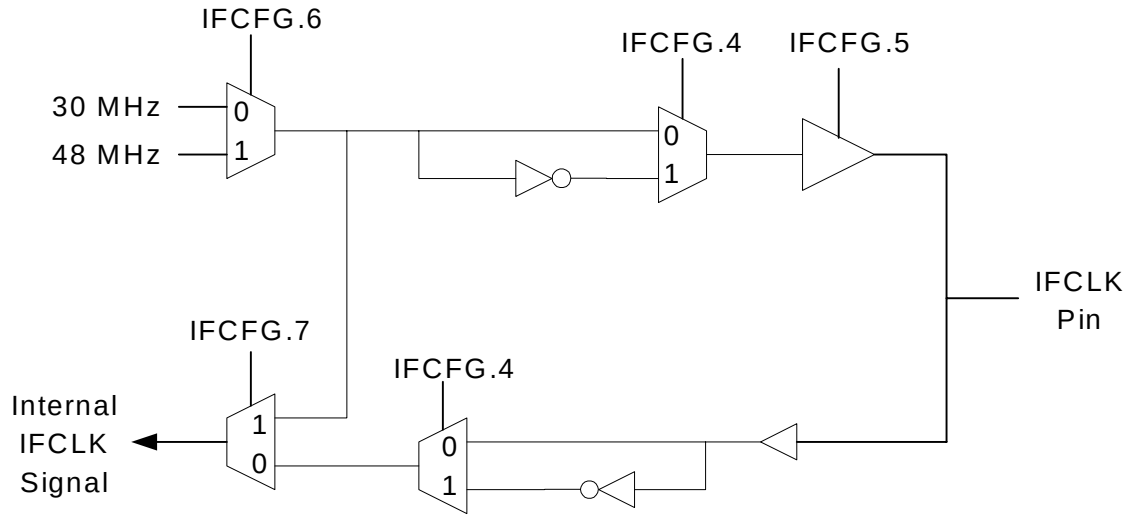


Figure 15-9. IFCLK Configuration

Bit 3 **ASYNC** *FIFO/GPIF Asynchronous Mode*

When ASYNC=0, the FIFO/GPIF operate synchronously: a clock is supplied either internally or externally on the IFCLK pin; the FIFO control signals function as read and write enable signals for the clock signal.

When ASYNC=1, the FIFO/GPIF operate asynchronously: no clock signal input to IFCLK is required; the FIFO control signals function directly as read and write strobes.

Bit 2 **GSTATE** *Drive GSTATE [2:0] on PORTE [2:0]*

When GSTATE=1, three bits in Port E take on the signals shown in Table 15-6. The GSTATE bits, which indicate GPIF states, are used for diagnostic purposes.

Table 15-6. Port E Alternate Functions When GSTATE=1

IO Pin	Alternate Function
PE0	GSTATE[0]
PE1	GSTATE[1]
PE2	GSTATE[2]

Bit 1-0 **IFCFG1:0** *Select Interface Mode (Ports, GPIF, or Slave FIFO)*

Table 15-7. Ports, GPIF, Slave FIFO Select

IFCFG1	IFCFG0	Configuration
0	0	Ports
0	1	Reserved
1	0	GPIF Interface (internal master)
1	1	Slave FIFO Interface (external master)

These bits control the following FX2 interface signals, as shown in Tabl e15-8.

Table 15-8. IFCFG Selection of Port I/O Pin Functions

IFCFG1:0 = 00 (Ports)	IFCFG1:0 = 10 (GPIF Master)	IFCFG1:0 = 11 (Slave FIFO)
PD7	FD[15]	FD[15]
PD6	FD[14]	FD[14]
PD5	FD[13]	FD[13]
PD4	FD[12]	FD[12]
PD3	FD[11]	FD[11]
PD2	FD[10]	FD[10]
PD1	FD[9]	FD[9]
PD0	FD[8]	FD[8]
PB7	FD[7]	FD[7]
PB6	FD[6]	FD[6]
PB5	FD[5]	FD[5]
PB4	FD[4]	FD[4]
PB3	FD[3]	FD[3]
PB2	FD[2]	FD[2]
PB1	FD[1]	FD[1]
PB0	FD[0]	FD[0]
$\overline{\text{INT0}}$ / PA0	**$\overline{\text{INT0}}$ / PA0**	**$\overline{\text{INT0}}$ / PA0**
$\overline{\text{INT1}}$ / PA1	**$\overline{\text{INT1}}$ / PA1**	**$\overline{\text{INT1}}$ / PA1**
PA2	PA2	SLOE
WU2 / PA3	**WU2 / PA3**	**WU2 / PA3**
PA4	PA4	FIFOADR0
PA5	PA5	FIFOADR1
PA6	PA6	PKTEND
PA7	PA7	PA7 / FLAGD / $\overline{\text{SLCS}}$
PC7:0	**PC7:0**	**PC7:0**
PE7:0	**PE7:0**	**PE7:0**

Note: Signals shown in bold type do not change with IFCFG; they are shown for completeness.

15.5.3 Slave FIFO FLAGA-FLAGD Pin Configuration

PINFLAGSAB — **Slave FIFO FLAGA and FLAGB Pin Configuration** — **E602**

see Section 15.14

b7	b6	b5	b4	b3	b2	b1	b0
FLAGB3	**FLAGB2**	**FLAGB1**	**FLAGB0**	**FLAGA3**	**FLAGA2**	**FLAGA1**	**FLAGA0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

PINFLAGSCD — **Slave FIFO FLAGC and FLAGD Pin Configuration** — **E603**

see Section 15.14

b7	b6	b5	b4	b3	b2	b1	b0
FLAGD3	**FLAGD2**	**FLAGD1**	**FLAGD0**	**FLAGC3**	**FLAGC2**	**FLAGC1**	**FLAGC0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	1	0	0	0	0	0	0

Figure 15-10. Slave FIFO FLAGA-FLAGD Pin Configuration

FX2 has four FIFO flag output pins, FLAGA, FLAGB, FLAGC and FLAGD. These flags can be programmed to represent various FIFO flags using four select bits for each FIFO. The PINFLAGSAB register controls the FLAGA and FLAGB signals, and the PINFLAGSCD register controls the FLAGC and FLAGD signal. The 4-bit coding for all four flags is the same, as shown in Table 15-9. In the “FLAGx” notation, “x” can be A, B, C or D.

Table 15-9. FIFO Flag Pin Functions

FLAGx3	FLAGx2	FLAGx1	FLAGx0	Pin Function
0	0	0	0	FLAGA=PF, FLAGB=FF, FLAGC=EF, FLAGD=EP2PF (Actual FIFO is selected by FIFOADR[0,1] pins)
0	0	0	1	Reserved
0	0	1	0	
0	0	1	1	
0	1	0	0	EP2 PF
0	1	0	1	EP4 PF
0	1	1	0	EP6 PF
0	1	1	1	EP8 PF
1	0	0	0	EP2 EF
1	0	0	1	EP4 EF
1	0	1	0	EP6 EF
1	0	1	1	EP8 EF
1	1	0	0	EP2 FF
1	1	0	1	EP4 FF
1	1	1	0	EP6 FF
1	1	1	1	EP8 FF

NOTE: FLAGD defaults to EP2PF (fixed flag).

For the default (0000) selection, the four FIFO flags are indexed as shown in the first table entry. The input pins FIFOADR1 and FIFOADR0 select to which of the four FIFOs the flags correspond. These pins are decoded as follows:

Table 15-10. FIFOADR1 FIFOADR0 Pin Correspondence

FIFOADR1 pin	FIFOADR0 pin	Selected FIFO
0	0	EP2
0	1	EP4
1	0	EP6
1	1	EP8

For example, if FLAGA[3:0]=0000 and the FIFO address pins are driven to [01], then FLAGA is the EP4-Programmable Flag, FLAGB is the EP4-Full Flag, and FLAGC is the EP4-Empty Flag, and FLAGD defaults as PA7. Set PORTACFG.7 = 1 to use FLAGD which by default is EP2PF(fixed flag).

The other (non-zero) values of FLAGx[3:0] allow the designer to independently configure the four flag outputs FLAGA-FLAGD to correspond to any flag—Programmable, Full, or Empty—from any of the four endpoint FIFOS. This allows each flag to be assigned to any of the four FIFOS, including those not currently selected by the FIFOADDR pins. For example, external logic could be filling the EP2IN FIFO with data while also checking the full flag for the EP4OUT FIFO.

15.5.4 FIFO Reset

FIFORESET **Restore FIFOs to Default State** **E604**

see Section 15.14

b7	b6	b5	b4	b3	b2	b1	b0
NAKALL	**0**	**0**	**0**	**EP3**	**EP2**	**EP1**	**EP0**
W	W	W	W	W	W	W	W
x	x	x	x	x	x	x	x

Figure 15-11. Restore FIFOs to Reset State

Write 0x80 to this register to NAK all transfers from the host, then write 0x02, 0x04, 0x06, or 0x08 to reset an individual FIFO (i.e., to restore endpoint FIFO flags and byte counts to their default states), then write 0x00 to restore normal operation.

Bit 3-0 **EP3:0** *Endpoint*

By writing the desired enpoint number (2,4,6,8), FX2 logic resets the individual endpoint.

15.5.5 Breakpoint, Breakpoint Address High, Breakpoint Address Low

BREAKPT **Breakpoint Control** **E605**

b7	b6	b5	b4	b3	b2	b1	b0
0	**0**	**0**	**0**	**BREAK**	**BPPULSE**	**BPEN**	**0**
R	R	R	R	R/W	R/W	R/W	R
0	0	0	0	0	0	0	0

Figure 15-12. Breakpoint Control

Bit 3 **Break** *Enable Breakpoint*

The BREAK bit is set when the CPU address bus matches the address held in the bit breakpoint address registers (0xE606/07). The BKPT pin reflects the state of this bit. Write a “1” to the BREAK bit to clear it. It is not necessary to clear the BREAK bit if the pulse mode bit (BPPULSE) is set.

Bit 2 **BPPULSE** *Breakpoint Pulse Mode*

Set this bit to “1” to pulse the BREAK bit (and BKPT pin) high for 8 CLKOUT cycles when the 8051 address bus matches the address held in the breakpoint address registers. When this bit is set to “0”, the BREAK bit (and BKPT pin) remains high until it is cleared by firmware.

Bit 1 **BPEN** *Breakpoint Enable*

If this bit is “1”, a BREAK signal is generated whenever the 16-bit address lines match the value in the Breakpoint Address Registers (BPADDRH:L). The behavior of the BREAK bit and associated BKPT pin signal is either latched or pulsed, depending on the state of the BPPULSE bit.

BPADDRH Breakpoint Address High E606

b7	b6	b5	b4	b3	b2	b1	b0
A15	**A14**	**A13**	**A12**	**A11**	**A10**	**A9**	**A8**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

Figure 15-13. Breakpoint Address High

BPADDRL Breakpoint Address Low E607

b7	b6	b5	b4	b3	b2	b1	b0
A7	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

Figure 15-14. Breakpoint Address Low

Bit 15-0 **A15:0** *High and Low Breakpoint Address*

When the current 16-bit address (code or XDATA) matches the BPADDRH/BPADDRL address, a breakpoint event occurs. The BPPULSE and BPEN bits in the BREAKPT register control the action taken on a breakpoint event.

15.5.6 230 Kbaud Clock (T0, T1, T2)

UART230 **230 KBaud clock for T1** **E608**

b7	b6	b5	b4	b3	b2	b1	b0
0	**0**	**0**	**0**	**0**	**0**	**230UART1**	**230UART0**
R	R	R	R	R	R	R/W	R/W
0	0	0	0	0	0	0	0

Figure 15-15. 230 Kbaud Internally Generated Reference Clock

Bit 1- 0 **230UARTx** *Set 230 KBaud Operation*

Setting these bits to 1 overrides the timer inputs to the USARTs, and USART0 and USART1 will use the 230 KBaud clock rate. This mode provides the correct frequency to the USART regardless of the CPU clock frequency (12, 24, or 48 MHz).

15.5.7 Slave FIFO Interface Pins Polarity

FIFOPINPOLAR **Slave FIFO Interface Pins Polarity** **E609**

see Section 15.14

b7	b6	b5	b4	b3	b2	b1	b0
0	**0**	**PKTEND**	**SLOE**	**SLRD**	**SLWR**	**EF**	**FF**
R	R	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Figure 15-16. Slave FIFO Interface Pins Polarity

Bit 5 **PKTEND** *FIFO Packet End Polarity*

This bit selects the polarity of the PKTEND FIFO input pin. 0 selects the polarity shown in the data sheet (active low). 1 selects active high.

Bit 4 **SLOE** *FIFO Output Enable Polarity*

This bit selects the polarity of the SLOE FIFO input pin. 0 selects the polarity shown in the data sheet (active low). 1 selects active high.

Bit 3 **SLRD** *FIFO Read Polarity*

This bit selects the polarity of the SLRD FIFO input pin. 0 selects the polarity shown in the data sheet (active low). 1 selects active high.

Bit 2 **SLWR** *FIFO Write Polarity*

This bit selects the polarity of the SLWR FIFO input pin. 0 selects the polarity shown in the data sheet (active low). 1 selects active high.

Bit 1 **EF** *Empty Flag Polarity*

This bit selects the polarity of the SLWR FIFO output pin. 0 selects the polarity shown in the data sheet (active low). 1 selects active high.

Bit 0 **FF** *Full Flag Polarity*

This bit selects the polarity of the SLWR FIFO output pin. 0 selects the polarity shown in the data sheet (active low). 1 selects active high.

15.5.8 Chip Revision ID

REVID **Chip Revision ID** **E60A**

b7	b6	b5	b4	b3	b2	b1	b0
RV7	**RV6**	**RV5**	**RV4**	**RV3**	**RV2**	**RV1**	**RV0**
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

Figure 15-17. Chip Revision ID

Bit 7-0 **RV7:0** *Chip Revision Number*

These register bits define the silicon revision. Consult individual Cypress Semiconductor data sheets for values.

15.5.9 Chip Revision Control

REVCTL **Chip Revision Control** **E60B**

See Section 15.14

b7	b6	b5	b4	b3	b2	b1	b0
0	**0**	**0**	**0**	**0**	**0**	**DYN_OUT**	**ENH_PKT**
R	R	R	R	R	R	R/W	R/W
0	0	0	0	0	0	0	0

Figure 15-18. Chip Revision Control

DYN_OUT and ENH_PKT default to 0 on POR.
Cypress highly recommends setting both bits to 1.

Bit 1 **DYN_OUT** *Disable Auto-Arming at the 0-1 transition of AUTOOUT*

When DYN_OUT=0, the core automatically arms the endpoints when AUTOOUT is switched from 0 to 1. This means that firmware must reset the endpoint (and risk losing endpoint data) when switching between Auto-Out mode and Manual-Out mode.

When DYN_OUT=1, the core disables auto-arming of the endpoints when AUTOOUT transitions from 0 to 1. This feature allows CPU intervention when switching between AUTO and Manual mode without having to reset the endpoint.

Note: When DYN_OUT=1 and AUTOOUT=1, the CPU is responsible for “priming the pump” by initially arming the endpoints (OUTPKTEND w/SKIP=1 to pass packets to host).

Bit 0 **ENH_PKT** *Enhanced Packet Handling*

When ENH_PKT=0, *the CPU can neither source OUT packets nor skip IN packets;* it has only the following capabilities:

- OUT packets: Skip or Commit
- IN packets: Commit or Edit/Source

When ENH_PKT=1, the CPU has additional capabilities:

- OUT packets: Skip, Commit, or Edit/Source
- IN packets: Skip, Commit, or Edit/Source

15.5.10 GPIF Hold Time

GPIFHOLDTIME **E60C**

b7	b6	b5	b4	b3	b2	b1	b0
0	**0**	**0**	**0**	**0**	**0**	**HOLDTIME[1:0]**	
R	R	R	R	R	R	RW	RW
0	0	0	0	0	0	0	0

For any transaction where the GPIF writes data onto FD[15:0], this register determines how long the data is held. Valid choices are 0, ½ or 1 IFCLK cycle. This register applies to *any* data written by the GPIF to FD[15:0], whether through a flow state or not.

For non-flow states, the hold amount is really just a delay of the normal (non-held) presentation of FD[15:0] by the amount specified in HOLDTIME[1:0].

For flow states in which the GPIF is the master on the bus (FLOWSTB.SLAVE = 0), the hold amount is with respect to the activating edge (see FLOW_MASTERSTB_EDGE) of Master Strobe (which will be a CTL pin in this case).

For flow states in which the GPIF is the slave on the bus (FLOWSTB.SLAVE = 1), the hold amount is really just a delay of the normal (non-held) presentation of FD[15:0] by the amount specified in HOLDTIME[1:0] in reaction to the activating edge of Master Strobe (which will be a RDY pin in this case). Note the hold amount is NOT *directly* with respect to the activating edge of Master Strobe in this case. It is with respect to when the data would normally come out in response to Master Strobe including any latency to synchronize Master Strobe.

In all cases, the data will be held for the desired amount even if the ensuing GPIF state calls for the data bus to be tristated. In other words the FD[15:0] output enable will be held by the same amount as the data itself.

Bits 1-0 **HOLDTIME[1:0]** *GPIF Hold Time*

00 = 0 IFCLK cycles

01 = ½ IFCLK cycle

10 = 1 IFCLK cycle

11 = Reserved

15.6 Endpoint Configuration

15.6.1 Endpoint 1-OUT/Endpoint 1-IN Configurations

EP1OUTCFG	**Endpoint 1-OUT Configuration**	**E610**
EP1INCFG	**Endpoint 1-IN Configuration**	**E611**

b7	b6	b5	b4	b3	b2	b1	b0
VALID	**0**	**TYPE1**	**TYPE0**	**0**	**0**	**0**	**0**
R/W	R	R/W	R/W	R	R	R	R
1	0	1	0	0	0	0	0

Figure 15-19. Endpoint 1-OUT/Endpoint 1-IN Configurations

Bit 7 **VALID** *Activate an Endpoint*

Set VALID=1 to activate an endpoint, and VALID=0 to de-activate it. All FX2 endpoints default to VALID. An endpoint whose VALID bit is 0 does not respond to any USB traffic.

Bit 5-4 **TYPE1:0** *Defines the Endpoint Type*

These bits define the endpoint type, as shown in the table below.

Table 15-11. Endpoint Type Definitions

TYPE1	TYPE0	Endpoint Type
0	0	Invalid
0	1	Invalid
1	0	BULK (default)
1	1	INTERRUPT

15.6.2 Endpoint 2, 4, 6 and 8 Configuration

EP2CFG **Endpoint 2 Configuration** **E612**

b7	b6	b5	b4	b3	b2	b1	b0
VALID	**DIR**	**TYPE1**	**TYPE0**	**SIZE**	**0**	**BUF1**	**BUF0**
R/W	R/W	R/W	R/W	R/W	R	R/W	R/W
1	0	1	0	0	0	1	0

Figure 15-20. Endpoint 2 Configuration

EP4CFG **Endpoint 4 Configuration** **E613**

b7	b6	b5	b4	b3	b2	b1	b0
VALID	**DIR**	**TYPE1**	**TYPE0**	**0**	**0**	**0**	**0**
R/W	R/W	R/W	R/W	R	R	R	R
1	0	1	0	0	0	0	0

Figure 15-21. Endpoint 4 Configuration

EP6CFG **Endpoint 6 Configuration** **E614**

b7	b6	b5	b4	b3	b2	b1	b0
VALID	**DIR**	**TYPE1**	**TYPE0**	**SIZE**	**0**	**BUF1**	**BUF0**
R/W	R/W	R/W	R/W	R/W	R	R/W	R/W
1	1	1	0	0	0	1	0

Figure 15-22. Endpoint 6 Configuration

EP8CFG **Endpoint 8 Configuration** **E615**

b7	b6	b5	b4	b3	b2	b1	b0
VALID	**DIR**	**TYPE1**	**TYPE0**	**0**	**0**	**0**	**0**
R/W	R/W	R/W	R/W	R	R	R	R
1	1	1	0	0	0	0	0

Figure 15-23. Endpoint 8 Configuration

These registers configure the large, data-handling FX2 endpoints.

Bit 7 **VALID** *Activate an Endpoint*

Set VALID=1 to activate an endpoint, and VALID=0 to de-activate it. All FX2 endpoints default to valid. An endpoint whose VALID bit is 0 does not respond to any USB traffic.

Bit 6 **DIR** *Sets Endpoint Direction*

0 = OUT, 1 = IN

Bit 5-4 **TYPE** *Defines the Endpoint Type*

These bits define the endpoint type, as shown in the table below. The TYPE bits apply to all of the large-endpoint configuration registers.

Table 15-12. Endpoint Type Definitions

TYPE1	TYPE0	Endpoint Type
0	0	Invalid
0	1	ISOCHRONOUS
1	0	BULK (default)
1	1	INTERRUPT

Bit 3 **SIZE** *Sets Size of Endpoint Buffer*

0 = 512 bytes, 1 = 1024 bytes

Endpoints 4 and 8 can only be 512 bytes. Endpoints 2 and 6 are selectable.

Bit 1-0 **BUF** *Buffering Type/Amount*

The amount of endpoint buffering is presented in Table 15-13.

Table 15-13. Endpoint Buffering Amounts

BUF1	BUF0	Buffering
0	0	Quad
0	1	Invalid
1	0	Double
1	1	Triple

15.6.3 Endpoint 2, 4, 6 and 8/Slave FIFO Configuration

EP2FIFOCFG	**Endpoint 2/Slave FIFO Configuration**	**E618**
see Section 15.14		
EP4FIFOCFG	**Endpoint 4/Slave FIFO Configuration**	**E619**
see Section 15.14		
EP6FIFOCFG	**Endpoint 6/Slave FIFO Configuration**	**E61A**
see Section 15.14		
EP8FIFOCFG	**Endpoint 8/Slave FIFO Configuration**	**E61B**
see Section 15.14		

b7	b6	b5	b4	b3	b2	b1	b0
0	**INFM1**	**OEP1**	**AUTOOUT**	**AUTOIN**	**ZEROLENIN**	**0**	**WORDWIDE**
R	R/W	R/W	R/W	R/W	R/W	R	R/W
0	0	0	0	0	1	0	1

Figure 15-24. Endpoint 2, 4, 6 and 8 /Slave FIFO Configuration

Bit 6 **INFM1** *IN Full Minus One*

When a FIFO configuration register's 'INEARLY' or INFM bit is set to 1, the FIFO flags for that endpoint become valid one sample earlier than when the FULL condition occurs. These bits take effect only when the FIFOS are operating synchronously—according to an internally- or externally-supplied clock. Having the FIFO flag indications a clock early simplifies some synchronous interfaces (applies **only** to IN endpoints).

Bit 5 **OEP1** *OUT Empty Plus One*

When a FIFO configuration register's 'OUTEARLY' or OEP1 bit is set to 1, the FIFO flags for that endpoint become valid one sample earlier than when the EMPTY condition occurs. These bits take effect only when the FIFOS are operating synchronously—according to an internally- or externally-supplied clock. Having the FIFO flag indications a clock early simplifies some synchronous interfaces (applies **only** to OUT endpoints).

Bit 4 **AUTOOUT** *Instantaneous Connection to Endpoint FIFO*

This bit applies only to OUT endpoints.

When AUTOOUT=1, as soon as a buffer fills with USB data, the buffer is automatically and instantaneously committed to the endpoint FIFO bypassing the CPU. The endpoint FIFO flags and buffer counts immediately indicate the change in FIFO status. Refer to the description of the DYN_OUT bit in Section 15.5.9.

When AUTOOUT=0, as soon as a buffer fills with USB data, an endpoint interrupt is asserted. The connection of the buffer to the endpoint FIFO is under control of the firmware, rather than automatically being connected. Using this method, the firmware can inspect the data in OUT packets, and based on what it finds, choose to include that packet in the endpoint FIFO or not. The firmware can even modify the packet data, and then commit it to the endpoint FIFO. Refer to Enhanced Packet Handling in Section 15.5.9.

The SKIP bit (in the EPxBCL registers) chooses between skipping and committing packet data. Refer to OUTPKTEND in Section 15.6.8.

Bit 3 **AUTOIN** *Auto Commit to SIE*

This bit applies only to IN endpoints.

FX2 has EPxAUTOINLEN registers that allow the firmware to configure endpoints to sizes smaller than the physical memory sizes used to implement the endpoint buffers (512 or 1024 bytes). For example, suppose the firmware configures the EP2 buffer to be 1024 bytes, and then sets up EP2 as a 760-byte endpoint by setting EP2AUTOINLEN=760 (this must match the wMaxPacketSize value in the endpoint descriptor). This makes EP2 appear to be a 760-byte endpoint to the USB host, even though EP2's physical buffer is 1024 bytes.

When AUTOIN=1, FX2 automatically packetizes and dispatches IN packets according to the packet length value it finds in the EPxAUTOINLEN registers. In this example, the GPIF (or an external master, if the FX2 is in Slave FIFO mode) could load the EP2 buffer with 950 bytes, which the FX2 logic would then automatically send as two packets, of 760 and 190 bytes. Refer to Enhanced Packet Handling in Section 15.5.9.

When AUTOIN=0, each packet has to initially be manually committed to SIE, (prime the pump). See Section 15.5.9, "Chip Revision Control".

Bit 2 **ZEROLENIN** *Enable Zero-length IN Packets*

When this flag is '1', a zero length packet will be sent when PKTEND is activated and there are no bytes in the current packet. If this flag is '0', zero length packets will not be sent on PKTEND.

Bit 0 **WORDWIDE** *Select Byte/Word FIFOs on PORTB/D Pins*

This bit selects byte or word FIFOS on the PORTB and PORTD pins. The WORD bit applies "for IFCFG=11 or 10".

The OR of all 4 WORDWIDE bits is what causes PORTD to be PORTD or FD[15:8]. The individual WORDWIDE bits indicate how data will be passed for each individual endpoint.

15.6.4 Endpoint 2, 4, 6, 8 AUTOIN Packet Length (High/Low)

EP2AUTOINLENH	**Endpoint 2 AUTOIN Packet Length HIGH**	**E620**
see Section 15.14		
EP6AUTOINLENH	**Endpoint 6 AUTOIN Packet Length HIGH**	**E624**
see Section 15.14		

b7	b6	b5	b4	b3	b2	b1	b0
0	**0**	**0**	**0**	**0**	**PL10**	**PL9**	**PL8**
R	R	R	R	R	R/W	R/W	R/W
0	0	0	0	0	0	1	0

Figure 15-25. Endpoint 2 and 6 AUTOIN Packet Length High

Bit 2-0 **PL10:8** *Packet Length High*

High three bits of Packet Length.

EP4AUTOINLENH	**Endpoint 4 AUTOIN Packet Length HIGH**	**E622**
see Section 15.14		
EP8AUTOINLENH	**Endpoint 8 AUTOIN Packet Length HIGH**	**E626**
see Section 15.14		

b7	b6	b5	b4	b3	b2	b1	b0
0	**0**	**0**	**0**	**0**	**0**	**PL9**	**PL8**
R	R	R	R	R	R	R/W	R/W
0	0	0	0	0	0	1	0

Figure 15-26. Endpoint 4 and 8 AUTOIN Packet Length High

Bit 1-0 **PL9:8** *Packet Length High*

High two bits of Packet Length.

EP2AUTOINLENL *see Section 15.14*	**Endpoint 2 AUTOIN Packet Length LOW**	**E621**
EP4AUTOINLENL *see Section 15.14*	**Endpoint 4 AUTOIN Packet Length LOW**	**E623**
EP6AUTOINLENL *see Section 15.14*	**Endpoint 6 AUTOIN Packet Length LOW**	**E625**
EP8AUTOINLENL *see Section 15.14*	**Endpoint 8 AUTOIN Packet Length LOW**	**E627**

b7	b6	b5	b4	b3	b2	b1	b0
PL7	**PL6**	**PL5**	**PL4**	**PL3**	**PL2**	**PL1**	**PL0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Figure 15-27. Endpoint 2, 4, 6, 8 AUTOIN Packet Length Low

Bit 7-0 **PL7:0** *Packet Length Low*

Low eight bits of packet length.

These registers can be used to set smaller packet sizes than the physical buffer size (refer to the previously described EPxCFG registers). The default packet size is 512 bytes for all endpoints. Note that EP2 and EP6 can have maximum sizes of 1024 bytes, and EP4 and EP8 can have maximum sizes of 512 bytes, to be consistent with the endpoint structure.

15.6.5 Endpoint 2, 4, 6, 8 /Slave FIFO Programmable-Level Flag (High/Low)

EP2FIFOPFH *see Section 15.14*	Endpoint 2/Slave FIFO Programmable-Level Flag HIGH [HIGH SPEED (480 Mbit/Sec) Mode and FULL-SPEED (12 Mbit/Sec) Iso Mode]	E630

b7	b6	b5	b4	b3	b2	b1	b0
DECIS	**PKTSTAT**	**IN: PKTS[2] OUT:PFC12**	**IN: PKTS[1] OUT:PFC11**	**IN: PKTS[0] OUT:PFC10**	**0**	**PFC9**	**PFC8**
R/W	R/W	R/W	R/W	R/W	R	R/W	R/W
1	0	0	0	1	0	0	0

EP2FIFOPFH *see Section 15.14*	Endpoint 2/Slave FIFO Programmable-Level Flag HIGH [FULL SPEED (12 Mbit/Sec) Non-Iso Mode]	E630

b7	b6	b5	b4	b3	b2	b1	b0
DECIS	**PKTSTAT**	**OUT:PFC12**	**OUT:PFC11**	**OUT:PFC10**	**0**	**PFC9**	**IN: PKTS[2] OUT:PFC8**
R/W	R/W	R/W	R/W	R/W	R	R/W	R/W
1	0	0	0	1	0	0	0

Figure 15-28. Endpoint 2/Slave FIFO Programmable Flag High

EP6FIFOPFH — **Endpoint 6/Slave FIFO Programmable-Level Flag HIGH [HIGH SPEED (480 Mbit/Sec) Mode and FULL-SPEED (12 Mbit/Sec) Iso Mode]** — **E634**

see Section 15.14

b7	b6	b5	b4	b3	b2	b1	b0
DECIS	**PKTSTAT**	**IN: PKTS[2] OUT:PFC12**	**IN: PKTS[1] OUT:PFC11**	**IN: PKTS[0] OUT:PFC10**	**0**	**PFC9**	**PFC8**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	1	0	0	0

EP6FIFOPFH — **Endpoint 6/Slave FIFO Programmable-Level Flag HIGH [FULL SPEED (12 Mbit/Sec) Non-Iso Mode]** — **E634**

see Section 15.14

b7	b6	b5	b4	b3	b2	b1	b0
DECIS	**PKTSTAT**	**OUT:PFC12**	**OUT:PFC11**	**OUT:PFC10**	**0**	**PFC9**	**IN: PKTS[2] OUT:PFC8**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	1	0	0	0

Figure 15-29. Endpoint 6/Slave FIFO Programmable Flag High

These registers control the point at which the programmable flag (PF) is asserted for each of the four endpoint FIFOs. The EPxFIFOPFH:L fields are interpreted differently for OUT and IN endpoints.

The threshold point for the programmable-level flag (PF) is configured as follows:

Each FIFO's programmable-level flag (PF) asserts when the FIFO reaches a user-defined fullness threshold. That threshold is configured as follows:

1. For OUT packets: The threshold is stored in PFC12:0. The PF is asserted when the number of bytes *in the entire FIFO* is less than/equal to (DECIS=0) or greater than/equal to (DECIS=1) the threshold.
2. For IN packets, with PKTSTAT = 1: The threshold is stored in PFC9:0. The PF is asserted when the number of bytes written into *the current, not-yet-committed packet in the FIFO* is less than/equal to (DECIS=0) or greater than/equal to (DECIS=1) the threshold.
3. For IN packets, with PKTSTAT = 0: The threshold is stored in two parts: PKTS2:0 holds the number of committed packets, and PFC9:0 holds the number of bytes in the current, not-yet-committed packet. The PF is asserted when the FIFO is at or less full than (DECIS=0), or at or more full than (DECIS=1), the threshold.

By default, FLAGA is the Programmable-Level Flag (PF) for the endpoint currently pointed to by the FIFOADR[1:0] pins. For EP2 and EP4, the default endpoint configuration is BULK, OUT, 512, 2x, and the PF pin asserts when the entire FIFO has greater than/equal to 512 bytes. For EP6 and EP8, the default endpoint configuration is BULK, IN, 512, 2x, and the PF pin asserts when the entire FIFO has less than/equal to 512 bytes.

In other words, the default-configuration PFs for EP2 and EP4 assert when the FIFOs are half-full, and the default-configuration PFs for EP6 and EP8 assert when those FIFOs are half-empty.

In the first example below, bits 5-3 have data that is required to complete the transfer. In the second example, bits 5-3 do not matter - those bits are don't cares because PKTSTAT=1:

Example 1:

Assume a Bulk IN transfer over Endpoint 2 and PKTSTAT=0:

EP2FIFOPFH = 0001 0000

- b6=0 (or PKTSTAT=0): this indicates that the transfer will include packets (as defined by bits 5, 4, and 3) plus bytes (the sum in the flag low register)
- **b5b4b3**=010 binary (or 2 decimal): this indicates the number of packets to expect during the transfer (in this case, two packets…)

EP2FIFOPFL = 0011 0010

- …plus 50 bytes in the currently filling packet
  (the sum of the binary bits in the EP2FIFOPFL register is 2 +16 + 32 = 50 decimal)

DECIS=0, thus PF activates when less than 2 PKTS+50 bytes.

Example 2:

To perform an IN transfer of a number over the same endpoint, set PKTSTAT=1 and write a value into the EP2FIFOPFL register:

EP2FIFOPFH = 01xxx000

EP2FIFOPFL = 75

Setting PKTSTAT=1 causes the PF decision to be based on the byte count alone, ignoring the packet count. This mode is valuable for double-buffered endpoints, where only the byte count of the currently-filling packet is important.

DECIS=0, thus PF activates when less than 75 bytes in the current PKTS.

Bit 1-0 **PFC9:8** *PF Threshold*

Bits 1-0 of EP2FIFOPFH are bits 9-8 of the byte count register.

EP4FIFOPFH — **Endpoint 4/Slave FIFO Programmable-Level Flag HIGH [HIGH SPEED (480 Mbit/Sec) Mode and FULL-SPEED (12 Mbit/Sec) Iso Mode]** — **E632**

see Section 15.14

b7	b6	b5	b4	b3	b2	b1	b0
DECIS	**PKTSTAT**	**0**	**IN: PKTS[1] OUT:PFC10**	**IN: PKTS[0] OUT:PFC9**	**0**	**0**	**PFC8**
R/W	R/W	R	R/W	R/W	R	R	R/W
1	0	0	0	1	0	0	0

EP4FIFOPFH — **Endpoint 4/Slave FIFO Programmable-Level Flag HIGH [FULL SPEED (12 Mbit/Sec) Non-Iso Mode]** — **E632**

see Section 15.14

b7	b6	b5	b4	b3	b2	b1	b0
DECIS	**PKTSTAT**	**0**	**OUT:PFC10**	**OUT:PFC9**	**0**	**0**	**PFC8**
R/W	R/W	R	R/W	R/W	R	R	R/W
1	0	0	0	1	0	0	0

Figure 15-30. Endpoint 4/Slave FIFO Programmable Flag High

EP8FIFOPFH *see Section 15.14*	Endpoint 8/Slave FIFO Programmable-Level Flag HIGH [HIGH SPEED (480 Mbit/Sec) Mode and FULL-SPEED (12 Mbit/Sec) Iso Mode]	E636

b7	b6	b5	b4	b3	b2	b1	b0
DECIS	**PKTSTAT**	**0**	**IN: PKTS[1] OUT:PFC10**	**IN: PKTS[0] OUT:PFC9**	**0**	**0**	**PFC8**
R/W	R/W	R	R/W	R/W	R	R	R/W
0	0	0	0	1	0	0	0

.

EP8FIFOPFH *see Section 15.14*	Endpoint 8/Slave FIFO Programmable-Level Flag HIGH [FULL SPEED (12 Mbit/Sec) Non-Iso Mode]	E636

b7	b6	b5	b4	b3	b2	b1	b0
DECIS	**PKTSTAT**	**0**	**OUT:PFC10**	**OUT:PFC9**	**0**	**0**	**PFC8**
R/W	R/W	R	R/W	R/W	R	R	R/W
0	0	0	0	1	0	0	0

Figure 15-31. Endpoint 8/Slave FIFO Programmable Flag High

Refer to the discussion for EP2PF.

Bit 7 **DECIS** *PF Polarity*

See EP2FIFOPFH and EP6FIFOPFH Register definition.

Bit 6 **PKSTAT** *Packet Status*

See EP2FIFOPFH and EP6FIFOPFH Register definition.

Bit 4-3 **PKTS1:0 / PFC10:9** *PF Threshold*

See EP2FIFOPFH and EP6FIFOPFH Register definition.

Bit 0 **PFC8** *PF Threshold*

See EP2FIFOPFH and EP6FIFOPFH Register definition.

EP2FIFOPFL *see Section 15.14*	**Endpoint 2/Slave FIFO Prog. Flag LOW**	**E631**
EP4FIFOPFL *see Section 15.14*	**Endpoint 4/Slave FIFO Prog. Flag LOW**	**E633**
EP6FIFOPFL *see Section 15.14*	**Endpoint 6/Slave FIFO Prog. Flag LOW**	**E635**
EP8FIFOPFL *see Section 15.14*	**Endpoint 8/Slave FIFO Prog. Flag LOW [HIGH SPEED (480 Mbit/Sec) Mode and FULL-SPEED (12 Mbit/Sec) Iso Mode]**	**E637**

b7	b6	b5	b4	b3	b2	b1	b0
PFC7	**PFC6**	**PFC5**	**PFC4**	**PFC3**	**PFC2**	**PFC1**	**PFC0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

EP2FIFOPFL *see Section 15.14*	**Endpoint 2/Slave FIFO Prog. Flag LOW**	**E631**
EP4FIFOPFL *see Section 15.14*	**Endpoint 4/Slave FIFO Prog. Flag LOW**	**E633**
EP6FIFOPFL *see Section 15.14*	**Endpoint 6/Slave FIFO Prog. Flag LOW**	**E635**
EP8FIFOPFL *see Section 15.14*	**Endpoint 8/Slave FIFO Prog. Flag LOW [FULL SPEED (12 Mbit/Sec) Non-Iso Mode]**	**E637**

b7	b6	b5	b4	b3	b2	b1	b0
IN: PKTS[1] OUT:PFC7	**IN: PKTS[0] OUT:PFC6**	**PFC5**	**PFC4**	**PFC3**	**PFC2**	**PFC1**	**PFC0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Figure 15-32. Endpoint 2, 4, 6, 8/Slave FIFO Programmable Flag Low

Bit 7-0 **PFC7:0** *PF Threshold*

This register contains the current packet bytes to be transferred when the EPxFIFOPFH register requires data.

Bits 9:8 of the byte count are in bits 1:0 of EP2FIFOPFH/EP6FIFOPFH.

Bit 8 of the byte count is bit 0 of EP4FIFOPFH/EP8FIFOPFH.

15.6.5.1 IN Endpoints

For IN endpoints, the Trigger registers can apply to either the full FIFO, comprising multiple packets, or only to the current packet being filled. The PKTSTAT bit controls this choice:

Table 15-14. Interpretation of PF for IN Endpoints

PKTSTAT	PF applies to:	EPxFIFOPFH:L format
0	PKTS + Current packet bytes	PKTS[ ] PBC[ ]
1	Current packet bytes only	PBC[ ]

Example 1:

The following is an example of how you might use the first case.

Assume a Bulk IN transfer over Endpoint 2. For Bulk transfers, the FX2 packet buffer size is 512 bytes. Assume you have reported a MaxPacketSize value of 100 bytes per packet, and you have configured the endpoint for triple-buffering. This means that whenever 100 bytes are loaded into a packet buffer, the FX2 logic commits that packet buffer to the USB interface, essentially adding 100 bytes to the “USB-side” FIFO.

You want to notify the external logic that is filling the endpoint FIFO under two conditions:

- Two of the three packet buffers are full (committed to sending over USB, but not yet sent).
- The current packet buffer is half-full.

In other words, all available IN endpoint buffer space is almost full. You accomplish this by setting:

EP2FIFOPFH = 0001 0000

- b6: PKTSTAT=0 to include packets plus bytes
- b5b4b3=2: two packets…

EP2FIFOPFL = 0011 0010

- …plus 50 bytes in the currently filling packet

Example 2:

If you want the PF to inform the outside interface (the logic that is filling the IN FIFO) whenever the current packet is 75% full, set PKTSTAT=1, and load a packet byte count of 75:

EP2FIFOPFH = 11xxx000

EP2FIFOPFHL = 75

Setting PKTSTAT=1 causes the PF decision to be based on the byte count alone, ignoring the packet count. This mode is valuable for double-buffered endpoints, where only the byte count of the currently-filling packet is important.

15.6.5.2 OUT Endpoints

For OUT endpoints, the PF flag applies to the total number of bytes in the multi-packet FIFO, with no packet count field. Instead of representing byte counts in two segments, a packet count and a byte count for the currently emptying packet, the byte Trigger values indicate total bytes available in the FIFO. Note the discontinuity between PBC10 and PBC9.

Notice that the packet byte counts differ in the upper PBC bits because the endpoints support different FIFO sizes: The EP2 FIFO can be a maximum of 4096 bytes long, the EP6 FIFO can be a maximum of 2048 bytes long, and the EP4 and EP8 FIFOS can be a maximum of 1024 bytes long. The diagram below shows examples of the maximum FIFO sizes.

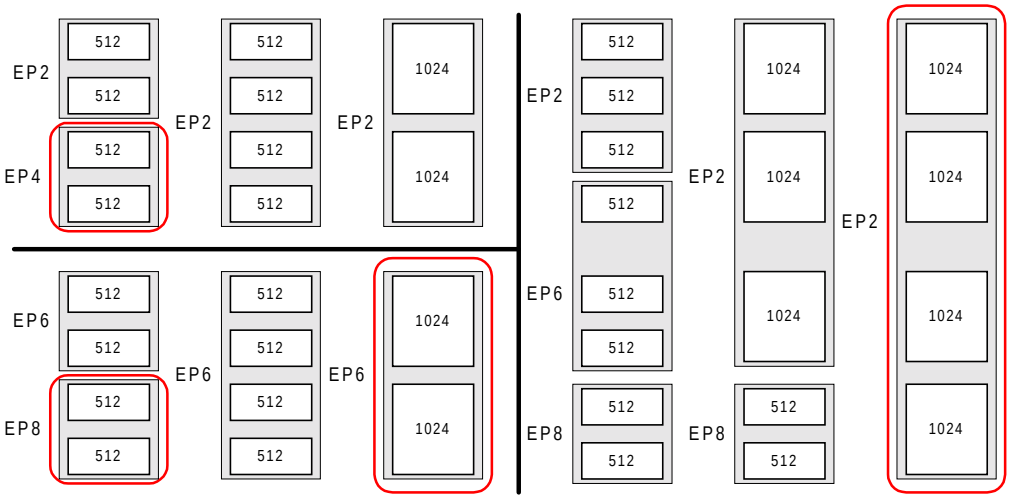


Figure 15-33. Maximum FIFO Sizes

15.6.6 Endpoint 2, 4, 6, 8 ISO IN Packets per Frame

EP2ISOINPKTS	**Endpoint 2 (if ISO) IN Packets Per Frame**	**E640**
EP4ISOINPKTS	**Endpoint 4 (if ISO) IN Packets Per Frame**	**E641**
EP6ISOINPKTS	**Endpoint 6 (if ISO) IN Packets Per Frame**	**E642**
EP8ISOINPKTS	**Endpoint 8 (if ISO) IN Packets Per Frame**	**E643**

b7	b6	b5	b4	b3	b2	b1	b0
0	**0**	**0**	**0**	**0**	**0**	**INPPF1**	**INPPF0**
R	R	R	R	R	R	R/W	R/W
0	0	0	0	0	0	0	1

Figure 15-34. Endpoint ISO IN Packets per Frame

Bit 1-0 **INPPF1:0** *IN Packets per Frame*

For ISOCHRONOUS IN endpoints only, these bits determine the number of packets per micro-frame (high speed mode).

Table 15-15. IN Packets per Microframe

INPPF1	INPPF0	Packets
0	0	Invalid
0	1	1
1	0	2
1	1	3

15.6.7 Force IN Packet End

INPKTEND	**Force IN Packet End**	**E648**

see Section 15.5.9
see Section 15.14

b7	b6	b5	b4	b3	b2	b1	b0
SKIP	**0**	**0**	**0**	**EP3**	**EP2**	**EP1**	**EP0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

Figure 15-35. Force IN Packet End

Bit 7 **SKIP** *Skip Packet*

When ENH_PKT (REVCTL.0) is set to 1, setting this bit to a “1“ will skip the IN packet. Clearing this bit to 0 automatically ‘dispatches’ an IN buffer.

Bit 3-0 **EP3:0** *Endpoint Number*

Duplicates the function of the PKTEND pin. This feature is used only for IN transfers.

By writing the desired endpoint number (2, 4, 6 or 8), FX2 logic automatically ‘dispatches’ an IN buffer, for example, it commits the packet to the USB logic, and writes the accumulated byte count to the endpoint’s byte count register, thus “arming” the IN transfer.

15.6.8 Force OUT Packet End

OUTPKTEND **Force OUT Packet End** **E649**

see Section 15.5.9
see Section 15.14

b7	b6	b5	b4	b3	b2	b1	b0
SKIP	**0**	**0**	**0**	**EP3**	**EP2**	**EP1**	**EP0**
W	W	W	W	W	W	W	W
x	x	x	x	x	x	x	x

Figure 15-36. Force OUT Packet End

Bit 7 **SKIP** *Skip Packet*

When ENH_PKT (REVCTL.0) is set to 1, setting this bit to a “1“ will skip the OUT packet. Clearing this bit to 0 automatically ‘dispatches’ an OUT buffer.

Bits 3:0 **EP3:0** *Endpoint Number*

Replaces the function of EPxBCL.7=1 (Skip). This feature is for OUT transfers. By writing the desired endpoint number (2, 4, 6, or 8), FX2 logic automatically skips or commits an OUT packet (depends on the SKIP bit settings).

Note: This register has no effect if REVCTL.0=0.

15.7 Interrupts

15.7.1 Endpoint 2, 4, 6, 8 Slave FIFO Flag Interrupt Enable/Request

EP2FIFOIE *see Section 15.14*	**EP2 Slave FIFO Flag Interrupt Enable (INT4)**	**E650**
EP4FIFOIE *see Section 15.14*	**EP4 Slave FIFO Flag Interrupt Enable (INT4)**	**E652**
EP6FIFOIE *see Section 15.14*	**EP6 Slave FIFO Flag Interrupt Enable (INT4)**	**E654**
EP8FIFOIE *see Section 15.14*	**EP8 Slave FIFO Flag Interrupt Enable (INT4)**	**E656**

b7	b6	b5	b4	b3	b2	b1	b0
0	**0**	**0**	**0**	**EDGEPF**	**PF**	**EF**	**FF**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Figure 15-37. Endpoint 2, 4, 6, 8 Slave FIFO Flag Interrupt Enable

The Interrupt Registers control all the FX2 Interrupt Enables (IE) and Interrupt requests (IRQ). Interrupt enables and request bits for endpoint FIFO: Programmable Flag (PF), Empty Flag (EF), and Full Flag (FF).

To enable any of these interrupts, INTSETUP.1 (INT4SRC) and INTSETUP.0 must be ‘1’.

Bit 3 **EDGEPF** *Firing Edge Programmable Flag*

When EDGEPF=0, the interrupt fires on the rising edge of the programmable flag.

When EDGEPF=1, the interrupt fires on the falling edge of the programmable flag.

Note: In order for the CPU to vector to the appropriate interrupt service routine, PF must be set to a “1“ and INTSETUP.0=1 (AV4EN) and INTSETUP.1=1 (INT4SRC). Refer to Section 15.7.12

Bit 2 **PF** *Programmable Flag*

When this bit is '1', the programmable flag interrupt is enabled on INT4. When this bit is '0' the programmable flag interrupt is disabled.

Bit 1 **EF** *Empty Flag*

When this bit is '1', the empty flag interrupt is enabled on INT4. When this bit is '0' the empty flag interrupt is disabled.

Bit 0 **FF** *Full Flag*

When this bit is '1', the full flag interrupt is enabled on INT4. When this bit is '0' the full flag interrupt is disabled.

EP2FIFOIRQ	**EP2 Slave FIFO Flag Interrupt Request (INT4)**	**E651**
see Section 15.14		
EP4FIFOIRQ	**EP4 Slave FIFO Flag Interrupt Request (INT4)**	**E653**
see Section 15.14		
EP6FIFOIRQ	**EP6 Slave FIFO Flag Interrupt Request (INT4)**	**E655**
see Section 15.14		
EP8FIFOIRQ	**EP8 Slave FIFO Flag Interrupt Request (INT4)**	**E657**
see Section 15.14		

b7	b6	b5	b4	b3	b2	b1	b0
0	**0**	**0**	**0**	**0**	**PF**	**EF**	**FF**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Figure 15-38. Endpoint 2, 4, 6, 8 Slave FIFO Flag Interrupt Request

Interrupt enables and request bits for endpoint FIFO: Programmable Flag (PF), Empty Flag (EF), and Full Flag (FF).

Bit 2 **PF** *Programmable Flag*

FX2 sets PF to **1** to indicate a “programmable flag” interrupt request. The interrupt source is available in the interrupt vector register IVEC4.

Bit 1 **EF** *Empty Flag*

FX2 sets EF to **1** to indicate an “empty flag” interrupt request. The interrupt source is available in the interrupt vector register IVEC4.

Bit 0 **FF** *Full Flag*

FX2 sets FF to **1** to indicate a “full flag” interrupt request. The interrupt source is available in the interrupt vector register IVEC4.

*Do **not** clear an IRQ Bit by reading an IRQ Register, ORing its contents with a bit mask, and writing back the IRQ Register. This will clear ALL pending interrupts. Instead, simply write the bit mask value (with a “1” in the bit position of the IRQ you want to clear) directly to the IRQ Register.*

15.7.2 IN-BULK-NAK Interrupt Enable/Request

IBNIE **IN-BULK-NAK Interrupt Enable (INT2)** **E658**

b7	b6	b5	b4	b3	b2	b1	b0
0	**0**	**EP8**	**EP6**	**EP4**	**EP2**	**EP1**	**EP0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Figure 15-39. IN-BULK-NAK Interrupt Enable

IBNIRQ **IN-BULK-NAK Interrupt Request (INT2)** **E659**

b7	b6	b5	b4	b3	b2	b1	b0
0	**0**	**EP8**	**EP6**	**EP4**	**EP2**	**EP1**	**EP0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Figure 15-40. IN-BULK-NAK Interrupt Request

Bit 5-0 **EP[8,6,4,2,1,0]** *Endpoint-Specific Interrupt Enable*

These interrupts occur when the host sends an IN token to a Bulk-IN endpoint which has not been loaded with data and armed for USB transfer. In this case the FX2 SIE automatically NAKs the IN token and sets the IBNIRQ bit for the endpoint.

Set **IE=1** to enable the interrupt, and **IE=0** to disable it.

An IRQ bit is set to **1** to indicate an interrupt request. The interrupt source is available in the interrupt vector register IVEC2. **The firmware clears an IRQ bit by writing a 1 to it.**

*Do **not** clear an IRQ bit by reading an IRQ Register, ORing its contents with a bit mask, and writing back the IRQ Register. This will clear ALL pending interrupts. Instead, simply write the bit mask value (with a "1" in the bit position of the IRQ you want to clear) directly to the IRQ Register.*

15.7.3 Endpoint Ping-NAK/IBN Interrupt Enable/Request

NAKIE Endpoint Ping-NAK/IBN Interrupt Enable (INT2) E65A

b7	b6	b5	b4	b3	b2	b1	b0
EP8	**EP6**	**EP4**	**EP2**	**EP1**	**EP0**	**0**	**IBN**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Figure 15-41. Endpoint Ping-NAK/IBN Interrupt Enable

NAKIRQ Endpoint Ping-NAK/IBN Interrupt Request (INT2) E65B

b7	b6	b5	b4	b3	b2	b1	b0
EP8	**EP6**	**EP4**	**EP2**	**EP1**	**EP0**	**0**	**IBN**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Figure 15-42. Endpoint Ping-NAK/IBN Interrupt Request

Bit 7-2 EP[8,6,4,2,1,0] *Ping-NAK INT Enable/Request*

These registers are active only during high speed (480 Mbits/sec) operation.

USB 2.0 improves the USB 1.1 bus bandwidth utilization by implementing a PING-NAK mechanism for OUT transfers. When the host wishes to send OUT data to an endpoint, it first sends a PING token to see if the endpoint is ready, i.e. it has an empty buffer. If a buffer is not available, the SIE returns a NAK handshake. PING-NAK transactions continue to occur until an OUT buffer is available, at which time the FX2 SIE answers a PING with an ACK handshake. Then the host sends the OUT data to the endpoint.

The OUT Ping NAK interrupt indicates that the host is trying to send OUT data, but the SIE responded with a NAK because no endpoint buffer memory is available. The firmware may wish to use this interrupt to free up an OUT endpoint buffer.

Bit 0 **IBN** *IBN INT Enable/Request*

This bit is automatically set when any of the IN bulk endpoints responds to an IN token with a NAK. This interrupt occurs when the host sends an IN token to a bulk IN endpoint which has not yet been armed. Individual enables and requests (per endpoint) are controlled by the IBNIE and IBNIRQ Registers. Write a “1” to this bit to clear the interrupt request.

The IBN INT only fires on a 0-to-1 transition of an “OR” condition of all IBN sources that are enabled.

The firmware clears an IRQ bit by writing a 1 to it.

*Do **not** clear an IRQ bit by reading an IRQ Register, ORing its contents with a bit mask, and writing back the IRQ Register. This will clear ALL pending interrupts. Instead, simply write the bit mask value (with a “1” in the bit position of the IRQ you want to clear) directly to the IRQ Register.*

15.7.4 USB Interrupt Enable/Request

USBIE **USB Interrupt Enables (INT2)** **E65C**

b7	b6	b5	b4	b3	b2	b1	b0
0	**EP0ACK**	**HSGRANT**	**URES**	**SUSP**	**SUTOK**	**SOF**	**SUDAV**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Figure 15-43. USB Interrupt Enables

USBIRQ **USB Interrupt Requests (INT2)** **E65D**

b7	b6	b5	b4	b3	b2	b1	b0
0	**EP0ACK**	**HSGRANT**	**URES**	**SUSP**	**SUTOK**	**SOF**	**SUDAV**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Figure 15-44. USB Interrupt Requests

Bit 6 **EP0ACK** *EndPoint 0 Acknowledge*

Status stage completed

Bit 5 **HSGRANT** *Grant High Speed Access*

The FX2 SIE sets this bit when it has been granted high speed (480 Mbits/sec) access to USB.

Bit 4 **URES** *USB Reset Interrupt Request*

The USB signals a bus reset by driving both D+ and D- low for at least 10 milliseconds. When the USB core detects the onset of USB bus reset, it activates the URES Interrupt Request. The USB core sets this bit to “1” when it detects a USB bus reset. Write a “1” to this bit to clear the interrupt request.

Bit 3 **SUSP** *Suspend Interrupt Request*

If the EZ-USB FX2 detects 3 ms of no bus activity, it activates the SUSP (Suspend) Interrupt Request. The USB core sets this bit to “1” when it detects USB SUSPEND signaling (no bus activity for 3 ms). Write a “1” to this bit to clear the interrupt request.

Bit 2 **SUTOK** *Setup Token*

The USB core sets this bit to “1” when it receives a SETUP token. Write a “1” to this bit to clear the interrupt request.

Bit 1 **SOF** *Start of Frame*

The USB core sets this bit to “1” when it receives a SOF packet. Write a “1” to this bit to clear the interrupt request.

Bit 0 **SUDAV** *SETUP Data Available Interrupt Request*

The USB core sets this bit to “1” when it has transferred the eight data bytes from an endpoint zero SETUP packet into internal registers (at SETUPDAT). Write a “1” to this bit to clear the interrupt request.

*Do **not** clear an IRQ bit by reading an IRQ Register, ORing its contents with a bit mask, and writing back the IRQ Register. This will clear ALL pending interrupts. Instead, simply write the bit mask value (with a “1” in the bit position of the IRQ you want to clear) directly to the IRQ Register.*

15.7.5 Endpoint Interrupt Enable/Request

EPIE **Endpoint Interrupt Enables (INT2)** **E65E**

b7	b6	b5	b4	b3	b2	b1	b0
EP8	**EP6**	**EP4**	**EP2**	**EP1OUT**	**EP1IN**	**EP0OUT**	**EP0IN**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Figure 15-45. Endpoint Interrupt Enables

EPIRQ **Endpoint Interrupt Requests (INT2)** **E65F**

b7	b6	b5	b4	b3	b2	b1	b0
EP8	**EP6**	**EP4**	**EP2**	**EP1OUT**	**EP1IN**	**EP0OUT**	**EP0IN**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Figure 15-46. Endpoint Interrupt Requests

These Endpoint interrupt enable/request registers indicate the pending interrupts for each bulk endpoint. For IN endpoints, the interrupt asserts when the host takes a packet from the endpoint; for OUT endpoints, the interrupt asserts when the host supplies a packet to the endpoint.

The IRQ bits function independently of the Interrupt Enable (IE) bits, so interrupt requests are held whether or not the interrupts are enabled.

*Do **not** clear an IRQ bit by reading an IRQ Register, ORing its contents with a bit mask, and writing back the IRQ Register. This will clear ALL pending interrupts. Instead, simply write the bit mask value (with a "1" in the bit position of the IRQ you want to clear) directly to the IRQ Register.*

15.7.6 GPIF Interrupt Enable/Request

GPIFIE **GPIF Interrupt Enable (INT4)** **E660**

see Section 15.14

b7	b6	b5	b4	b3	b2	b1	b0
0	**0**	**0**	**0**	**0**	**0**	**GPIFWF**	**GPIFDONE**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Figure 15-47. GPIF Interrupt Enable

GPIFIRQ **GPIF Interrupt Request (INT4)** **E661**

see Section 15.14

b7	b6	b5	b4	b3	b2	b1	b0
0	**0**	**0**	**0**	**0**	**0**	**GPIFWF**	**GPIFDONE**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Figure 15-48. GPIF Interrupt Request

Bit 1 **GPIFWF** *FIFO Read/Write Waveform*

GPIF-to-firmware “hook” in Waveform, when waveform descriptor is programmed to assert the GPIFWF interrupt.

Bit 0 **GPIFDONE** *GPIF Idle State*

0 = Transaction in progress.

1 = Transaction Done (GPIF is idle, hence GPIF is ready for next Transaction). Fires IRQ4 if enabled.

The firmware clears an interrupt request bit by writing a “1” to it.

*Do **not** clear an IRQ bit by reading an IRQ Register, ORing its contents with a bit mask, and writing back the IRQ Register. This will clear ALL pending interrupts. Instead, simply write the bit mask value (with a “1” in the bit position of the IRQ you want to clear) directly to the IRQ Register.*

15.7.7 USB Error Interrupt Enable/Request

USBERRIE **USB Error Interrupt Enables (INT2)** **E662**

b7	b6	b5	b4	b3	b2	b1	b0
ISOEP8	**ISOEP6**	**ISOEP4**	**ISOEP2**	**0**	**0**	**0**	**ERRLIMIT**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Figure 15-49. USB Error Interrupt Enables

USBERRIRQ **USB Error Interrupt Request (INT2)** **E663**

b7	b6	b5	b4	b3	b2	b1	b0
ISOEP8	**ISOEP6**	**ISOEP4**	**ISOEP2**	**0**	**0**	**0**	**ERRLIMIT**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Figure 15-50. USB Error Interrupt Request

Bit 7-4 **ISOEP[8,6,4,2]** *ISO Error Packet*

The ISO EP Flag is set when:

- ISO OUT data PIDs arrive out of sequence (applies to high speed only).
- An ISO OUT packet was dropped because no buffer space was available for an OUT packet (in either full- or high-speed modes).

Bit 0 **ERRLIMIT** *Error Limit*

ERRLIMIT counts USB bus errors—CRC, bit stuff, etc., and triggers the interrupt when the programmed limit (0-15) is reached.

The firmware clears an interrupt request bit by writing a “1” to it. (See the following Note).

*Do **not** clear an IRQ bit by reading an IRQ Register, ORing its contents with a bit mask, and writing back the IRQ Register. This will clear ALL pending interrupts. Instead, simply write the bit mask value (with a “1” in the bit position of the IRQ you want to clear) directly to the IRQ Register.*

15.7.8 USB Error Counter Limit

ERRCNTLIM **USB Error Counter and Limit** **E664**

b7	b6	b5	b4	b3	b2	b1	b0
EC3	**EC2**	**EC1**	**EC0**	**LIMIT3**	**LIMIT2**	**LIMIT1**	**LIMIT0**
R	R	R	R	R/W	R/W	R/W	R/W
x	x	x	x	0	1	0	0

Figure 15-51. USB Error Counter and Limit

Bit 7-4 **EC3:0** *USB Error Count*

Error count has a maximum value of 15.

Bit 3-0 **LIMIT3:0** *Error Count Limit*

USB bus error count and limit. The firmware can enable the interrupt to cause an interrupt when the limit is reached. The default limit count is 4.

15.7.9 Clear Error Count

CLRERRCNT **Clear Error Count EC3:0** **E665**

b7	b6	b5	b4	b3	b2	b1	b0
x	**x**	**x**	**x**	**x**	**x**	**x**	**x**
W	W	W	W	W	W	W	W
x	x	x	x	x	x	x	x

Figure 15-52. Clear Error Count EC3:0

Write 0xFF to this register to clear the EC (Error Count) bits in the ERRCNTLIM Register.

15.7.10 INT 2 (USB) Autovector

INT2IVEC **INTERRUPT 2 (USB) Autovector** **E666**

b7	b6	b5	b4	b3	b2	b1	b0
0	**I2V4**	**I2V3**	**I2V2**	**I2V1**	**I2V0**	**0**	**0**
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

Figure 15-53. INT 2 (USB) Autovector

Bit 6-2 **I2V4:0** *INT 2 Autovector*

To save the code and processing time required to sort out which USB interrupt occurred, the USB core provides a second level of interrupt vectoring, called Autovectoring. When the CPU takes a USB interrupt, it pushes the program counter onto its stack, and then executes a jump to address 43, where it expects to find a jump instruction to the INT2 service routine.

I2V indicates the source of an interrupt from the USB Core. When the USB core generates an INT2 (USB) Interrupt Request, it updates INT2IVEC to indicate the source of the interrupt. The interrupt sources are encoded on I2V4:0.

15.7.11 INT 4 (slave FIFOs & GPIF) Autovector

INT4IVEC **Interrupt 4 (slave FIFOs & GPIF) Autovector** **E667**

b7	b6	b5	b4	b3	b2	b1	b0
1	**0**	**I4V3**	**I4V2**	**I4V1**	**I4V0**	**0**	**0**
R	R	R	R	R	R	R	R
1	0	0	0	0	0	0	0

Figure 15-54. INT 4 (slave FIFOs & GPIF) Autovector

Bit 5-2 **I4V3:0** *INT 4 Autovector*

To save the code and processing time required to sort out which FIFO interrupt occurred, the USB core provides a second level of interrupt vectoring, called Autovectoring. When the CPU takes a USB interrupt, it pushes the program counter onto its stack, and then executes a jump to address 53, where it expects to find a jump instruction to the INT4 service routine.

I4V indicates the source of an interrupt from the USB Core. When the USB core generates an INT4 (FIFO/GPIF) Interrupt Request, it updates INT4IVEC to indicate the source of the interrupt. The interrupt sources are encoded on I2V3:0.

15.7.12 INT 2 and INT 4 Setup

INTSETUP **INT 2 & INT 4 Setup** **E668**

b7	b6	b5	b4	b3	b2	b1	b0
0	**0**	**0**	**0**	**AV2EN**	**0**	**INT4SRC**	**AV4EN**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Figure 15-55. INT 2 and INT 4 Setup

Bit 3 **AV2EN** *INT2 Autovector Enable*

To streamline the code that deals with the USB interrupts, this bit enables autovectoring on INT2.

Bit 1 **INT4SRC** *INT 4 Source*

If 0, INT4 is supplied by the pin. If **INT4SRC** = 1:INT4 supplied internally from FIFO/GPIF sources.

Bit 0 **AV4EN** *INT4 Autovector Enable*

To streamline the 8051 code that deals with the FIFO interrupts, this bit enables autovectoring on INT4.

15.8 Input/Output Registers

15.8.1 I/O PORTA Alternate Configuration

PORTACFG I/O PORTA Alternate Configuration E670

b7	b6	b5	b4	b3	b2	b1	b0
FLAGD	**SLCS**	**0**	**0**	**0**	**0**	**INT1**	**INT0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Figure 15-56. I/O PORTA Alternate Configuration

Note: Bit 3 is the WU2EN bit in the Wakeup register.

The PORTxCFG register selects alternate functions for the PORTx pins.

Bit 7 FLAGD *FlagD Alternate Configuration*

If IFCFG1:0=11, setting this bit to '1' configures the PA7 pin as FLAGD, a programmable FIFO flag.

Bit 6 SLCS *$\overline{\text{SLCS}}$ Alternate Configuration*

If IFCFG1:0=11, setting this bit to '1' configures the PA7 pin as $\overline{\text{SLCS}}$, the slave-FIFO chip-select.

Bit 1-0 INT1:0 *Interrupts Enabled for Alternate Configuration*

Setting these bits to '1' configures these PORTA pins as the INT1 or INT0 pins.

Note: Bits PORTACFG.7 and PORTACFG.6 both affect pin PA7. If both bits are set, FLAGD takes precedence.

15.8.2 I/O PORTC Alternate Configuration

PORTCCFG I/O PORTC Alternate Configuration E671

b7	b6	b5	b4	b3	b2	b1	b0
GPIFA7	**GPIFA6**	**GPIFA5**	**GPIFA4**	**GPIFA3**	**GPIFA2**	**GPIFA1**	**GPIFA0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Figure 15-57. I/O PORTC Alternate Configuration

Bit 7-0 GPIFA7:0 *Enable GPIF Address Pins*

Set these pins to “1” to configure this port to output the lower address of enabled GPIF address pins. Additional bit set in PORTECFG, bit 7.

Set these pins to “0” to configure this as Port C.

15.8.3 I/O PORTE Alternate Configuration

PORTECFG I/O PORTE Alternate Configuration E672

b7	b6	b5	b4	b3	b2	b1	b0
GPIFA8	**T2EX**	**INT6**	**RXD1OUT**	**RXD0OUT**	**T2OUT**	**T1OUT**	**T0OUT**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Figure 15-58. I/O PORTE Alternate Configuration

Bit 7 GPIFA8 *Enable GPIF Address Pin*

GPIF address bit 8 pin. Set these pin to “1” to configure this port to output the high address of enabled GPIF address pins.

Set these pin to “0” to configure this as Port E.

Bit 6 T2EX *Timer 2 Counter*

Timer/Counter 2 Capture/Reload Input.

Bit 5 **INT6** *INT6 Interrupt Request*

Setting this bit to '1' configures this Port E pin as INT6.

Bit 4 **RXD1OUT** *Mode 0: USART1 Synchronous Data Output*

Mode 0: USART1 Synchronous Data Output.

Bit 3 **RXD0OUT** *Mode 0: USART0 Synchronous Data Output*

Mode 0: USART0 Synchronous Data Output.

Bit 2-0 **T2OUT, T1OUT, T0OUT** *Serial Data*

Serial mode 0 provides synchronous, half-duplex serial communication. For Serial Port 0, serial data output occurs on the RXD0OUT pin, serial data is received on the RXD0 pin, and the TXD0 pin provides the shift clock for both transmit and receive. Mode 0: Clock Output Modes 1-3: Serial Port 0 Data Output.

15.8.4 I²C Compatible Bus Control and Status

I2CS **I²C-Compatible Bus Control and Status** **E678**

b7	b6	b5	b4	b3	b2	b1	b0
START	**STOP**	**LASTRD**	**ID1**	**ID0**	**BERR**	**ACK**	**DONE**
R/W	R/W	R/W	R	R	R	R	R
0	0	0	x	x	0	0	0

Figure 15-59. I²C-Compatible Bus Control and Status

Bit 7 **START** *Signal START Condition*

Set the START bit to “1” to prepare a bus transfer. If START=1, the next write to I2DAT will generate the start condition followed by the serialized byte of data in I2DAT. The firmware loads byte data into I2DAT after setting the START bit. The bus controller clears the START bit during the ACK interval.

Bit 6 **STOP** *Signal STOP Condition*

Set STOP=1 to terminate a bus transfer. The bus controller clears the STOP bit after completing the STOP condition. If the firmware sets the STOP bit during a byte transfer, the STOP condition will be generated immediately following the ACK phase of the byte transfer. If no byte transfer is occurring when the STOP bit is set, the STOP condition will be carried out immediately on the bus. Data should not be written to I2CS or I2DAT until the STOP bit returns low.

Bit 5 **LASTRD** *Last Data Read*

To read data over the I²C compatible bus, a bus master floats the SDA line and issues clock pulses on the SCL line. After every eight bits, the master drives SDA low for one clock to indicate ACK. To signal the last byte of the read transfer, the master floats SDA at ACK time to instruct the slave to stop sending. This is controlled by setting LastRD=1 before reading the last byte of a read transfer. The bus controller clears the LastRD bit at the end of the transfer (at ACK time).

Bit 4-3 **ID1:0** *Boot EEPROM ID*

These bits are set by the boot loader to indicate whether an 8-bit address or 16-bit address EEPROM at slave address 000 or 001 was detected at power-on. Normally, they are used for debug purposes only.

Bit 2 **BERR** *Bus Error*

This bit indicates a bus error. BERR=1 indicates that there was bus contention, which results when an outside device drives the bus low when it should not, or when another bus master wins arbitration, taking control of the bus. BERR is cleared when the IDATA register is read or written.

Bit 1 **ACK** *Acknowledge Bit*

Every ninth SCL or a write transfer the slave indicates reception of the byte by asserting ACK. The bus controller floats SDA during this time, samples the SDA line, and updates the ACK bit with the complement of the detected value. ACK=1 indicates acknowledge, and ACK=0 indicates not-acknowledge. The USB core updates the ACK bit at the same time it sets DONE=1. The ACK bit should be ignored for read transfers on the bus.

Bit 0 **DONE** *Transfer DONE*

The bus controller sets this bit whenever it completes a byte transfer, right after the ACK stage. The controller also generates an Interrupt Request (INT3) when it sets the DONE bit. The bus controller automatically clears the DONE bit and the Interrupt Request bit whenever theI2DAT register is read or written.

15.8.5 I²C-Compatible Bus Data

I2DAT **I²C-Compatible Bus Data** **E679**

b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

Figure 15-60. I²C-Compatible Bus Data

Bit 7-0 **Data** *Data Bits*

Eight bits of data; triggers bus transactions.

15.8.6 I²C-Compatible Bus Control

I2CTL **I²C-Compatible Bus Control** **E67A**

b7	b6	b5	b4	b3	b2	b1	b0
0	**0**	**0**	**0**	**0**	**0**	**STOPIE**	**400KHZ**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Figure 15-61. I²C-Compatible Bus Control

Bit 1 **STOPIE** *STOP Interrupt Enable Bit*

The STOP bit Interrupt Request is activated when the STOP bit makes a 1-0 transition.To enable this interrupt, set the STOPIE bit in the I²CMODE Register. The firmware determines the interrupt source by checking the DONE and STOP bits in the I2CS Register.

Bit 0 **400KHZ** *High-speed I²C Compatible Bus*

For I²C-compatible peripherals that support it, the I²C-compatible bus can run at 400 KHz. For compatibility, the bus powers-up at the 100-KHz frequency. If 400KHZ=0, the I²C-compatible bus operates at approximately 100 KHz. If 400KHZ=1, the I²C-compatible bus operates at approximately 400 KHz. This bit is copied to the I²CCTL register bit 0, which is read-write to the firmware. Thus the I²C-compatible bus speed is initially set by the EEPROM bit, and may be changed subsequently by firmware.

15.8.7 AUTOPOINTERs 1 and 2 MOVX access

XAUTODAT1	**AUTOPTR1 MOVX access**	**E67B**
XAUTODAT2	**AUTOPTR2 MOVX access**	**E67C**

b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

Figure 15-62. AUTOPTR1 & AUTOPTR2 MOVX access (when APTREN=1)

Bit 7-0 **Data** *AUTODATAx*

Data read or written to the xAUTODATn register accesses the memory addressed by the AUTOPTRHn/Ln registers, and optionally increments the address after the read or write.

15.9 UDMA CRC Registers

For complete Flowstate / UDMA information, please contact the Cypress Semiconductor Applications Department.

UDMACRCH E67D

see Section 15.14

b7	b6	b5	b4	b3	b2	b1	b0
CRC[15:8]							
RW	RW	RW	RW	RW	RW	RW	RW
0	1	0	0	1	0	1	0

UDMACRCL E67E

see Section 15.14

b7	b6	b5	b4	b3	b2	b1	b0
CRC[7:0]							
RW	RW	RW	RW	RW	RW	RW	RW
1	0	1	1	1	0	1	0

These two registers are strictly for debug purposes. The CRC represented by these registers is calculated based on the rules defined in the ATAPI specification for UDMA transfers. It is calculated automatically by the GPIF as data is transferred on FD[15:0].

These registers will return the live calculation of the CRC at any point in the transfer, but will be reset to the seed value of 0x4ABA upon the GPIF entering the IDLE state. These registers are writable; thus the currently calculated CRC including the seed value can be overwritten at any time.

UDMACRCQUALIFIER E67F

b7	b6	b5	b4	b3	b2	b1	b0
QENABLE	**0**	**0**	**0**	**QSTATE**	**QSIGNAL[2:0]**		
RW	R	R	R	RW	RW	RW	RW
0	0	0	0	0	0	0	0

This register only applies to UDMA IN transactions that are host terminated. Otherwise, this register can be completely ignored.

This register covers a very specific and potentially nonexistent (from a typical system implementation standpoint*) UDMA CRC situation. However rare the situation may be, it is still allowed by the ATAPI specification and thus must be considered and solved by this register.

The ATAPI specification says that if the host (in this case the GPIF) terminates a UDMA IN transaction, that the device (e.g., the disk drive) is allowed to send up to 3 more words after the host deactivates the HDMARDY signal. These “dribble” words may not be of interest to the host and thus may be discarded. However, CRC must still be calculated on them since the host and the device must compare and match the CRC at the end of the transaction to consider the transfer error-free.

The GPIF normally only calculates CRC on words that are written into the FIFO (and not discarded). This poses a problem since in this case some words will be discarded but still must be included in the CRC calculation. This register gives a way to have the GPIF calculate CRC on the extra discarded words as well.

The user would program this register in the following way. The QENABLE bit would be set to 1. The QSIGNAL[2:0] field would be programmed to select the CTL pin that coincides with the UDMA STOP signal. The QSTATE bit would be programmed to be 0. This would instruct the GPIF to calculate CRC on any DSTROBE edges from the device when STOP=0, which solves the problem.

Bit 7 QENABLE

This bit enables the CRC qualifier feature, and thus the other bits in this register.

Bit 3 QSTATE

This bit says what state the CRC qualifier signal (selected by QSIGNAL[2:0] below) must be in to allow CRC to be calculated on words being written into the GPIF.

Bits 2-0 QSIGNAL[2:0]

These bits select which of the CTL[5:0] pins is the CRC qualifier signal.

* - A typical UDMA system will have the device, instead of the host, terminate UDMA IN transfers thus completely avoiding this situation.

15.10 USB Control

15.10.1 USB Control and Status

USBCS **USB Control and Status** **E680**

b7	b6	b5	b4	b3	b2	b1	b0
HSM	**0**	**0**	**0**	**DISCON**	**NOSYNSOF**	**RENUM**	**SIGRSUME**
R	R	R	R	R/W	R/W	R/W	R/W
x	0	0	0	0	0	0	0

Figure 15-63. USB Control and Status

Bit 7 **HSM** *High Speed Mode*

If HSM=1, the SIE is operating in High Speed Mode, 480 bits/sec. 0-1 transition of this bit causes a HSGRANT interrupt request.

Bit 3 **DISCON** *Signal a Disconnect on the $\overline{DISCON}$ Pin*

DISCON is one of the EZ-USB FX2 control bits in the USBCS (USB Control and Status) Register that control the ReNumeration process. Setting this bit to “1” will disconnect from the USB bus by removing the internal 1.5 K pull-up resistor from the D+. A boot EEPROM may be used to default this bit to 1 at startup time. This bit will also reset several registers. See *Chapter 7 "Resets"* for details.

Bit 2 **NOSYNSOF** *Disable Synthesizing Missing SOFs*

If set to 1, disable synthesizing missing SOFs.

Bit 1 **RENUM** *Renumerate*

This bit controls whether USB device requests are handled by firmware or automatically by the FX2. When RENUM=0, the USB core handles all device requests. When RENUM=1, the firmware handles all device requests except Set_Address. Set RENUM=1 during a bus disconnect to transfer USB control to the firmware. The FX2 automatically sets RENUM=1 under two conditions:

1. Completion of a “C2” boot load
2. When external memory is used (EA=1) and no boot EEPROM is used.

Bit 0 **SIGRSUME** *Signal Remote Device Resume*

Set SIGRSUME=1 to drive the “K” state onto the USB bus. This should be done only by a device that is capable of remote wakeup, and then only during the SUSPEND state.To signal RESUME, set SIGRSUME=1, waits 10-15 ms, then sets SIGRSUME=0.

15.10.2 Enter Suspend State

SUSPEND **Put Chip into SUSPEND State** **E681**

b7	b6	b5	b4	b3	b2	b1	b0
x	**x**	**x**	**x**	**x**	**x**	**x**	**x**
W	W	W	W	W	W	W	W
x	x	x	x	x	x	x	x

Figure 15-64. Enter Suspend State

Bit 7-0 **Suspend** *Enable Suspend Regardless of Bus State*

Write 0xFF to prepare the chip for standby without having to wait for a Bus Suspend.

15.10.3 Wakeup Control & Status

WAKEUPCS **Wakeup Control & Status** **E682**

b7	b6	b5	b4	b3	b2	b1	b0
WU2	**WU**	**WU2POL**	**WUPOL**	**0**	**DPEN**	**WU2EN**	**WUEN**
R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
x	x	0	0	0	1	0	1

Figure 15-65. Wakeup Control & Status

FX2 has two pins that can be activated by external logic to take FX2 out of standby. These pins are called WAKEUP and WU2.

Bit 7 **WU2** *Wakeup Initiated from WU2 Pin*

The FX2 sets this status bit to1 when wakeup was initiated by the WU2 pin. Write a 1 to this bit to clear it.

Bit 6 **WU** *Wakeup Initiated from WU Pin*

The FX2 sets this bit to1 when wakeup was initiated by the WU pin. Write a 1 to this bit to clear it.

Bit 5 **WU2POL** *Polarity of WU2 Pin*

Polarity of the WU2 input pin. 0 = active low, 1 = active high.

Bit 4 **WUPOL** *Polarity of WU Pin*

Polarity of the WU input pin. 0 = active low, 1 = active high.

Bit 2 **DPEN** *Enable/Disable DPLUS Wakeup*

Activity on the USB DPLUS signal normally initiates a USB wakeup sequence.

0=Disable
1=Enable

Bit 1 **WU2EN** *Enable WU2 Wakeup*

WU2EN =1: enable wakeup from WU2 pin.

Bit 0 **WUEN** *Enable WU Wakeup*

WUEN=1: enable wakeup from the WAKEUP pin.

15.10.4 Data Toggle Control

TOGCTL **Data Toggle Control** **E683**

b7	b6	b5	b4	b3	b2	b1	b0
Q	**S**	**R**	**IO**	**EP3**	**EP2**	**EP1**	**EP0**
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Figure 15-66. Data Toggle Control

Bit 7 **Q** *Data Toggle Value*

Q=0 indicates DATA0 and Q=1 indicates DATA1, for the endpoint selected by the I/O and EP3:0 bits. Write the endpoint select bits (IO and EP3:0), before reading this value.

Bit 6 **S** *Set Data Toggle to DATA1*

After selecting the desired endpoint by writing the endpoint select bits (IO and EP3:0), set S=1 to set the data toggle to DATA1. The endpoint selection bits should not be changed while this bit is written.

Bit 5 **R** *Set Data Toggle to DATA0*

Set R=1 to set the data toggle to DATA0. The endpoint selection bits should not be changed while this bit is written.

Bit 4 **IO** *Select IN or OUT Endpoint*

Set this bit to select an endpoint direction prior to setting its R or S bit. IO=0 selects an OUT endpoint, IO=1 selects an IN endpoint.

Bit 3-0 **EP3:0** *Select Endpoint*

Set these bits to select an endpoint prior to setting its R or S bit. Valid values are 0, 1, 2, 4, 6, and 8.

15.10.5 USB Frame Count High

USBFRAMEH **USB Frame Count HIGH** **E684**

b7	b6	b5	b4	b3	b2	b1	b0
0	**0**	**0**	**0**	**0**	**FC10**	**FC9**	**FC8**
R	R	R	R	R	R	R	R
0	0	0	0	0	x	x	x

Figure 15-67. USB Frame Count HIGH

Bit 2-0 **FC10:8** *High Bits for USB Frame Count*

Every millisecond the host sends a SOF token indicating “Start Of Frame,” along with an 11-bit incrementing frame count. The EZ-USB FX2 copies the frame count into these registers at every SOF. One use of the frame count is to respond to the USB SYNC_FRAME Request. If the USB core detects a missing or garbled SOF, it generates an internal SOF and increments USBFRAMEL-USBRAMEH.

15.10.6 USB Frame Count Low

USBFRAMEL **USB Frame Count LOW** **E685**

b7	b6	b5	b4	b3	b2	b1	b0
FC7	**FC6**	**FC5**	**FC4**	**FC3**	**FC2**	**FC1**	**FC0**
R	R	R	R	R	R	R	R
x	x	x	x	x	x	x	x

Figure 15-68. USB Frame Count Low

Bit 7-0 **FC7:0** *Low Byte for USB Frame Count*

Every millisecond the host sends a SOF token indicating “Start Of Frame,” along with an 11-bit incrementing frame count. The EZ-USB FX2 copies the frame count into these registers at every SOF. One use of the frame count is to respond to the USB SYNC_FRAME Request. If the USB core detects a missing or garbled SOF, it generates an internal SOF and increments USBFRAMEL-USBRAMEH.

15.10.7 USB Microframe Count

MICROFRAME **USB Microframe Count, 0-7** **E686**

b7	b6	b5	b4	b3	b2	b1	b0
0	**0**	**0**	**0**	**0**	**MF2**	**MF1**	**MF0**
R	R	R	R	R	R	R	R
0	0	0	0	0	x	x	x

Figure 15-69. USB Microframe Count

Bit 2-0 **MF2:0** *Last Occurring Microframe*

MICROFRAME contains a count 0-7 which indicates which of the 8 125-microsecond microframes last occurred. This register is active only when FX2 is operating at high speed (480 Mbits/sec).

15.10.8 USB Function Address

FNADDR **USB Function Address** **E687**

b7	b6	b5	b4	b3	b2	b1	b0
0	**FA6**	**FA5**	**FA4**	**FA3**	**FA2**	**FA1**	**FA0**
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

Figure 15-70. USB Function Address

Bit 6-0 **FA6:0** *USB Function Address*

During the USB enumeration process, the host sends a device a unique 7-bit address, which the USB core copies into this register. There is normally no reason for the CPU to know its USB device address because the USB Core automatically responds only to its assigned address.

15.11 Endpoints

15.11.1 Endpoint 0 (Byte Count High)

EP0BCH **Endpoint 0 Byte Count HIGH** **E68A**

b7	b6	b5	b4	b3	b2	b1	b0
(BC15)	**(BC14)**	**(BC13)**	**(BC12)**	**(BC11)**	**(BC10)**	**(BC9)**	**(BC8)**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

Figure 15-71. Endpoint 0 (Byte Count High)

Bit 7-0 **BC15:8** *High Order Byte Count*

Even though the EP0 buffer is only 64 bytes, the EP0 byte count is expanded to 16 bits to allow using the SUDPTR with a custom length, instead of USB-dictated length (from Setup Data Packet and number of requested bytes). The byte count bits in parentheses apply only when SDPAUTO (SUDPTRCTL.0) = 0.

The SIE normally determines how many bytes to send over EP0 in response to a device request by taking the smaller of (a) the wLength field in the SETUP packet, and (b) the number of bytes available for transfer (byte count).

15.11.2 Endpoint 0 Control and Status (Byte Count Low)

EP0BCL	Endpoint 0 Byte Count Low	E68B

b7	b6	b5	b4	b3	b2	b1	b0
(BC7)	**BC6**	**BC5**	**BC4**	**BC3**	**BC2**	**BC1**	**BC0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

Figure 15-72. Endpoint 0 Control and Status (Byte Count Low)

Bit 7-0 **BC7:0** *Low Order Byte Count*

Even though the EP0 buffer is only 64 bytes, the EP0 byte count is expanded to 16 bits to allow using the SUDPTR with a custom length, instead of USB-dictated length (from Setup Data Packet and number of requested bytes). The byte count bits in parentheses apply only when SDPAUTO (SUDPTRCTL.0) = 0.

15.11.3 Endpoint 1 OUT and IN Byte Count

EP1OUTBC	Endpoint 1 OUT Byte Count	E68D
EP1INBC	Endpoint 1 IN Byte Count	E68F

b7	b6	b5	b4	b3	b2	b1	b0
0	**BC6**	**BC5**	**BC4**	**BC3**	**BC2**	**BC1**	**BC0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	x	x	x	x	x	x	x

Figure 15-73. Endpoint 1 OUT/IN Byte Count

Bit 7-0 **BC6:0** *Endpoint 1 IN/OUT Byte Count*

15.11.4 Endpoint 2 and 6 Byte Count High

EP2BCH **Endpoint 2 Byte Count HIGH** **E690**

see Section 15.14

EP6BCH **Endpoint 6 Byte Count HIGH** **E698**

see Section 15.14

b7	b6	b5	b4	b3	b2	b1	b0
0	**0**	**0**	**0**	**0**	**BC10**	**BC9**	**BC8**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	x	x	x

Figure 15-74. Endpoint 2 and 6 Byte Count High

Bit 1-0 **BC9:8** *Endpoint 2, 6 Byte Count High*

EP2 and EP6 can be either 512 or 1024 bytes. These are the high 2 bits of the byte-count.

15.11.5 Endpoint 4 and 8 Byte Count High

EP4BCH **Endpoint 4 Byte Count HIGH** **E694**

see Section 15.14

EP8BCH **Endpoint 8 Byte Count HIGH** **E69C**

see Section 15.14

b7	b6	b5	b4	b3	b2	b1	b0
0	**0**	**0**	**0**	**0**	**0**	**BC9**	**BC8**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	x	x

Figure 15-75. Endpoint 4 and 5 Byte Count High

Bit 0 **BC8** *Endpoint 4, 8 Byte Count High*

EP4 and EP8 can be 512 bytes only. This is the most significant bit of the byte-count.

15.11.6 Endpoint 2, 4, 6, 8 Byte Count Low

EP2BCL	**Endpoint 2 Byte Count LOW**	**E691**
see Section 15.14		
EP4BCL	**Endpoint 4 Byte Count LOW**	**E695**
see Section 15.14		
EP6BCL	**Endpoint 6 Byte Count LOW**	**E699**
see Section 15.14		
EP8BCL	**Endpoint 8 Byte Count LOW**	**E69D**
see Section 15.14		

b7	b6	b5	b4	b3	b2	b1	b0
BC7	**BC6**	**BC5**	**BC4**	**BC3**	**BC2**	**BC1**	**BC0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

Figure 15-76. Endpoint 2, 4, 6, 8 Byte Count Low

Bit 7-0 **BC7:0** *Byte Count*

Low byte count for Endpoints 2, 4, 6, and 8.

15.11.7 Endpoint 0 Control and Status

EP0CS	**Endpoint 0 Control and Status**	**E6A0**

b7	b6	b5	b4	b3	b2	b1	b0
HSNAK	**0**	**0**	**0**	**0**	**0**	**BUSY**	**STALL**
R/W	R/W	R/W	R/W	R/W	R/W	R	R/W
1	0	0	0	0	0	0	0

Figure 15-77. Endpoint 0 Control and Status

Bit 7 **HSNAK** *Hand Shake w/ NAK*

The STATUS stage consists of an empty data packet with the opposite direction of the data stage, or an IN if there was no data stage. This empty data packet gives the device a chance to ACK, NAK, or STALL the entire CONTROL transfer. Write a “1” to the NAK (handshake NAK) bit to clear it and instruct the USB core to ACK the STATUS stage. The HSNAK bit holds

off completing the CONTROL transfer until the device has had time to respond to a request.Clear the HSNAK bit (by writing “1” to it) to instruct the USB core to ACK the status stage of the transfer.

Bit 1 **BUSY** *EP0 Buffer Busy*

BUSY is a read-only bit that is automatically cleared when a SETUP token arrives. The BUSY bit is set by writing a byte count to EP0BCL.

Bit 0 **STALL** *EP0 Stalled*

STALL is a read/write bit that is automatically cleared when a SETUP token arrives. The STALL bit is set by writing a “1” to the register bit.

While STALL=1, the USB core sends the STALL PID for any IN or OUT token. This can occur in either the data or handshake phase of the CONTROL transfer.

To indicate an endpoint stall on endpoint zero, set both STALL and HSNAK bits. Setting the STALL bit alone causes endpoint zero to NAK forever because the host keeps the control transfer pending.

15.11.8 Endpoint 1 OUT/IN Control and Status

EP1OUTCS	**Endpoint 1 OUT Control and Status**	**E6A1**
EP1INCS	**Endpoint 1 IN Control and Status**	**E6A2**

b7	b6	b5	b4	b3	b2	b1	b0
0	**0**	**0**	**0**	**0**	**0**	**BUSY**	**STALL**
R/W	R/W	R/W	R/W	R/W	R/W	R	R/W
0	0	0	0	0	0	0	0

Figure 15-78. Endpoint 1 OUT/IN Control and Status

Bit 1 **BUSY** *OUT/IN Endpoint Busy*

The BUSY bit indicates the status of the endpoint’s OUT Buffer EP1OUTBUF. The USB core sets BUSY=0 when the host data is available in the OUT buffer. The firmware sets BUSY=1 by loading the endpoint’s byte count register.

When BUSY=1, endpoint RAM data is invalid—the endpoint buffer has been emptied by the firmware and is waiting for new OUT data from the host, or it is the process of being loaded over the USB. BUSY=0 when the USB OUT transfer is complete and endpoint RAM data in

EP1OUTBUF is available for the firmware to read. USB OUT tokens for the endpoint are NAK'd while BUSY=1 (the firmware is still reading data from the OUT endpoint).

A 1-to-0 transition of BUSY (indicating that the firmware can access the buffer) generates an interrupt request for the OUT endpoint. After the firmware reads the data from the OUT endpoint buffer, it loads the endpoint's byte count register with any value to re-arm the endpoint, which automatically sets BUSY=1. This enables the OUT transfer of data from the host in response to the next OUT token. The CPU should never read endpoint data while BUSY=1.

The BUSY bit, also indicates the status of the endpoint's IN Buffer EP1INBUF. The USB core sets BUSY=0 when the endpoint's IN buffer is empty and ready for loading by the firmware. The firmware sets BUSY=1 by loading the endpoint's byte count register.

When BUSY=1, the firmware should not write data to an IN endpoint buffer, because the endpoint FIFO could be in the act of transferring data to the host over the USB. BUSY=0 when the USB IN transfer is complete and endpoint RAM data is available for firmware access. USB IN tokens for the endpoint are NAK'd while BUSY=0 (the firmware is still loading data into the endpoint buffer).

A 1-to-0 transition of BUSY (indicating that the firmware can access the buffer) generates an interrupt request for the IN endpoint. After the firmware writes the data to be transferred to the IN endpoint buffer, it loads the endpoint's byte count register with the number of bytes to transfer, which automatically sets BUSY=1. This enables the IN transfer of data to the host in response to the next IN token. Again, the CPU should never load endpoint data while BUSY=1.

The firmware writes a "1" to an IN endpoint busy bit to disarm a previously armed endpoint. (This sets BUSY=0.) The firmware should do this only after a USB bus reset, or when the host selects a new interface or alternate setting that uses the endpoint. This prevents stale data from a previous setting from being accepted by the host's first IN transfer that uses the new setting.

Bit 0 STALL *OUT/IN Endpoint Stalled*

Each bulk endpoint (IN or OUT) has a STALL bit in its Control and Status Register (bit 0). If the CPU sets this bit, any requests to the endpoint return a STALL handshake rather than ACK or NAK. The Get Status-Endpoint Request returns the STALL state for the endpoint indicated in byte 4 of the request. Note that bit 7 of the endpoint number EP (byte 4) specifies direction.

15.11.9 Endpoint 2 Control and Status

EP2CS — Endpoint 2 Control and Status — E6A3

b7	b6	b5	b4	b3	b2	b1	b0
0	**NPAK2**	**NPAK1**	**NPAK0**	**FULL**	**EMPTY**	**0**	**STALL**
R	R	R	R	R	R	R	R/W
0	0	1	0	1	0	0	0

Figure 15-79. Endpoint 2 Control and Status

Bit 6-4 NPAK2:0 *Number of Packets in FIFO*

The number of packets in the FIFO. 0-4 Packets.

Bit 3 FULL *Endpoint FIFO Full*

This bit is set to “1” to indicate that the Endpoint FIFO is full.

Bit 2 EMPTY *Endpoint FIFO Empty*

This bit is set to “1” to indicate that the Endpoint FIFO is empty.

Bit 0 STALL *ENDPOINT STALL*

Set this bit to “1” to *stall* an endpoint, and to “0” to clear a stall.

When the stall bit is “1,” the USB core returns a STALL handshake for all requests to the endpoint. This notifies the host that something unexpected has happened.

15.11.10 Endpoint 4 Control and Status

EP4CS — Endpoint 4 Control and Status — E6A4

b7	b6	b5	b4	b3	b2	b1	b0
0	**0**	**NPAK1**	**NPAK0**	**FULL**	**EMPTY**	**0**	**STALL**
R	R	R	R	R	R	R	R/W
0	0	1	0	1	0	0	0

Figure 15-80. Endpoint 4 Control and Status

Bit 5-4 **NPAK1:0** *Number of Packets in FIFO*

The number of packets in the FIFO. 0-2 Packets.

Bit 3 **FULL** *Endpoint FIFO Full*

This bit is set to “1” to indicate that the Endpoint FIFO is full.

Bit 2 **EMPTY** *Endpoint FIFO Empty*

This bit is set to “1” to indicate that the Endpoint FIFO is empty.

Bit 0 **STALL** *ENDPOINT STALL*

Set this bit to “1” to *stall* an endpoint, and to “0” to clear a stall.

When the stall bit is “1,” the USB core returns a STALL handshake for all requests to the endpoint. This notifies the host that something unexpected has happened.

15.11.11 Endpoint 6 Control and Status

EP6CS **Endpoint 6 Control and Status** **E6A5**

b7	b6	b5	b4	b3	b2	b1	b0
0	**NPAK2**	**NPAK1**	**NPAK0**	**FULL**	**EMPTY**	**0**	**STALL**
R	R	R	R	R	R	R	R/W
0	0	0	0	0	1	0	0

Figure 15-81. Endpoint 6 Control and Status

Bit 6-4 **NPAK2:0** *Number of Packets in FIFO*

The number of packets in the FIFO. 0-4 Packets.

Bit 3 **FULL** *Endpoint FIFO Full*

This bit is set to “1” to indicate that the Endpoint FIFO is full.

Bit 2 **EMPTY** *Endpoint FIFO Empty*

This bit is set to “1” to indicate that the Endpoint FIFO is empty.

Bit 0 **STALL** *ENDPOINT STALL*

Set this bit to “1” to *stall* an endpoint, and to “0” to clear a stall.

When the stall bit is “1,” the USB core returns a STALL handshake for all requests to the endpoint. This notifies the host that something unexpected has happened.

15.11.12 Endpoint 8 Control and Status

EP8CS — Endpoint 8 Control and Status — E6A6

b7	b6	b5	b4	b3	b2	b1	b0
0	**0**	**NPAK1**	**NPAK0**	**FULL**	**EMPTY**	**0**	**STALL**
R	R	R	R	R	R	R	R/W
0	0	0	0	0	1	0	0

Figure 15-82. Endpoint 8 Control and Status

Bit 5-4 NPAK1:0 *Number of Packets in FIFO*

The number of packets in the FIFO. 0-2 Packets.

Bit 3 FULL *Endpoint FIFO Full*

This bit is set to “1” to indicate that the Endpoint FIFO is full.

Bit 2 EMPTY *Endpoint FIFO Empty*

This bit is set to “1” to indicate that the Endpoint FIFO is empty.

Bit 0 STALL *ENDPOINT STALL*

Set this bit to “1” to *stall* an endpoint, and to “0” to clear a stall.

When the stall bit is “1,” the USB core returns a STALL handshake for all requests to the endpoint. This notifies the host that something unexpected has happened.

15.11.13 Endpoint 2 and 4 Slave FIFO Flags

EP2FIFOFLGS	Endpoint 2 Slave FIFO Flags	E6A7
EP4FIFOFLGS	Endpoint 4 Slave FIFO Flags	E6A8

b7	b6	b5	b4	b3	b2	b1	b0
0	**0**	**0**	**0**	**0**	**PF**	**EF**	**FF**
R	R	R	R	R	R	R	R
0	0	0	0	0	0	1	0

Figure 15-83. Endpoint 2 and 4 Slave FIFO Flags

Bit 2 **PF** *Programmable Flag*

State of the EP2/EP4 Programmable Flag.

Bit 1 **EF** *Empty Flag*

State of the EP2/EP4 Empty Flag.

Bit 0 **FF** *Full Flag*

State of the EP2/EP4 Full Flag.

FIFOPINPOLAR settings do not affect the behavior of these bits.

15.11.14 Endpoint 6 and 8 Slave FIFO Flags

EP6FIFOFLGS	Endpoint 6 Slave FIFO Flags	E6A9
EP8FIFOFLGS	Endpoint 8 Slave FIFO Flags	E6AA

b7	b6	b5	b4	b3	b2	b1	b0
0	**0**	**0**	**0**	**0**	**PF**	**EF**	**FF**
R	R	R	R	R	R	R	R
0	0	0	0	0	1	1	0

Figure 15-84. Endpoint 6 and 8 Slave FIFO Flags

Bit 2 **PF** *Programmable Flag*

State of the EP6/EP8 Programmable Flag.

The default value is different from EP2FIFOFLGS.PF and EP4FIFOFLGS.PF.

Bit 1 **EF** *Empty Flag*

State of the EP6/EP8 Empty Flag.

Bit 0 **FF** *Full Flag*

State of the EP6/EP8 Full Flag.

FIFOPINPOLAR settings do not affect the behavior of these bits.

15.11.15 Endpoint 2 Slave FIFO Byte Count High

EP2FIFOBCH Endpoint 2 Slave FIFO Total Byte Count HIGH E6AB

b7	b6	b5	b4	b3	b2	b1	b0
0	**0**	**0**	**BC12**	**BC11**	**BC10**	**BC9**	**BC8**
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

Figure 15-85. Endpoint 2 Slave FIFO Total Byte Count High

Bit 4-0 **BC12:8** *Byte Count High*

Total number of bytes in Endpoint FIFO. Maximum of 4096 bytes.

15.11.16 Endpoint 6 Slave FIFO Total Byte Count High

EP6FIFOBCH Endpoint 6 Slave FIFO Total Byte Count HIGH E6AF

b7	b6	b5	b4	b3	b2	b1	b0
0	**0**	**0**	**0**	**BC11**	**BC10**	**BC9**	**BC8**
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

Figure 15-86. Endpoint 6 Slave FIFO Total Byte Count High

Bit 3-0 **BC11:8** *Byte Count High*

Total number of bytes in Endpoint FIFO. Maximum of 2048 bytes.

15.11.17 Endpoint 4 and 8 Slave FIFO Byte Count High

EP4FIFOBCH	**Endpoint 4 Slave FIFO Total Byte Count HIGH**	**E6AD**
EP8FIFOBCH	**Endpoint 8 Slave FIFO Total Byte Count HIGH**	**E6B1**

b7	b6	b5	b4	b3	b2	b1	b0
0	**0**	**0**	**0**	**0**	**BC10**	**BC9**	**BC8**
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

Figure 15-87. Endpoint 4 and 8 Slave FIFO Byte Count High

Bit 2-0 **BC10:8** *Byte Count High*

Total number of bytes in Endpoint FIFO. Maximum of 1024 bytes.

15.11.18 Endpoint 2, 4, 6, 8 Slave FIFO Byte Count Low

EP2FIFOBCL	**Endpoint 2 Slave FIFO Total Byte Count LOW**	**E6AC**
EP4FIFOBCL	**Endpoint 4 Slave FIFO Total Byte Count LOW**	**E6AE**
EP6FIFOBCL	**Endpoint 6 Slave FIFO Total Byte Count LOW**	**E6B0**
EP8FIFOBCL	**Endpoint 8 Slave FIFO Total Byte Count LOW**	**E6B2**

b7	b6	b5	b4	b3	b2	b1	b0
BC7	**BC6**	**BC5**	**BC4**	**BC3**	**BC2**	**BC1**	**BC0**
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

Figure 15-88. Endpoint 2, 4, 6, 8 Slave FIFO Byte Count Low

Bit 7-0 **BC7:0** *Byte Count High*

Low byte for number of bytes in Endpoint FIFO.

15.11.19 Setup Data Pointer High and Low Address

SUDPTRH **Setup Data Pointer High Address Byte** **E6B3**

b7	b6	b5	b4	b3	b2	b1	b0
A15	**A14**	**A13**	**A12**	**A11**	**A10**	**A9**	**A8**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

Figure 15-89. Setup Data Pointer High Address Byte

SUDPTRL **Setup Data Pointer Low Address Byte** **E6B4**

b7	b6	b5	b4	b3	b2	b1	b0
A7	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
x	x	x	x	x	x	x	0

Figure 15-90. Setup Data Pointer Low Address Byte

Bit 15-0 **A15:0** *Setup Data Pointer*

This buffer is used as a target or source by the Setup Data Pointer and it must be WORD (2-byte) aligned. This 16-bit pointer, SUDPTRH:L provides hardware assistance for handling CONTROL IN transfers.

When the firmware loads SUDPTRL, the SIE automatically responds to IN commands with the appropriate data. If SDPAUTO=1, the length field is taken from the packet or descriptor. If SDPAUTO=0, SUDPTRL triggers a send to the host and the length is taken from the EP0BCH and EP0BCL bytes.

15.11.20 Setup Data Pointer Auto

SUDPTRCTL **Setup Data Pointer AUTO Mode** **E6B5**

b7	b6	b5	b4	b3	b2	b1	b0
0	**0**	**0**	**0**	**0**	**0**	**0**	**SDPAUTO**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	1

Figure 15-91. Setup Data Pointer AUTO Mode

Bit 0 **SDPAUTO** *Setup Data Pointer Auto Mode*

To send a block of data using the Setup Data Pointer, the block's starting address is loaded into SUDPTRH:L. The block length must previously have been set; the method for accomplishing this depends on the state of the SDPAUTO bit:

- **SDPAUTO = 0 (Manual Mode):** Used for general-purpose block transfers. Firmware writes the block length to EP0BCH:L.
- **SDPAUTO = 1 (Auto Mode):** Used for sending Device, Configuration, String, Device Qualifier, and Other Speed Configuration descriptors *only*. The block length is automatically read from the "length" field of the descriptor itself; no explicit loading of EP0BCH:L is necessary.

Writing to SUDPTRL starts the transfer; the FX2 automatically sends the entire block, packetizing as necessary.

*When SDPAUTO = 0, writing to EP0BCH:L only sets the block length; it does not arm the transfer (the transfer is armed by writing to SUDPTRL). Therefore, before performing an EP0 transfer which does **not** use the Setup Data Pointer (i.e., one which is meant to be armed by writing to EP0BCL), SDPAUTO **must** be set to 1.*

15.11.21 Setup Data - 8 Bytes

SETUPDAT **8 Bytes of Setup Data** **E6B8-E6BF**

b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R	R	R	R	R	R	R	R
x	x	x	x	x	x	x	x

Figure 15-92. Setup Data - 8 Bytes

The setup data bytes are defined as follows:

SETUPDAT[0] = bmRequestType

SETUPDAT[1] = bmRequest

SETUPDAT[2:3] = wValue

SETUPDAT[4:5] = wIndex

SETUPDAT[6:7] = wLength

This buffer contains the 8 bytes of SETUP packet data from the most recently received CONTROL transfer.

The data in SETUPBUF is valid when the SUDAV (Setup Data Available) Interrupt Request bit is set.

15.12 General Programmable Interface (GPIF)

15.12.1 GPIF Waveform Selector

GPIFWFSELECT **Waveform Selector** **E6C0**

b7	b6	b5	b4	b3	b2	b1	b0
SINGLEWR1	**SINGLEWR0**	**SINGLERD1**	**SINGLERD0**	**FIFOWR1**	**FIFOWR0**	**FIFORD1**	**FIFORD0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	0	0	1	0	0

Figure 15-93. GPIF Waveform Selector

Bit 7-6 **SINGLEWR1:0** *Single Write Waveform Index*

Index to the Waveform Program to run when a “Single Write” is triggered by the firmware.

Bit 5-4 **SINGLERD1:0** *Single Read Waveform Index*

Index to the Waveform Program to run when a “Single Read” is triggered by the firmware.

Bit 3-2 **FIFOWR1:0** *FIFO Write Waveform Index*

Index to the Waveform Program to run when a “FIFO Write” is triggered by the firmware.

Bit 1-0 **FIFORD1:0** *FIFO Read Waveform Index*

Index to the Waveform Program to run when a “FIFO Read” is triggered by the firmware. Select waveform 0 [00], 1 [01], 2 [10] or 3 [11].

15.12.2 GPIF Done and Idle Drive Mode

GPIFIDLECS **GPIF Done, GPIF Idle Drive Mode** **E6C1**

b7	b6	b5	b4	b3	b2	b1	b0
DONE	**0**	**0**	**0**	**0**	**0**	**0**	**IDLEDRV**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	0	0	0	0	0	0	0

Figure 15-94. GPIF Done and Idle Drive

Bit 7 **DONE** *GPIF Idle State*

0 = Transaction in progress.
1 = Transaction Done (GPIF is idle, hence GPIF is ready for next Transaction). Fires IRQ4 if enabled.

Bit 0 **IDLEDRV** *Set Data Bus when GPIF Idle*

When the GPIF is idle:

0 = Tri-state the Data Bus.
1 = Drive the Data Bus.

15.12.3 CTL Outputs

GPIFIDLECTL **CTL Output States in Idle** **E6C2**

b7	b6	b5	b4	b3	b2	b1	b0
0/ CTLOE3	**0/ CTLOE2**	**CTL5/ CTLOE1**	**CTL4/ CTLOE0**	**CTL3**	**CTL2**	**CTL1**	**CTL0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

Figure 15-95. CTL Output States in Idle

Bit 7-4 **CTLOE3:0** *CTL Output Enables*
Bit 5-0 **CTL5:0** *CTL Output States*

See GPIFCTLCFG, below.

GPIFCTLCFG **CTL Output Drive Type** **E6C3**

b7	b6	b5	b4	b3	b2	b1	b0
TRICTL	**0**	**CTL5**	**CTL4**	**CTL3**	**CTL2**	**CTL1**	**CTL0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Figure 15-96. CTL Output Drive Type

Bit 7 **TRICTL** *Number Active Outputs/Tristating*
Bit 5-0 **CTL5:0** *CTL Output Drive Type*

The GPIF Control pins (CTL[5:0]) have several output modes:

- CTL[3:0] can act as CMOS outputs (optionally tristatable) or open-drain outputs.
- CTL[5:4] can act as CMOS outputs or open-drain outputs.
  If CTL[3:0] are configured to be tristatable, CTL[5:4] are not available.

Table 15-16. CTL[5:0] Output Modes

TRICTL (GPIFCTLCFG.7)	GPIFCTLCFG[6:0]	CTL[3:0]	CTL[5:4]
0	0	CMOS, Not Tristatable	CMOS, Not Tristatable
0	1	Open-Drain	Open-Drain
1	X	CMOS, Tristatable	Not Available

During the IDLE State, the state of CTL[5:0] depends on the following register bits:

- TRICTL (GPIFCTLCFG.7).
- GPIFCTLCFG[5:0]
- GPIFIDLECTL[5:0].

The combination of these bits defines CTL5:0 during IDLE as follows:

- If TRICTL is 0, GPIFIDLECTL[5:0] directly represent the output states of CTL5:0 during the IDLE State. The GPIFCTLCFG[5:0] bits determine whether the CTL5:0 outputs are CMOS or open-drain: If GPIFCTLCFG.x = 0, CTLx is CMOS; if GPIFCTLCFG.x = 1, CTLx is open-drain.
- If TRICTL is 1, GPIFIDLECTL[7:4] are the output enables for the CTL[3:0] signals, and GPIFIDLECTL[3:0] are the output values for CTL[3:0]. CTL4 and CTL5 are unavailable in this mode.

Table 15-17 illustrates this relationship.

Table 15-17. Control Outputs (CTLx) During the IDLE State

TRICTL	Control Output	Output State	Output Enable
0	CTL0	GPIFIDLECTL.0	N/A (CTL Outputs are always enabled when TRICTL = 0)
	CTL1	GPIFIDLECTL.1	
	CTL2	GPIFIDLECTL.2	
	CTL3	GPIFIDLECTL.3	
	CTL4	GPIFIDLECTL.4	
	CTL5	GPIFIDLECTL.5	
1	CTL0	GPIFIDLECTL.0	GPIFIDLECTL.4
	CTL1	GPIFIDLECTL.1	GPIFIDLECTL.5
	CTL2	GPIFIDLECTL.2	GPIFIDLECTL.6
	CTL3	GPIFIDLECTL.3	GPIFIDLECTL.7
	CTL4	N/A (CTL4 and CTL5 are not available when TRICTL = 1)	
	CTL5		

15.12.4 GPIF Address High

GPIFADRH **GPIF Address High** **E6C4**

see Section 15.14

b7	b6	b5	b4	b3	b2	b1	b0
0	**0**	**0**	**0**	**0**	**0**	**0**	**GPIFA8**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Figure 15-97. GPIF Address High

Bit 0 **GPIF A8** *High Bit of GPIF Address*

See GPIFADDRL.

15.12.5 GPIF Address Low

GPIFADRL **GPIF Address Low** **E6C5**

see Section 15.14

b7	b6	b5	b4	b3	b2	b1	b0
GPIFA7	**GPIFA6**	**GPIFA5**	**GPIFA4**	**GPIFA3**	**GPIFA2**	**GPIFA1**	**GPIFA0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Figure 15-98. GPIF Address Low

Bit 7-0 **GPIFA7:0** *Lower 8 bits of GPIF Address*

Data written to this register immediately appears as the bus address on the ADR[7:0] pins.

15.12.6 GPIF Flowstate Registers

For complete Flowstate / UDMA information, please contact the Cypress Semiconductor Applications Department.

FLOWSTATE **E6C6**

b7	b6	b5	b4	b3	b2	b1	b0
FSE	**0**	**0**	**0**	**0**	**FS[2:0]**		
0	0	0	0	0	0	0	0
RW	R	R	R	R	RW	RW	RW

Any one (and only one) of the seven GPIF states in a waveform can be programmed to be the flow state. This register defines which state, if any, in the next invoked GPIF waveform will be the flow state.

Bit 7 **FSE** *Global Flow State Enable*

Global enable for the flow state. When it is disabled all flow state registers are don't care and the next waveform invocation will not cause a flow state to be used.

Bit 2-0 **FS[2:0]** *Flow State Selection*

Defines which GPIF state is the flow state. Valid values are 0-6.\

FLOWLOGIC E6C7

b7	b6	b5	b4	b3	b2	b1	b0
LFUNC[1:0]		**TERMA[2:0]**			**TERMB[2:0]**		
0	0	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

The bit definitions for this register are analogous to the bit definitions in the RDY LOGIC opcode in a waveform descriptor. Except, instead of controlling the branching for a decision point, it controls the freezing or flowing of data on the bus in a flow state.

The user defines the states of CTL[5:0] for when the flow logic equals 0 and 1 (see FLOWEQ0_CTL and FLOWEQ1_CTL). This is useful in activating or deactivating protocol ready signals to hold off an external master (where the GPIF is acting like a slave) in response to internal FIFO flags warning of an impending underflow or overflow situation.

In the case where the GPIF is the master, then the user also defines whether Master Strobe (a CTL pin in this case; see FLOWSTB) toggles (reads or writes data on the bus) when the flow logic evaluates to a 1 or a 0. This is useful for the GPIF to consider protocol ready signals from the slave as well as FIFO flags to decide when to clock data out of or into the FIFOs and when to freeze the data flow instead.

It should be noted that this flow logic does not replace the decision point logic defined in a waveform descriptor. The decision point logic in a waveform descriptor is still used to decide when to branch out of the flow state. The decision point logic can use an entirely different pair of ready signals than the flow logic in making its decisions.

Bits 7-6 **LFUNC[1:0]** *Flow State Logic Function*

00 = A AND B
01 = A OR B
10 = A XOR B
11 = !A AND B

Since the flow logic decision can be based on the output being a 1 or a 0, NAND, NOR, XNOR and !(!A AND B) operations can be achieved as well. Note that !(!A AND B) is the same as (A OR !B).

Bits 5-3 **TERMA[2:0]** *Flow State Logic-Function Arguments*
Bits 2-0 **TERMB[2:0]**

0 = RDY[0]
1 = RDY[1]
2 = RDY[2]
3 = RDY[3]
4 = RDY[4]
5 = RDY[5] or TC-Expiration (depending on GPIF_READYCFG.5)
6 = FIFO Flag (PF, EF, or FF depending on GPIF_EPxFLAGSEL)
7 = 8051 RDY (GPIF_READYCFG.7)

FLOWEQ0CTL E6C8

b7	b6	b5	b4	b3	b2	b1	b0
CTLOE3	**CTLOE2**	**CTLOE1/ CTL5**	**CTLOE0/ CTL4**	**CTL3**	**CTL2**	**CTL1**	**CTL0**
0	0	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

FLOWEQ1CTL E6C9

b7	b6	b5	b4	b3	b2	b1	b0
CTLOE3	**CTLOE2**	**CTLOE1/ CTL5**	**CTLOE0/ CTL4**	**CTL3**	**CTL2**	**CTL1**	**CTL0**
0	0	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

FLOWEQ0CTL defines the state of the CTL5:0 pins when the output of the flow logic equals 0; FLOWEQ1CTL defines the state when the logic output equals 1. During a flow state, the CTL opcode in the waveform descriptor is completely ignored and the behavior of the CTL[5:0] pins are defined by these two registers instead.

CTLOEx Bit: If TRICTL = 1, CTL5:4 are unused and CTLOE3:0 specifies whether the corresponding CTL3:0 output signals are tristated.

1 = Drive CTLx
0 = Tristate CTLx

CTLx Bit: specifies the state to set each CTLx signal to during this entire State.

1 = High level

If the CTLx bit in the GPIFCTLCFG register is set to 1, the output driver will be an open-drain.

If the CTLx bit in the GPIFCTLCFG register is set to 0, the output driver will be driven to CMOS levels.

0 = Low level

defined by FLOWEQxCTL and these bits, instead:

- TRICTL (GPIFCTLCFG.7), as described in Section 10.2.3.1, "Control Output Modes".
- GPIFCTLCFG[5:0].

The combination of these bits defines CTL5:0 during a Flow State as follows:

- If TRICTL is 0, FLOWEQxCTL[5:0] directly represent the output states of CTL5:0 during the Flow State. The GPIFCTLCFG[5:0] bits determine whether the CTL5:0 outputs are CMOS or open-drain: If GPIFCTLCFG.x = 0, CTLx is CMOS; if GPIFCTLCFG.x = 1, CTLx is open-drain.
- If TRICTL is 1, FLOWEQxCTL[7:4] are the output enables for the CTL[3:0] signals, and FLOWEQxCTL[3:0] are the output values for CTL[3:0]. CTL4 and CTL5 are unavailable in this mode.

Table 15-17 illustrates this relationship.

Table 15-18. Control Outputs (CTLx) During the Flow State

TRICTL	Control Output	Output State	Drive Type (0 = CMOS, 1 = Open-Drain)	Output Enable
0	CTL0	FLOWEQxCTL.0	GPIFCTLCFG.0	N/A (CTL Outputs are always enabled when TRICTL = 0)
	CTL1	FLOWEQxCTL.1	GPIFCTLCFG.0	
	CTL2	FLOWEQxCTL.2	GPIFCTLCFG.0	
	CTL3	FLOWEQxCTL.3	GPIFCTLCFG.0	
	CTL4	FLOWEQxCTL.4	GPIFCTLCFG.0	
	CTL5	FLOWEQxCTL.5	GPIFCTLCFG.0	
1	CTL0	FLOWEQxCTL.0	N/A (CTL Outputs are always tristatable CMOS when TRICTL = 1)	FLOWEQxCTL.4
	CTL1	FLOWEQxCTL.1		FLOWEQxCTL.5
	CTL2	FLOWEQxCTL.2		FLOWEQxCTL.6
	CTL3	FLOWEQxCTL.3		FLOWEQxCTL.7
	CTL4	N/A (CTL4 and CTL5 are not available when TRICTL = 1)		
	CTL5			

FLOWSTB E6CB

b7	b6	b5	b4	b3	b2	b1	b0
SLAVE	**RDYASYNC**	**CTLTOGL**	**SUSTAIN**	**0**	**MSTB[2:0]**		
0	0	1	0	0	0	0	0
RW	RW	RW	RW	R	RW	RW	RW

* - based on suggested FLOW_LOGIC settings.

This register defines the Master Strobe that causes data to be read or written during a flow state.

For transactions where GPIF is the slave on the bus, the Master Strobe will be one of the RDY[5:0] pins. This includes external masters that can either write data into GPIF (e.g., UDMA IN) or read data out of GPIF.

For transactions where GPIF is the master on the bus, the Master Strobe will be one of the CTL[5:0] pins. This includes cases where the GPIF writes data out to a slave (e.g., UDMA OUT) or reads data from a slave.

Bit 7 SLAVE

0: GPIF is the master of the bus transaction. This means that one of the CTL[5:0] pins will be the Master Strobe and the particular one is selected by MSTB[2:0].

1: GPIF is the slave of the bus transaction. This means that one of the RDY[5:0] pins will be the Master Strobe and the particular one is selected by MSTB[2:0].

Bit 6 RDYASYNC

If SLAVE is 0 then this bit is ignored, otherwise:

0: Master Strobe (which is a RDY pin in this case) is asynchronous to IFCLK.

1: Master Strobe (which is a RDY pin in this case) is synchronous to IFCLK.

Bit 5 CTLTOGL

If SLAVE is 1 then this bit is ignored. Otherwise, this bit defines which state of the flow logic (see FLOWLOGIC) causes Master Strobe (which will be a CTL pin in this case) to toggle. For example, if this bit is set to 1, then if the output of the flow logic equals 1 then Master Strobe will toggle causing data to flow on the bus. If in the same example the output of the flow logic equals 0 then Master Strobe will freeze causing data flow to halt on the bus.

Bit 4 SUSTAIN

If SLAVE is 1 then this bit is ignored.

Upon exiting a flow state in which SLAVE is 0, Master Strobe (which is a CTL pin in this case) will normally go back to adhering to the CTL opcodes defined in the waveform descriptor.

Bit 2-0 MSTB[2:0]

If SLAVE is 0 then these bits will select which CTL[5:0] pin is the Master Strobe. If SLAVE is 1 then these bits will select which RDY[5:0] pin is the Master Strobe.

FLOWHOLDOFF E6CA

b7	b6	b5	b4	b3	b2	b1	b0
HOPERIOD[3:0]				**HOSTATE**	**HOCTL[2:0]**		
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	1	0	0	1	0

For flow state transactions that meet the following criteria:

1. The interface is asynchronous.
2. GPIF is acting like a slave (FLOWSTB.SLAVE = 1), and thus Master Strobe is a RDY pin.
3. data is being written into the GPIF.

4. the rate at which data is being written in exceeds 96 MB/s for a word-wide data bus or 48 MB/s for a byte-wide data bus.

Bits 7-4 HOPERIOD[3:0]

Defines how many IFCLK cycles to assert not ready (HOCTL) to the external master in order to allow the synchronization interface to catch up.

Bit 3 HOSTATE

Defines what the state of the HOCTL signal should be in to assert not ready.

Bits 2-0 HOCTL[2:0]

Defines which of the six CTL[5:0] pins will be the HOCTL signal which asserts not ready to the external master when the synchronization detects a potential overflow coming. It should coincide with the CTL[5:0] pin that is picked as the “not ready” signal for the (macro-level) endpoint FIFO overflow protection.

FLOWSTBEDGE E6CC

b7	b6	b5	b4	b3	b2	b1	b0
0	**0**	**0**	**0**	**0**	**0**	**FALLING**	**RISING**
R	R	R	R	R	R	R/W	RW
0	0	0	0	0	0	0	1

This register defines whether the Master Strobe (see FLOWSTB) causes data to read or written on either the falling edge, the rising edge, or both (double-edge).

Bit 1 FALLING

0: data is not transferred on the falling edge of Master Strobe

1: data is transferred on the falling edge of Master Strobe

Bit 0 RISING

0: data is not transferred on the rising edge of Master Strobe

1: data is transferred on the rising edge of Master Strobe

To cause data to transfer on both edges of Master Strobe, set both bits to 1

FLOWSTBHPERIOD E6CD

b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	1	0

If the flow state is such that the GPIF is the master on the bus (FLOWSTB.SLAVE = 0) then Master Strobe will be one of the CTL[5:0] pins (see FLOWSTB). While in the flow state, if the flow logic (see FLOWLOGIC) evaluates in such a way that Master Strobe should toggle (see FLOWSTB.CTLTOGL), then this register defines the frequency at which it will toggle.

More precisely, this register defines the half period of the Master Strobe toggling frequency. Further, to give the user a high degree of resolution this Master Strobe half period is defined in terms of half IFCLK periods. Therefore, if IFCLK is running at 48 MHz, this gives a resolution of 10.8 nS.

Bits 7-0 D7:0 *Master Strobe Half-Period*

Number of *half* IFCLK periods that define the half period of Master Strobe (if it is a CTL pin). Value must be at least 2, meaning that the minimum half period for Master Strobe is one full IFCLK cycle.

GPIFHOLDTIME E60C

b7	b6	b5	b4	b3	b2	b1	b0
0	**0**	**0**	**0**	**0**	**0**	**HOLDTIME[1:0]**	
R	R	R	R	R	R	RW	RW
0	0	0	0	0	0	0	0

For any transaction where the GPIF writes data onto FD[15:0], this register determines how long the data is held. Valid choices are 0, ½ or 1 IFCLK cycle. This register applies to *any* data written by the GPIF to FD[15:0], whether through a flow state or not.

For non-flow states, the hold amount is really just a delay of the normal (non-held) presentation of FD[15:0] by the amount specified in HOLDTIME[1:0].

For flow states in which the GPIF is the master on the bus (FLOWSTB.SLAVE = 0), the hold amount is with respect to the activating edge (see FLOW_MASTERSTB_EDGE) of Master Strobe (which will be a CTL pin in this case).

For flow states in which the GPIF is the slave on the bus (FLOWSTB.SLAVE = 1), the hold amount is really just a delay of the normal (non-held) presentation of FD[15:0] by the amount specified in HOLDTIME[1:0] in reaction to the activating edge of Master Strobe (which will be a RDY pin in this case). Note the hold amount is NOT *directly* with respect to the activating edge of Master Strobe in

this case. It is with respect to when the data would normally come out in response to Master Strobe including any latency to synchronize Master Strobe.

In all cases, the data will be held for the desired amount even if the ensuing GPIF state calls for the data bus to be tristated. In other words the FD[15:0] output enable will be held by the same amount as the data itself.

Bits 1-0 **HOLDTIME[1:0]** *GPIF Hold Time*

00 = 0 IFCLK cycles

01 = ½ IFCLK cycle

10 = 1 IFCLK cycle

11 = Reserved

15.12.7 GPIF Transaction Count Bytes

GPIFTCB3 **GPIF Transaction Count Byte3** **E6CE**

see Section 15.14

b7	b6	b5	b4	b3	b2	b1	b0
TC31	**TC30**	**TC29**	**TC28**	**TC27**	**TC26**	**TC25**	**TC24**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Figure 15-99. GPIF Transaction Count Byte3

Bit 7-0 **TC31:24** *GPIF Transaction Count*

Refer to Bit 0 of this register.

GPIFTCB2 **GPIF Transaction Count Byte2** **E6CF**

see Section 15.14

b7	b6	b5	b4	b3	b2	b1	b0
TC23	**TC22**	**TC21**	**TC20**	**TC19**	**TC18**	**TC17**	**TC16**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Figure 15-100. GPIF Transaction Count Byte2

Bit 7-0 **TC16:23** *GPIF Transaction Count*

Refer to Bit 0 of this register.

GPIFTCB1 GPIF Transaction Count Byte1 E6D0

see Section 15.14

b7	b6	b5	b4	b3	b2	b1	b0
TC15	**TC14**	**TC13**	**TC12**	**TC11**	**TC10**	**TC9**	**TC8**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Figure 15-101. GPIF Transaction Count Byte1

Bit 7-0 **TC8:15** *GPIF Transaction Count*

Refer to Bit 0 of this register.

GPIFTCB0 GPIF Transaction Count Byte0 E6D1

see Section 15.14

b7	b6	b5	b4	b3	b2	b1	b0
TC7	**TC6**	**TC5**	**TC4**	**TC3**	**TC2**	**TC1**	**TC0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	1

Figure 15-102. GPIF Transaction Count Byte0

Bit 7-0 **TC7:0** *GPIF Transaction Count*

Registers GPIFTCB3, GPIFTCB2, GPIFTCB1, and GPIFTCB0 represent the live update of GPIF transactions.

15.12.8 Endpoint 2, 4, 6, 8 GPIF Flag Select

EP2GPIFFLGSEL ***see Section 15.14***	**Endpoint 2 GPIF Flag Select**	**E6D2**
EP4GPIFFLGSEL ***see Section 15.14***	**Endpoint 4 GPIF Flag Select**	**E6DA**
EP6GPIFFLGSEL ***see Section 15.14***	**Endpoint 6 GPIF Flag Select**	**E6E2**
EP8GPIFFLGSEL ***see Section 15.14***	**Endpoint 8 GPIF Flag Select**	**E6EA**

b7	b6	b5	b4	b3	b2	b1	b0
0	**0**	**0**	**0**	**0**	**0**	**FS1**	**FS0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Figure 15-103. Endpoint 2, 4, 6, 8 GPIF Flag Select

Bit 1-0 **FS1:0** *GPIF Flag Select*

Table 15-19. Endpoint 2, 4, 6, 8 GPIF Flag Select Values

FS1	FS0	Flag
0	0	Programmable
0	1	Empty
1	0	Full
1	1	Reserved

Only one FIFO flag at a time may be made available to the GPIF as a control input. The FS1:FS0 bits select which flag is made available.

15.12.9 Endpoint 2, 4, 6, and 8 GPIF Stop Transaction

EP2GPIFPFSTOP	**Endpoint 2 GPIF Stop Transaction**	**E6D3**
EP4GPIFPFSTOP	**Endpoint 4 GPIF Stop Transaction**	**E6DB**
EP6GPIFPFSTOP	**Endpoint 6 GPIF Stop Transaction**	**E6E3**
EP8GPIFPFSTOP	**Endpoint 8 GPIF Stop Transaction**	**E6EB**

b7	b6	b5	b4	b3	b2	b1	b0
0	**0**	**0**	**0**	**0**	**0**	**0**	**FIFO[2,4,6,8] FLAG**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Figure 15-104. Endpoint 2, 4, 6, and 8 GPIF Stop Transaction

Bit 0 **EP[2,4,6,8]PF** *Stop on Endpoint Programmable Flag*

1= GPIF transitions to “DONE” state when the flag selected by EPxGPIFFLGSEL is asserted.
0= When transaction count has been met.

15.12.10 Endpoint 2, 4, 6, and 8 Slave FIFO GPIF Trigger

EP2GPIFTRIG *see Section 15.14*	**Endpoint 2 Slave FIFO GPIF Trigger**	**E6D4**
EP4GPIFTRIG *see Section 15.14*	**Endpoint 4 Slave FIFO GPIF Trigger**	**E6DC**
EP6GPIFTRIG *see Section 15.14*	**Endpoint 6 Slave FIFO GPIF Trigger**	**E6E4**
EP8GPIFTRIG *see Section 15.14*	**Endpoint 8 Slave FIFO GPIF Trigger**	**E6EC**

b7	b6	b5	b4	b3	b2	b1	b0
x	**x**	**x**	**x**	**x**	**x**	**x**	**x**
W	W	W	W	W	W	W	W
x	x	x	x	x	x	x	x

Figure 15-105. Endpoint 2, 4, 6, and 8 Slave FIFO GPIF Trigger

Write 0xFF to this register to initiate a GPIF write. Read from this register to initiate a GPIF read.

15.12.11 GPIF Data High (16-Bit Mode)

XGPIFSGLDATH GPIF Data HIGH (16-bit mode) E6F0

b7	b6	b5	b4	b3	b2	b1	b0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

Figure 15-106. GPIF Data High (16-Bit Mode)

Bit 7-0 D15:8 *GPIF Data High*

Contains the data written to or read from the FD15:8 (PORTD) pins using the GPIF waveform.

15.12.12 Read/Write GPIF Data LOW & Trigger Transaction

XGPIFSGLDATLX Read/Write GPIF Data LOW & Trigger Transaction E6F1

b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

Figure 15-107. Read/Write GPIF Data LOW & Trigger Transaction

Bit 7-0 D7:0 *GPIF Data Low /Trigger GPIF Transaction*

Contains the data written to or read from the FD7:0 (PORTB) pins. Reading or writing low-byte triggers a GPIF transaction.

15.12.13 Read GPIF Data LOW, No Transaction Trigger

XGPIFSGLDATLNOX — Read GPIF Data LOW, No Transaction Trigger — E6F2

b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R	R	R	R	R	R	R	R
x	x	x	x	x	x	x	x

Figure 15-108. Read GPIF Data LOW, No Transaction Trigger

Bit 7-0 **D7:0** *GPIF Data Low /Don't Trigger GPIF Transaction*

Contains the data written to or read from the FD7:0 (PORTB) pins. Read or write low byte does not trigger GPIF transaction.

15.12.14 GPIF RDY Pin Configuration

GPIFREADYCFG — GPIF RDY Pin Configuration — E6F3

b7	b6	b5	b4	b3	b2	b1	b0
INTRDY	**SAS**	**TCXRDY5**	**0**	**0**	**0**	**0**	**0**
R/W	R/W	R/W	R	R	R	R	R
0	0	0	0	0	0	0	0

Figure 15-109. GPIF Ready Pins

Bit 7 **INTRDY** *Force Ready Condition*

Internal RDY. Functions as a sixth RDY input, controlled by the firmware instead of a RDY pin.

Bit 6 **SAS** *RDY Signal Connection to GPIF Input Logic*

Synchronous/Asynchronous RDY signals. This bit controls how the RDY signals connect to the GPIF input logic.

If the internal IFCLK is used to clock the GPIF, the RDY signals can make transitions in an asynchronous manner, i.e. not referenced to the internal clock. Setting SAS=1 causes the RDY inputs to pass through two flip-flops for synchronization purposes.

If the RDY signals are synchronized to IFCLK, and obey the setup and hold times with respect to this clock, the user can set SAS=0, which causes the RDY signals to pass through a single flip-flop.

Bit 5 **TCXRDY5** *TC Expiration Replaces RDY5*

To use the transaction count expiration signal as a ready input to a waveform, set this bit to 1. Setting this bit will take the place of the pin RDY5 in the decision point of the waveform. The default value of the bit is zero (in other words, the RDY5 from the pin prevails).

15.12.15 GPIF RDY Pin Status

GPIFREADYSTAT **GPIF RDY Pin Status** **E6F4**

b7	b6	b5	b4	b3	b2	b1	b0
0	**0**	**RDY5**	**RDY4**	**RDY3**	**RDY2**	**RDY1**	**RDY0**
R	R	R	R	R	R	R	R
0	0	x	x	x	x	x	x

Figure 15-110. GPIF Ready Status Pins

Bit 5-0 **RDY5:0** *Current State of Ready Pins*

RDYx. Instantaneous states of the RDY pins. The current state of the RDY[5:0] pins, sampled at each rising edge of the GPIF clock.

15.12.16 Abort GPIF Cycles

GPIFABORT **Abort GPIF** **E6F5**

b7	b6	b5	b4	b3	b2	b1	b0
x	**x**	**x**	**x**	**x**	**x**	**x**	**x**
W	W	W	W	W	W	W	W
x	x	x	x	x	x	x	x

Figure 15-111. Abort GPIF

Write 0xFF to immediately abort a GPIF transaction and transition to the Idle State.

15.13 Endpoint Buffers

15.13.1 EP0 IN-OUT Buffer

EP0BUF **EP0 IN/OUT Buffer** **E740-E77F**

b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
X	X	X	X	X	X	X	X

Figure 15-112. EP0 IN/OUT Buffer

Bit 7-0 **D7:0** *EP0 Data*

EP0 Data buffer (IN/OUT). 64 bytes.

15.13.2 Endpoint 1-OUT Buffer

EP1OUTBUF **EP1-OUT Buffer** **E780-E7BF**

b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
X	X	X	X	X	X	X	X

Figure 15-113. EP1-OUT Buffer

Bit 7-0 **D7:0** *EP1-Out Data*

EP1-Out Data buffer. 64 bytes.

15.13.3 Endpoint 1-IN Buffer

EP1INBUF **EP1-IN Buffer** **E7C0-E7FF**

b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
X	X	X	X	X	X	X	X

Figure 15-114. EP1-IN Buffer

Bit 7-0 **D7:0** *EP1-IN Buffer*

EP1-IN Data buffer. 64 bytes.

15.13.4 Endpoint 2/Slave FIFO Buffer

EP2FIFOBUF **512/1024-byte EP2/Slave FIFO Buffer** **F000-F3FF**

b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
X	X	X	X	X	X	X	X

Figure 15-115. 512/1024-byte EP2/Slave FIFO Buffer

Bit 7-0 **D7:0** *EP2 Data*

512/1024-byte EP2 buffer.

15.13.5 512-byte Endpoint 4/Slave FIFO Buffer

EP4FIFOBUF 512-byte EP4/Slave FIFO Buffer F400-F5FF

b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
X	X	X	X	X	X	X	X

Figure 15-116. 512-byte EP4/Slave FIFO Buffer

Bit 7-0 D7:0 *EP4 Data*

512-byte EP4 buffer.

15.13.6 512/1024-byte Endpoint 6/Slave FIFO Buffer

EP6FIFOBUF 512/1024-byte EP6/Slave FIFO Buffer F800-FBFF

b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
X	X	X	X	X	X	X	X

Figure 15-117. 512/1024-byte EP6/Slave FIFO Buffer

Bit 7-0 D7:0 *EP6 Data*

512/1024-byte EP6 buffer.

15.13.7 512-byte Endpoint 8/Slave FIFO Buffer

EP8FIFOBUF **512-byte EP8/Slave FIFO Buffer** **FC00-FDFF**

b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
X	X	X	X	X	X	X	X

Figure 15-118. 512-byte EP8/Slave FIFO Buffer

Bit 7-0 **D7:0** *EP8 Data*

512-byte EP8 buffer.

15.14 Synchronization Delay

Under certain conditions, some read and write accesses to FX2 registers must be separated by a *synchronization delay*. The delay is necessary only under the following conditions:

- Between a write to any register in the 0xE600-0xE6FF range and a write to one of the registers in Table 15-20.
- Between a write to one of the registers in Tabl e15-20 and a read from any register in the 0xE600-0xE6FF range.

Table 15-20. Registers Which Require a Synchronization Delay

FIFORESET	FIFOPINPOLAR
INPKTEND	EPxBCH:L
EPxFIFOPFH:L	EPxAUTOINLENH:L
EPxFIFOCFG	EPxGPIFFLGSEL
PINFLAGSAB	PINFLAGSCD
EPxFIFOIE	EPxFIFOIRQ
GPIFIE	GPIFIRQ
UDMACRCH:L	GPIFADRH:L
GPIFTRIG	EPxGPIFTRIG
OUTPKTEND	REVCTL
GPIFTCB3	GPIFTCB2
GPIFTCB1	GPIFTCB0

The minimum delay length is a function of the IFCLK and CLKOUT (CPU Clock) frequencies, and is determined by the equation:

$$\text{Minimum Sync Delay, in CPU cycles} = \left\lceil 1.5 \times \left(\frac{\text{IFCLK Period}}{\text{CLKOUT Period}} + 1 \right) \right\rceil$$

Note:
$\lceil n \rceil$ means *"round n upward"*

The required delay length is smallest when the CPU is running at its slowest speed (12 MHz, 83.2 ns/cycle) and IFCLK is running at its fastest speed (48 MHz, 20.8 ns/cycle). Under those conditions, the minimum required delay is:

$$\left\lceil 1.5 \times \left(\frac{20.8}{83.2} + 1 \right) \right\rceil = \lceil 1.5 \times (1.25) \rceil = \lceil 1.875 \rceil = 2 \text{ CPU Cycles}$$

The longest delay is required when the CPU is running at its fastest speed (48MHz, 20.8 ns/cycle) and IFCLK is running much slower (e.g., 5.2 MHz, 192 ns/cycle):

$$\left\lceil 1.5 \times \left(\frac{192}{20.8} + 1 \right) \right\rceil = \lceil 1.5 \times (10.23) \rceil = \lceil 15.3 \rceil = 16 \text{ CPU Cycles}$$

The most-typical FX2 configuration, IFCLK and CLKOUT both running at 48 MHz, requires a minimum delay of:

$$\left\lceil 1.5 \times \left(\frac{20.8}{20.8} + 1 \right) \right\rceil = \lceil 1.5 \times (2) \rceil = \lceil 3 \rceil = 3 \text{ CPU Cycles}$$

The *Frameworks* fimware supplied with the EZ-USB FX2 Development Kit includes a macro, called SYNCDELAY, which implements the synchronization delay. The macro is in the file *fx2sdly.h*.

Appendix A
Default Descriptors for Full Speed Mode

Tables A-1 through A-25 show the descriptor data built into the FX2 logic. The tables are presented in the order that the bytes are stored.

Table A-1 Default USB Device Descriptor

Offset	Field	Description	Value
0	bLength	Length of this Descriptor = 18 bytes	12H
1	bDescriptorType	Descriptor Type = **Device**	01H
2	bcdUSB (L)	USB Specification Version 2.00 (L)	00H
3	bcdUSB (H)	USB Specification Version 2.00 (H)	02H
4	bDeviceClass	Device Class (FF is Vendor-Specific)	FFH
5	bDeviceSubClass	Device Sub-class (FF is Vendor-Specific)	FFH
6	bDeviceProtocol	Device Protocol (FF is Vendor-Specific)	FFH
7	bMaxPacketSize0	Maximum Packet Size for EP0 = **64 bytes**	40H
8	idVendor (L)	Vendor ID (L) Cypress Semi = 04B4H	B4H
9	idVendor (H)	Vendor ID (H)	04H
10	idProduct (L)	Product ID (L) EZ-USB = 8613H	13H
11	idProduct (H)	Product ID (H)	86H
12	bcdDevice (L)	Device Release Number (BCD,L) (see individual data sheet)	xxH
13	bcdDevice (H)	Device Release Number (BCD,H) (see individual data sheet)	xxH
14	iManufacturer	Manufacturer Index String = None	00H
15	iProduct	Product Index String = None	00H
16	iSerialNumber	Serial number Index String = None	00H
17	bNumConfigurations	Number of Configurations in this Interface = 1	01H

The Device Descriptor specifies a MaxPacketSize of 64 bytes for endpoint 0, contains Cypress Semiconductor Vendor, Product and Release Number IDs, and uses no string indices. Release Number IDs (*XX* and *YY*) are found in individual Cypress Semiconductor data sheets. The FX2 logic returns this information response to a “Get_Descriptor/Device” host request.

Table A-2 Device Qualifier

Offset	Field	Description	Value
0	bLength	Length of this Descriptor = 10 bytes	0AH
1	bDescriptorType	Descriptor Type = **Device Qualifier**	06H
2	bcdUSB (L)	USB Specification Version 2.00 (L)	00H
3	bcdUSB (H)	USB Specification Version 2.00 (H)	02H
4	bDeviceClass	Device Class (FF is Vendor-Specific)	FFH
5	bDeviceSubClass	Device Sub-class (FF is Vendor-Specific)	FFH
6	bDeviceProtocol	Device Protocol (FF is Vendor-Specific)	FFH
7	bMaxPacketSize0	Maximum Packet Size for other speed = **64 bytes**	40H
8	bNumConfigurations	Number of other Configurations = 1	01H
9	bReserved	Must be set to zero	00H

Table A-3 USB Default Configuration Descriptor

Offset	Field	Description	Value
0	bLength	Length of this Descriptor = 9 bytes	09H
1	bDescriptorType	Descriptor Type = **Configuration**	02H
2	wTotalLength (L)	Total Length (L) Including Interface and Endpoint Descriptors (171 total)	ABH
3	wTotalLength (H)	Total Length (H)	00H
4	bNumInterfaces	Number of Interfaces in this Configuration	01H
5	bConfigurationValue	Configuration Value Used by Set_Configuration Request to Select this interface	01H
6	iConfiguration	Index of String Describing this Configuration = None	00H
7	bmAttributes	Attributes - Bus-Powered, No Wakeup	80H
8	MaxPower	Maximum Power - 100 mA	32H

The configuration descriptor includes a total length field (offset 2-3) that encompasses all interface and endpoint descriptors that follow the configuration descriptor. This configuration describes a single interface (offset 4). The host selects this configuration by issuing a Set_Configuration requests specifying configuration #1 (offset 5).

Table A-4 USB Default Interface 0, Alternate Setting 0

Offset	Field	Description	Value
0	bLength	Length of the Interface Descriptor	09H
1	bDescriptorType	Descriptor Type = **Interface**	04H
2	bInterfaceNumber	Zero based index of this interface = **0**	00H
3	bAlternateSetting	Alternate Setting Value = **0**	00H
4	bNumEndpoints	Number of endpoints in this interface (not counting EP0) = **0**	00H
5	bInterfaceClass	Interface Class = Vendor Specific	FFH
6	bInterfaceSubClass	Interface Sub-class = Vendor Specific	FFH
7	bInterfaceProtocol	Interface Protocol = Vendor Specific	FFH
8	iInterface	Index to string descriptor for this interface = None	00H

Table A-5 USB Default Interface 0, Alternate Setting 1

Offset	Field	Description	Value
0	bLength	Length of this Interface Descriptor	09H
1	bDescriptorType	Descriptor Type = **Interface**	04H
2	bInterfaceNumber	Zero based index of this interface = **0**	00H
3	bAlternateSetting	Alternate Setting Value = **1**	01H
4	bNumEndpoints	Number of endpoints in this interface (not counting EP0) = 6	06H
5	bInterfaceClass	Interface Class = Vendor Specific	FFH
6	bInterfaceSubClass	Interface Sub-class = Vendor Specific	FFH
7	bInterfaceProtocol	Interface Protocol = Vendor Specific	FFH
8	iInterface	Index to string descriptor for this interface = None	00H

Table A-6 Endpoint Descriptor (EP1 out)

Offset	Field	Description	Value
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint direction (1 is in) and address = **OUT1**	01H
3	bmAttributes	XFR Type = **BULK**	02H
4	wMaxPacketSize (L)	Maximum Packet Size = **64 bytes**	40H
5	WMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds (**1 for iso**)	00H

Table A-7 Endpoint Descriptor (EP1 in)

Offset	Field	Description	Value
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and address = **IN1**	81H
3	bmAttributes	XFR Type = **BULK**	02H
4	wMaxPacketSize (L)	Maximum Packet Size = 64 bytes	40H
5	WMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	00H

Table A-8 Endpoint Descriptor (EP2)

Offset	Field	Description	Value
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and address = **OUT2**	02H
3	bmAttributes	XFR Type = BULK	02H
4	wMaxPacketSize (L)	Maximum Packet Size = 64 bytes	40H
5	WMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	00H

Table A-9 Endpoint Descriptor (EP4)

Offset	Field	Description	Value
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and address = **OUT4**	04H
3	bmAttributes	XFR Type = BULK	02H
4	wMaxPacketSize (L)	Maximum Packet Size = 64 bytes	40H
5	WMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	00H

Table A-10 Endpoint Descriptor (EP6)

Offset	Field	Description	Value
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and address = IN6	86H
3	bmAttributes	XFR Type = BULK	02H
4	wMaxPacketSize (L)	Maximum Packet Size = 64 bytes	40H
5	WMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	00H

Table A-11 Endpoint Descriptor (EP8)

Offset	Field	Description	Value
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and address = IN8	88H
3	bmAttributes	XFR Type = BULK	02H
4	wMaxPacketSize (L)	Maximum Packet Size = 64 bytes	40H
5	WMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	00H

Table A-12 Interface Descriptor (Alt. Setting 2)

Offset	Field	Description	Value
0	bLength	Length of the Interface Descriptor	09H
1	bDescriptorType	Descriptor Type = **Interface**	04H
2	bInterfaceNumber	Zero based index of this interface = 0	00H
3	bAlternateSetting	Alternate Setting Value = 2	02H
4	bNumEndpoints	Number of endpoints in this interface (not counting EP0) = 6	06H
5	bInterfaceClass	Interface Class = Vendor Specific	FFH
6	bInterfaceSubClass	Interface Sub-class = Vendor Specific	FFH
7	bInterfaceProtocol	Interface Protocol = Vendor Specific	FFH
8	iInterface	Index to string descriptor for this interface = None	00H

Table A-13 Endpoint Descriptor (EP1 out)

Offset	Field	Description	Value
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and address = OUT1	01H
3	bmAttributes	XFR Type = INT	03H
4	wMaxPacketSize (L)	Maximum Packet Size = 64 bytes	40H
5	WMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	0AH

Table A-14 Endpoint Descriptor (EP1 in)

Offset	Field	Description	Value
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and address = IN1	81H
3	bmAttributes	XFR Type = INT	03H
4	wMaxPacketSize (L)	Maximum Packet Size = 64 bytes	40H
5	WMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	0AH

Table A-15 Endpoint Descriptor (EP2

Offset	Field	Description	Value
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and address = OUT2	02H
3	bmAttributes	XFR Type = INT	03H
4	wMaxPacketSize (L)	Maximum Packet Size = 64 bytes	40H
5	WMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	0AH

Table A-16 Endpoint Descriptor (EP4)

Offset	Field	Description	Value
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and address = OUT4	04H
3	bmAttributes	XFR Type = BULK	02H
4	wMaxPacketSize (L)	Maximum Packet Size = 64 bytes	40H
5	WMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	00H

Table A-17 Endpoint Descriptor (EP6)

Offset	Field	Description	Value
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and address = IN6	86H
3	bmAttributes	XFR Type = INT	03H
4	wMaxPacketSize (L)	Maximum Packet Size = 64 bytes	40H
5	WMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	0AH

Table A-18 Endpoint Descriptor (EP8)

Offset	Field	Description	Value
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and address = IN8	88H
3	bmAttributes	XFR Type = BULK	02H
4	wMaxPacketSize (L)	Maximum Packet Size = 64 bytes	40H
5	WMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	00H

Table A-19 Interface Descriptor (Alt. Setting 3)

Offset	Field	Description	Value
0	bLength	Length of the Interface Descriptor	09H
1	bDescriptorType	Descriptor Type = **Interface**	04H
2	bInterfaceNumber	Zero based index of this interface = 0	00H
3	bAlternateSetting	Alternate Setting Value = 3	03H
4	bNumEndpoints	Number of endpoints in this interface (not counting EP0) = 6	06H
5	bInterfaceClass	Interface Class = Vendor Specific	FFH
6	bInterfaceSubClass	Interface Sub-class = Vendor Specific	FFH
7	bInterfaceProtocol	Interface Protocol = Vendor Specific	FFH
8	iInterface	Index to string descriptor for this interface = None	00H

Table A-20 Endpoint Descriptor (EP1 out)

Offset	Field	Description	Value
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and address = OUT1	01H
3	bmAttributes	XFR Type = INT	03H
4	wMaxPacketSize (L)	Maximum Packet Size = 64 bytes	40H
5	WMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	0AH

Table A-21 Endpoint Descriptor (EP1 in)

Offset	Field	Description	Value
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and address = IN1	81H
3	bmAttributes	XFR Type = INT	03H
4	wMaxPacketSize (L)	Maximum Packet Size = 64 bytes	40H
5	WMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	0AH

Table A-22 Endpoint Descriptor (EP2)

Offset	Field	Description	Value
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and address = OUT2	02H
3	bmAttributes	XFR Type = ISO, No Synchronization, Data endpoint	01H
4	wMaxPacketSize (L)	Maximum Packet Size = 64 bytes	40H
5	WMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	01H

Table A-23 Endpoint Descriptor (EP4)

Offset	Field	Description	Value
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and address = OUT4	04H
3	bmAttributes	XFR Type = BULK	02H
4	wMaxPacketSize (L)	Maximum Packet Size = 64 bytes	40H
5	WMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	00H

Table A-24 Endpoint Descriptor (EP6)

Offset	Field	Description	Value
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and address = IN6	86H
3	bmAttributes	XFR Type = ISO, No Synchronization, Data Endpoint	01H
4	wMaxPacketSize (L)	Maximum Packet Size = 64 bytes	40H
5	WMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	01H

Table A-25 Endpoint Descriptor (EP8)

Offset	Field	Description	Value
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and address = IN8	88H
3	bmAttributes	XFR Type = BULK	02H
4	wMaxPacketSize (L)	Maximum Packet Size = 64 bytes	40H
5	WMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	00H

Appendix B
Default Descriptors for High Speed Mode

Tables B-1 through B-25 show the descriptor data built into the FX2 logic. The tables are presented in the order that the bytes are stored.

Table B-1 Device Descriptor

Offset	Field	Description	Value
0	bLength	Length of this Descriptor = 18 bytes	12H
1	bDescriptorType	Descriptor Type = **Device**	01H
2	bcdUSB (L)	USB Specification Version 2.00 (L)	00H
3	bcdUSB (H)	USB Specification Version 2.00 (H)	02H
4	bDeviceClass	Device Class (FF is Vendor-Specific)	FFH
5	bDeviceSubClass	Device Sub-class (FF is Vendor-Specific)	FFH
6	bDeviceProtocol	Device Protocol (FF is Vendor-Specific)	FFH
7	bMaxPacketSize0	Maximum Packet Size for EP0 = **64 bytes**	40H
8	idVendor (L)	Vendor ID (L) Cypress Semi = 04B4H	B4H
9	idVendor (H)	Vendor ID (H)	04H
10	idProduct (L)	Product ID (L) EZ-USB = 8613H	13H
11	idProduct (H)	Product ID (H)	86H
12	bcdDevice (L)	Device Release Number (BCD,L) (see individual data sheet)	xxH
13	bcdDevice (H)	Device Release Number (BCD,H) (see individual data sheet)	xxH
14	iManufacturer	Manufacturer Index String = None	00H
15	iProduct	Product Index String = None	00H
16	iSerialNumber	Serial Number Index String = None	00H
17	bNumConfigurations	Number of Configurations in this Interface = 1	01H

The Device Descriptor specifies a MaxPacketSize of 64 bytes for endpoint 0, contains Cypress Semiconductor Vendor, Product and Release Number IDs, and uses no string indices. Release Number IDs (*XX* and *YY*) are found in individual Cypress Semiconductor data sheets. The FX2 logic returns this information response to a “Get_Descriptor/Device” host request.

Table B-2 Device Qualifier

Offset	Field	Description	Value
0	bLength	Length of this Descriptor = 10 bytes	0AH
1	bDescriptorType	Descriptor Type = **Device Qualifier**	06H
2	bcdUSB (L)	USB Specification Version 2.00 (L)	00H
3	bcdUSB (H)	USB Specification Version 2.00 (H)	02H
4	bDeviceClass	Device Class (FF is vendor-specific)	FFH
5	bDeviceSubClass	Device Sub-class (FF is vendor-specific)	FFH
6	bDeviceProtocol	Device Protocol (FF is vendor-specific)	FFH
7	bMaxPacketSize0	Maximum Packet Size for other speed = 64 bytes	40H
8	bNumConfigurations	Number of other Configurations = 1	01H
9	bReserved	Must be set to Zero	00H

Table B-3 Configuration Descriptor

Offset	Field	Description	Value
0	bLength	Length of this Descriptor = 9 bytes	09H
1	bDescriptorType	Descriptor Type = **Configuration**	02H
2	wTotalLength (L)	Total length (L) including Interface and Endpoint descriptors (171 total)	ABH
3	wTotalLength (H)	Total Length (H)	00H
4	bNumInterfaces	Number of Interfaces in this Configuration	01H
5	bConfigurationValue	Configuration value used by Set_Configuration Request to select this interface	01H
6	iConfiguration	Index of String Describing this Configuration = None	00H
7	bmAttributes	Attributes - Bus Powered, No Wakeup	80H
8	MaxPower	Maximum Power - 100 ma	32H

Table B-4 Interface Descriptor (Alt. Setting 0)

Offset	Field	Description	Value
0	bLength	Length of the Interface Descriptor	09H
1	bDescriptorType	Descriptor Type = **Interface**	04H
2	bInterfaceNumber	Zero based index of this interface = 0	00H
3	bAlternateSetting	Alternate Setting Value = 0	00H
4	bNumEndpoints	Number of endpoints in this interface (not counting EP0) = 0	00H
5	bInterfaceClass	Interface Class = Vendor Specific	FFH
6	bInterfaceSubClass	Interface Sub-class = Vendor Specific	FFH
7	bInterfaceProtocol	Interface Protocol = Vendor Specific	FFH
8	iInterface	Index to string descriptor for this interface = None	00H

Table B-5 Interface Descriptor (Alt. Setting 1)

Offset	Field	Description	Value
0	bLength	Length of the Interface Descriptor	09H
1	bDescriptorType	Descriptor Type = **Interface**	04H
2	bInterfaceNumber	Zero based index of this interface = 0	00H
3	bAlternateSetting	Alternate Setting Value = 1	01H
4	bNumEndpoints	Number of endpoints in this interface (not counting EP0) = 6	06H
5	bInterfaceClass	Interface Class = Vendor Specific	FFH
6	bInterfaceSubClass	Interface Sub-class = Vendor Specific	FFH
7	bInterfaceProtocol	Interface Protocol = Vendor Specific	FFH
8	iInterface	Index to string descriptor for this interface = None	00H

Table B-6 Endpoint Descriptor (EP1 out)

Offset	Field	Description	Value
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and address = OUT1	01H
3	bmAttributes	XFR Type = BULK	02H
4	wMaxPacketSize (L)	Maximum Packet Size = 512 bytes	00H
5	WMaxPacketSize (H)	Maximum Packet Size - High	02H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	00H

Table B-7 Endpoint Descriptor (EP1 in)

Offset	Field	Description	Value
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and address = IN1	81H
3	bmAttributes	XFR Type = BULK	02H
4	wMaxPacketSize (L)	Maximum Packet Size = 512 bytes	00H
5	WMaxPacketSize (H)	Maximum Packet Size - High	02H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	00H

Table B-8 Endpoint Descriptor (EP2)

Offset	Field	Description	Value
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and address = OUT2	02H
3	bmAttributes	XFR Type = BULK	02H
4	wMaxPacketSize (L)	Maximum Packet Size = 512 bytes	00H
5	WMaxPacketSize (H)	Maximum Packet Size - High	02H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	00H

Table B-9 Endpoint Descriptor (EP4)

Offset	Field	Description	Value
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and address = OUT4	04H
3	bmAttributes	XFR Type = BULK	02H
4	wMaxPacketSize (L)	Maximum Packet Size = 512 bytes	00H
5	WMaxPacketSize (H)	Maximum Packet Size - High	02H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	00H

Table B-10 Endpoint Descriptor (EP6)

Offset	Field	Description	Value
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and address = IN6	86H
3	bmAttributes	XFR Type = BULK	02H
4	wMaxPacketSize (L)	Maximum Packet Size = 512 bytes	00H
5	WMaxPacketSize (H)	Maximum Packet Size - High	02H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	00H

Table B-11 Endpoint Descriptor (EP8)

Offset	Field	Description	Value
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and address = IN8	88H
3	bmAttributes	XFR Type = BULK	02H
4	wMaxPacketSize (L)	Maximum Packet Size = 512 bytes	00H
5	WMaxPacketSize (H)	Maximum Packet Size - High	02H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	00H

Table B-12 Interface Descriptor (Alt. Setting 2)

Offset	Field	Description	Value
0	bLength	Length of the Interface Descriptor	09H
1	bDescriptorType	Descriptor Type = **Interface**	04H
2	bInterfaceNumber	Zero based index of this interface = 0	00H
3	bAlternateSetting	Alternate Setting Value = 2	02H
4	bNumEndpoints	Number of endpoints in this interface (not counting EP0) = 6	06H
5	bInterfaceClass	Interface Class = Vendor Specific	FFH
6	bInterfaceSubClass	Interface Sub-class = Vendor Specific	FFH
7	bInterfaceProtocol	Interface Protocol = Vendor Specific	FFH
8	iInterface	Index to string descriptor for this interface = None	00H

Table B-13 Endpoint Descriptor (EP1 out)

Offset	Field	Description	Value
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and address = OUT1	01H
3	bmAttributes	XFR Type = INT	03H
4	wMaxPacketSize (L)	Maximum Packet Size = 64 bytes	40H
5	WMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	01H

Table B-14 Endpoint Descriptor (EP1 in)

Offset	Field	Description	Value
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and address = IN1	81H
3	bmAttributes	XFR Type = INT	03H
4	wMaxPacketSize (L)	Maximum Packet Size = 64 bytes	40H
5	WMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	01H

Table B-15 Endpoint Descriptor (EP2)

Offset	Field	Description	Value
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and address = OUT2	02H
3	bmAttributes	XFR Type = INT	03H
4	wMaxPacketSize (L)	Maximum Packet Size = 512 bytes	00H
5	WMaxPacketSize (H)	Maximum Packet Size - High	02H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	01H

Table B-16 Endpoint Descriptor (EP4)

Offset	Field	Description	Value
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and address = OUT4	04H
3	bmAttributes	XFR Type = BULK	02H
4	wMaxPacketSize (L)	Maximum Packet Size = 512 bytes	00H
5	WMaxPacketSize (H)	Maximum Packet Size - High	02H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	00H

Table B-17 Endpoint Descriptor (EP6)

Offset	Field	Description	Value
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and address = IN6	86H
3	bmAttributes	XFR Type = INT	03H
4	wMaxPacketSize (L)	Maximum Packet Size = 512 bytes	00H
5	WMaxPacketSize (H)	Maximum Packet Size - High	02H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	01H

Table B-18 Endpoint Descriptor (EP8)

Offset	Field	Description	Value
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and address = IN8	88H
3	bmAttributes	XFR Type = BULK	02H
4	wMaxPacketSize (L)	Maximum Packet Size = 512 bytes	00H
5	WMaxPacketSize (H)	Maximum Packet Size - High	02H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	00H

Table B-19 Interface Descriptor (Alt. Setting 3)

Offset	Field	Description	Value
0	bLength	Length of the Interface Descriptor	09H
1	bDescriptorType	Descriptor Type = **Interface**	04H
2	bInterfaceNumber	Zero based index of this interface = 0	00H
3	bAlternateSetting	Alternate Setting Value = 3	03H
4	bNumEndpoints	Number of endpoints in this interface (not counting EP0) = 6	06H
5	bInterfaceClass	Interface Class = Vendor Specific	FFH
6	bInterfaceSubClass	Interface Sub-class = Vendor Specific	FFH
7	bInterfaceProtocol	Interface Protocol = Vendor Specific	FFH
8	iInterface	Index to string descriptor for this interface = None	00H

Table B-20 Endpoint Descriptor (EP1 out)

Offset	Field	Description	Value
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and address = OUT1	01H
3	bmAttributes	XFR Type = INT	03H
4	wMaxPacketSize (L)	Maximum Packet Size = 64 bytes	40H
5	WMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	01H

Table B-21 Endpoint Descriptor (EP1 in)

Offset	Field	Description	Value
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and address = IN1	81H
3	bmAttributes	XFR Type = INT	03H
4	wMaxPacketSize (L)	Maximum Packet Size = 64 bytes	40H
5	WMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	01H

Table B-22 Endpoint Descriptor (EP2)

Offset	Field	Description	Value
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and address = OUT2	02H
3	bmAttributes	XFR Type = ISO, No Synchronization, Data endpoint	01H
4	wMaxPacketSize (L)	Maximum Packet Size = 512 bytes	00H
5	WMaxPacketSize (H)	Maximum Packet Size - High	02H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	01H

Table B-23 Endpoint Descriptor (EP4)

Offset	Field	Description	Value
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and address = OUT4	04H
3	bmAttributes	XFR Type = BULK	02H
4	wMaxPacketSize (L)	Maximum Packet Size = 512 bytes	00H
5	WMaxPacketSize (H)	Maximum Packet Size - High	02H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	00H

Table B-24 Endpoint Descriptor (EP6)

Offset	Field	Description	Value
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and address = IN6	86H
3	bmAttributes	XFR Type = ISO, No Synchronization, Data endpoint	01H
4	wMaxPacketSize (L)	Maximum Packet Size = 512 bytes	00H
5	WMaxPacketSize (H)	Maximum Packet Size - High	02H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	01H

Table B-25 Endpoint Descriptor (EP8)

Offset	Field	Description	Value
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and address = IN8	88H
3	bmAttributes	XFR Type = BULK	02H
4	wMaxPacketSize (L)	Maximum Packet Size = 512 bytes	00H
5	WMaxPacketSize (H)	Maximum Packet Size - High	02H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	00H

Appendix C
FX2 Register Summary

The following table is a summary of all the EZ-USB FX2 Registers.

In the “b7-b0” columns, bit positions that contain a 0 or a 1 cannot be written to and, when read, always return the value shown (0 or 1). Bit positions that contain “-” are available but unused.

The “Default” column shows each register’s power-on-reset value (“x” indicates “undefined”).

The “Access” column indicates each register’s read/write accessibility.

Register Summary

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access	Notes
		GPIF Waveform Memories												
E400	128	WAVEDATA	GPIF Waveform Descriptor 0, 1, 2, 3 data	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW	associated / pointed to by GPIFWFSELECT
E480	384	reserved												
		GENERAL CONFIGURATION												
E600	1	CPUCS	CPU Control & Status	0	0	PORTCSTB	CLKSPD1	CLKSPD0	CLKINV	CLKOE	8051RES	00000010	rrbbbbbr	**PORTCSTB**=1: reads/writes to PORTC generate RD# and WR# strobes **CLKSPD1:0**=8051 clock speed: 00=12, 01-24, 10=48, 11=X **CLKINV**=1 to invert CLKOUT signal **CLKOE**=1 to drive CLKOUT pin **8051RES**=1 to reset 8051
E601	1	IFCONFIG	Interface Configuration (Ports, GPIF, slave FIFOs)	IFCLKSRC	3048MHZ	IFCLKOE	IFCLKPOL	ASYNC	GSTATE	IFCFG1	IFCFG0	11000000	RW	**IFCLKSRC**: FIFO/GPIF Clock Source: 0:external (IFGCLK pin); 1:internal **3048MHZ**: Internal FIFO/ GPIF clock freq: 0=30 MHz, 1=48 MHz **IFCLKOE**: FIFO/GPIF Clock Output Enable (on IFCLK pin) **IFCLKPOL**: FIFO/GPIF clock polarity (on IFCLK pin) **ASYNC**: 1=FIFOs/GPIF use internal clock (30/48); 0=use external IFCLK **GSTATE**: 1: drive GSTATE[0:2] on PORTE[0:2] **IFCFG[1:0]**: 00: ports; 01: reserved; 10: GPIF; 11: Slave FIFO (ext master)
E602	1	PINFLAGSAB ***see Section 15.14***	Slave FIFO FLAGA and FLAGB Pin Configuration	FLAGB3	FLAGB2	FLAGB1	FLAGB0	FLAGA3	FLAGA2	FLAGA1	FLAGA0	00000000	RW	**FLAGx[3:0]** where x=A,B,C or D FIFO Flag: 0000: PF for FIFO selected by FIFOADR[1:0] pins. 0001-0011: reserved 0100: EP2 PF, 0101: EP4PF, 0110: EP6PF, 0111: EP8 PF 1000: EP2 EF, 1001: EP4EF, 1010: EP6EF, 1011: EP8 EF 1100: EP2 FF, 1101: EP4FF, 1110: EP6FF, 1111: EP8FF
E603	1	PINFLAGSCD ***see Section 15.14***	Slave FIFO FLAGC and FLAGD Pin Configuration	FLAGD3	FLAGD2	FLAGD1	FLAGD0	FLAGC3	FLAGC2	FLAGC1	FLAGC0	01000000	RW	
E604	1	FIFORESET ***see Section 15.14***	Restore FIFOS to default state	NAKALL	0	0	0	EP3	EP2	EP1	EP0	xxxxxxxx	W	Set flags and byte counts to default values; write 0x80 to NAK all transfers, then write FIFO number, then write 0x00 to restore normal operation
E605	1	BREAKPT	Breakpoint Control	0	0	0	0	BREAK	BPPULSE	BPEN	0	00000000	rrrrbbbr	
E606	1	BPADDRH	Breakpoint Address H	A15	A14	A13	A12	A11	A10	A9	A8	xxxxxxxx	RW	
E607	1	BPADDRL	Breakpoint Address L	A7	A6	A5	A4	A3	A2	A1	A0	xxxxxxxx	RW	

EZ-USB FX2 Registers & Buffers

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access	Notes
E608	1	UART230	230 Kbaud internally generated ref. clock	0	0	0	0	0	0	230UART1	230UART0	00000000	rrrrrrbb	If "1", overrides timer inputs to UART. 230 rate valid for any CPU clock rate.
E609	1	FIFOPINPOLAR ***see Section 15.14***	slave FIFO Interface pins polarity	0	0	PKTEND	SLOE	SLRD	SLWR	EF	FF	00000000	rrbbbbbb	0=active low, 1=active high
E60A	1	REVID	Chip Revision	rv7	rv6	rv5	rv4	rv3	rv2	rv1	rv0	See Datasheet	R	Chip revision number
E60B	1	REVCTL	Chip Revision Control	0	0	0	0	0	0	dyn_out	enh_pkt	00000000	rrrrrrbb	
		UDMA												
E60C	1	GPIFHOLDTIME	MSTB Hold Time (for UDMA)	0	0	0	0	0	0	HOLDTIME1	HOLDTIME0	00000000	rrrrrrbb	
	3	reserved												
		ENDPOINT CONFIGURATION												**TYPE[00]** = illegal; 01=ISO, 10=BULK, 11=INT. dir=0:OUT; dir=1:IN **BUF1:0**: 00=quad, 01=illegal, 10=double, 11=triple **SIZE**=0: 512 bytes, SIZE=1: 1024 bytes
E610	1	EP1OUTCFG	Endpoint 1-OUT Configuration	VALID	0	TYPE1	TYPE0	0	0	0	0	10100000	brbbrrrr	default: BULK OUT 64
E611	1	EP1INCFG	Endpoint 1-IN Configuration	VALID	0	TYPE1	TYPE0	0	0	0	0	10100000	brbbrrrr	default: BULK OUT 64
E612	1	EP2CFG	Endpoint 2 Configuration	VALID	DIR	TYPE1	TYPE0	SIZE	0	BUF1	BUF0	10100010	bbbbbrbb	default: BULK OUT 512 double buffered
E613	1	EP4CFG	Endpoint 4 Configuration	VALID	DIR	TYPE1	TYPE0	0	0	0	0	10100000	bbbbrrrr	default: BULK OUT (512 double buffered only choice)
E614	1	EP6CFG	Endpoint 6 Configuration	VALID	DIR	TYPE1	TYPE0	SIZE	0	BUF1	BUF0	11100010	bbbbbrbb	default: BULK IN 512 double buffered
E615	1	EP8CFG	Endpoint 8 Configuration	VALID	DIR	TYPE1	TYPE0	0	0	0	0	11100000	bbbbrrrr	default: BULK IN (512 double buffered only choice)
	2	reserved												
E618	1	EP2FIFOCFG ***see Section 15.14***	Endpoint 2 / slave FIFO configuration	0	INFM1	OEP1	AUTOOUT	AUTOIN	ZEROLENIN	0	WORDWIDE	00000101	rbbbbbrb	**INFM1** (In FULL flag minus 1): 0=normal, 1=flags active one byte early **OEP1** (Out EMPTY flag plus 1): 0=normal, 1=flags active one byte early **AUTOOUT**=1--valid OUT packet automatically becomes part of OUT FIFO **AUTOOUT**=0--8051 decides if to commit data to the OUT FIFO **AUTOIN**=1--SIE packetizes/ dispatches IN-FIFO data using EPxAUTOINLEN **AUTOIN**=0--8051 dispatches an IN packet by writing byte count **WORDWIDE**=1: PB=FD[0:7], PD=FD[8:15]; =1: PB=FD[0:7], PD=PD **ZEROLENIN**: 0=disable; 1=send zero len pkt on PKTEND - If any of the four WORDWIDE bits=1, core configures PD as FD15:8
E619	1	EP4FIFOCFG ***see Section 15.14***	Endpoint 4 / slave FIFO configuration	0	INFM1	OEP1	AUTOOUT	AUTOIN	ZEROLENIN	0	WORDWIDE	00000101	rbbbbbrb	
E61A	1	EP6FIFOCFG ***see Section 15.14***	Endpoint 6 / slave FIFO configuration	0	INFM1	OEP1	AUTOOUT	AUTOIN	ZEROLENIN	0	WORDWIDE	00000101	rbbbbbrb	
E61B	1	EP8FIFOCFG ***see Section 15.14***	Endpoint 8 / slave FIFO configuration	0	INFM1	OEP1	AUTOOUT	AUTOIN	ZEROLENIN	0	WORDWIDE	00000101	rbbbbbrb	
	4	reserved												

EZ-USB FX2 Registers & Buffers

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access	Notes
E620	1	EP2AUTOINLENH ***see Section 15.14***	Endpoint 2 AUTOIN Packet Length H	0	0	0	0	0	PL10	PL9	PL8	00000010	rrrrrbbb	Default is 512 byte packets; can set smaller IN packets. SIE divides IN-FIFO data into this-length packets when AUTOIN=1. When AUTOIN=0, 8051 loads a byte count for every packet (in EPxBCH/L). EP2,6 can have 1024 max bytes, EP4,8 can have 512 max bytes. these registers only used for AUTOIN
E621	1	EP2AUTOINLENL ***see Section 15.14***	Endpoint 2 AUTOIN Packet Length L	PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0	00000000	RW	
E622	1	EP4AUTOINLENH ***see Section 15.14***	Endpoint 4 AUTOIN Packet Length H	0	0	0	0	0	0	PL9	PL8	00000010	rrrrrrbb	
E623	1	EP4AUTOINLENL ***see Section 15.14***	Endpoint 4 AUTOIN Packet Length L	PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0	00000000	RW	
E624	1	EP6AUTOINLENH ***see Section 15.14***	Endpoint 6 AUTOIN Packet Length H	0	0	0	0	0	PL10	PL9	PL8	00000010	rrrrrbbb	
E625	1	EP6AUTOINLENL ***see Section 15.14***	Endpoint 6 AUTOIN Packet Length L	PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0	00000000	RW	
E626	1	EP8AUTOINLENH ***see Section 15.14***	Endpoint 8 AUTOIN Packet Length H	0	0	0	0	0	0	PL9	PL8	00000010	rrrrrrbb	
E627	1	EP8AUTOINLENL ***see Section 15.14***	Endpoint 8 AUTOIN Packet Length L	PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0	00000000	RW	
	8	reserved												
E630 H.S.	1	EP2FIFOPFH ***see Section 15.14***	Endpoint 2 / slave FIFO Programmable Flag H	DECIS	PKTSTAT	IN:PKTS[2] OUT:PFC12	IN:PKTS[1] OUT:PFC11	IN:PKTS[0] OUT:PFC10	0	PFC9	PFC8	10001000	bbbbbrbb	**DECIS**: PF decision bit. 0: PF=1 when BC <= PF; 1: PF=1 when BC >= PF **PKTSTAT**=0--PF and BC refer to full FIFO; =1: PF/BC refer to current packet (IN) (OUT) PF/BC refer to full FIFO
E630 F.S.	1	EP2FIFOPFH ***see Section 15.14***	Endpoint 2 / slave FIFO Programmable Flag H	DECIS	PKTSTAT	OUT:PFC12	OUT:PFC11	OUT:PFC10	0	PFC9	IN:PKTS[2] OUT:PFC8	10001000	bbbbbrbb	
E631 H.S.	1	EP2FIFOPFL ***see Section 15.14***	Endpoint 2 / slave FIFO Programmable Flag L	PFC7	PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW	
E631 F.S	1	EP2FIFOPFL ***see Section 15.14***	Endpoint 2 / slave FIFO Programmable Flag L	IN:PKTS[1] OUT:PFC7	IN:PKTS[0] OUT:PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW	
E632 H.S.	1	EP4FIFOPFH ***see Section 15.14***	Endpoint 4 / slave FIFO Programmable Flag H	DECIS	PKTSTAT	0	IN: PKTS[1] OUT:PFC10	IN: PKTS[0] OUT:PFC9	0	0	PFC8	10001000	bbrbbrrb	max 1024
E632 F.S	1	EP4FIFOPFH ***see Section 15.14***	Endpoint 4 / slave FIFO Programmable Flag H	DECIS	PKTSTAT	0	OUT:PFC10	OUT:PFC9	0	0	PFC8	10001000	bbrbbrrb	max 1024
E633 H.S.	1	EP4FIFOPFL ***see Section 15.14***	Endpoint 4 / slave FIFO Programmable Flag L	PFC7	PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW	
E633 F.S	1	EP4FIFOPFL ***see Section 15.14***	Endpoint 4 / slave FIFO Programmable Flag L	IN: PKTS[1] OUT:PFC7	IN: PKTS[0] OUT:PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW	
E634 H.S.	1	EP6FIFOPFH ***see Section 15.14***	Endpoint 6 / slave FIFO Programmable Flag H	DECIS	PKTSTAT	IN:PKTS[2] OUT:PFC12	IN:PKTS[1] OUT:PFC11	IN:PKTS[0] OUT:PFC10	0	PFC9	PFC8	00001000	bbbbbrbb	max 2048
E634 F.S	1	EP6FIFOPFH ***see Section 15.14***	Endpoint 6 / slave FIFO Programmable Flag H	DECIS	PKTSTAT	OUT:PFC12	OUT:PFC11	OUT:PFC10	0	PFC9	IN:PKTS[2] OUT:PFC8	00001000	bbbbbrbb	max 2048
E635 H.S.	1	EP6FIFOPFL ***see Section 15.14***	Endpoint 6 / slave FIFO Programmable Flag L	PFC7	PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW	
E635 F.S	1	EP6FIFOPFL ***see Section 15.14***	Endpoint 6 / slave FIFO Programmable Flag L	IN:PKTS[1] OUT:PFC7	IN:PKTS[0] OUT:PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW	
E636 H.S.	1	EP8FIFOPFH ***see Section 15.14***	Endpoint 8 / slave FIFO Programmable Flag H	DECIS	PKTSTAT	0	IN: PKTS[1] OUT:PFC10	IN: PKTS[0] OUT:PFC9	0	0	PFC8	00001000	bbrbbrrb	max 1024
E636 F.S	1	EP8FIFOPFH ***see Section 15.14***	Endpoint 8 / slave FIFO Programmable Flag H	DECIS	PKTSTAT	0	OUT:PFC10	OUT:PFC9	0	0	PFC8	00001000	bbrbbrrb	max 1024
E637 H.S.	1	EP8FIFOPFL ***see Section 15.14***	Endpoint 8 / slave FIFO Programmable Flag L	PFC7	PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW	
E637 F.S	1	EP8FIFOPFL ***see Section 15.14***	Endpoint 8 / slave FIFO Programmable Flag L	IN: PKTS[1] OUT:PFC7	IN: PKTS[0] OUT:PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW	
	8	reserved												

EZ-USB FX2 Registers & Buffers

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access	Notes
E640	1	EP2ISOINPKTS	EP2 (if ISO) IN Packets per frame (1-3)	0	0	0	0	0	0	INPPF1	INPPF0	00000001	rrrrrrbb	**INPPF1:0**: 00=illegal, 01=1 per frame, 10=2 per frame, 11=3 per frame
E641	1	EP4ISOINPKTS	EP4 (if ISO) IN Packets per frame (1-3)	0	0	0	0	0	0	INPPF1	INPPF0	00000001	rrrrrrbb	
E642	1	EP6ISOINPKTS	EP6 (if ISO) IN Packets per frame (1-3)	0	0	0	0	0	0	INPPF1	INPPF0	00000001	rrrrrrbb	
E643	1	EP8ISOINPKTS	EP8 (if ISO) IN Packets per frame (1-3)	0	0	0	0	0	0	INPPF1	INPPF0	00000001	rrrrrrbb	
	4	reserved												
E648	1	INPKTEND ***see Section 15.14***	Force IN Packet End	Skip	0	0	0	EP3	EP2	EP1	EP0	xxxxxxxx	W	Same function as slave interface PKTEND pin, but 8051 controls dispatch of IN, Typically used after a GPIF FIFO transaction completes to send jagged edge pkt, user needs to check status of FIFO full flag for available buffer before doing PKTEND
E649	7	OUTPKTEND	Force out Packet End	Skip	0	0	0	EP3	EP2	EP1	EP0	xxxxxxxx	W	REVCTL.0=1 to enable this feature
		INTERRUPTS												
E650	1	EP2FIFOIE ***see Section 15.14***	Endpoint 2 slave FIFO Flag Interrupt Enable	0	0	0	0	EDGEPF	PF	EF	FF	00000000	RW	EDGEPF=0; Rising edge EDGEPF=1; Falling edge
E651	1	EP2FIFOIRQ ***see Section 15.14***	Endpoint 2 slave FIFO Flag Interrupt Request	0	0	0	0	0	PF	EF	FF	00000000	RW	
E652	1	EP4FIFOIE ***see Section 15.14***	Endpoint 4 slave FIFO Flag Interrupt Enable	0	0	0	0	EDGEPF	PF	EF	FF	00000000	RW	
E653	1	EP4FIFOIRQ ***see Section 15.14***	Endpoint 4 slave FIFO Flag Interrupt Request	0	0	0	0	0	PF	EF	FF	00000000	RW	
E654	1	EP6FIFOIE ***see Section 15.14***	Endpoint 6 slave FIFO Flag Interrupt Enable	0	0	0	0	EDGEPF	PF	EF	FF	00000000	RW	
E655	1	EP6FIFOIRQ ***see Section 15.14***	Endpoint 6 slave FIFO Flag Interrupt Request	0	0	0	0	0	PF	EF	FF	00000000	RW	
E656	1	EP8FIFOIE ***see Section 15.14***	Endpoint 8 slave FIFO Flag Interrupt Enable	0	0	0	0	EDGEPF	PF	EF	FF	00000000	RW	
E657	1	EP8FIFOIRQ ***see Section 15.14***	Endpoint 8 slave FIFO Flag Interrupt Request	0	0	0	0	0	PF	EF	FF	00000000	RW	
E658	1	IBNIE	IN-BULK-NAK Interrupt Enable	0	0	EP8	EP6	EP4	EP2	EP1	EP0	00000000	RW	
E659	1	IBNIRQ	IN-BULK-NAK interrupt Request	0	0	EP8	EP6	EP4	EP2	EP1	EP0	00000000	RW	1 = clear request, 0= no effect
E65A	1	NAKIE	Endpoint Ping-NAK / IBN Interrupt Enable	EP8	EP6	EP4	EP2	EP1	EP0	0	IBN	00000000	RW	OUT endpoint was pinged and NAK'd
E65B	1	NAKIRQ	Endpoint Ping-NAK / IBN Interrupt Request	EP8	EP6	EP4	EP2	EP1	EP0	0	IBN	00000000	RW	
E65C	1	USBIE	USB Int Enables	0	EP0ACK	HSGRANT	URES	SUSP	SUTOK	SOF	SUDAV	00000000	RW	
E65D	1	USBIRQ	USB Interrupt Requests	0	EP0ACK	HSGRANT	URES	SUSP	SUTOK	SOF	SUDAV	00000000	RW	1 = clear request, 0= no effect
E65E	1	EPIE	Endpoint Interrupt Enables	EP8	EP6	EP4	EP2	EP1OUT	EP1IN	EP0OUT	EP0IN	00000000	RW	
E65F	1	EPIRQ	Endpoint Interrupt Requests	EP8	EP6	EP4	EP2	EP1OUT	EP1IN	EP0OUT	EP0IN	00000000	RW	1 = clear request, 0= no effect

EZ-USB FX2 Registers & Buffers

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access	Notes
E660	1	GPIFIE ***see Section 15.14***	GPIF Interrupt Enable	0	0	0	0	0	0	GPIFWF	GPIFDONE	00000000	RW	WF--8051 "hook" in waveform, DONE-returned to IDLE state
E661	1	GPIFIRQ ***see Section 15.14***	GPIF Interrupt Request	0	0	0	0	0	0	GPIFWF	GPIFDONE	00000000	RW	Write "1" to clear
E662	1	USBERRIE	USB Error Interrupt Enables	ISOEP8	ISOEP6	ISOEP4	ISOEP2	0	0	0	ERRLIMIT	00000000	RW	ISO endpoint error: PID sequence error or dropped packet (no available buffer)
E663	1	USBERRIRQ	USB Error Interrupt Requests	ISOEP8	ISOEP6	ISOEP4	ISOEP2	0	0	0	ERRLIMIT	00000000	RW	
E664	1	ERRCNTLIM	USB Error counter and limit	EC3	EC2	EC1	EC0	LIMIT3	LIMIT2	LIMIT1	LIMIT0	xxxx0100	rrrrbbbb	Default limit count is 4
E665	1	CLRERRCNT	Clear Error Counter EC3:0	x	x	x	x	x	x	x	x	xxxxxxxx	W	
E666	1	INT2IVEC	Interrupt 2 (USB) Autovector	0	I2V4	I2V3	I2V2	I2V1	I2V0	0	0	00000000	R	
E667	1	INT4IVEC	Interrupt 4 (slave FIFO & GPIF) Autovector	1	0	I4V3	I4V2	I4V1	I4V0	0	0	10000000	R	
E668	1	INTSETUP	Interrupt 2&4 Setup	0	0	0	0	AV2EN	0	INT4SRC	AV4EN	00000000	RW	INT4IN=0: INT4 from pin; 1: INT4 from FIFO/GPIF interrupts
E669	7	reserved												
		INPUT / OUTPUT												
E670	1	PORTACFG	I/O PORTA Alternate Configuration	FLAGD	SLCS	0	0	0	0	INT1	INT0	00000000	RW	
E671	1	PORTCCFG	I/O PORTC Alternate Configuration	GPIFA7	GPIFA6	GPIFA5	GPIFA4	GPIFA3	GPIFA2	GPIFA1	GPIFA0	00000000	RW	
E672	1	PORTECFG	I/O PORTE Alternate Configuration	GPIFA8	T2EX	INT6	RXD1OUT	RXD0OUT	T2OUT	T1OUT	T0OUT	00000000	RW	GSTATE bit =1 overrides bits 2:0.
E673	5	reserved												
E678	1	I2CS	I²C-Compatible Bus Control & Status	START	STOP	LASTRD	ID1	ID0	BERR	ACK	DONE	000xx000	bbbrrrrr	
E679	1	I2DAT	I²C-Compatible Bus Data	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	RW	
E67A	1	I2CTL	I²C-Compatible Bus Control	0	0	0	0	0	0	STOPIE	400KHZ	00000000	RW	
E67B	1	XAUTODAT1	Autoptr1 MOVX access, when APTREN=1	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW	AUTOPTRSETUP bit APTREN=1: off-chip access use this reg - code-space hole at this location AUTOPTRSETUP bit APTREN=0: on-chip access use duplicate SFR @ 9C , no code-space hole
E67C	1	XAUTODAT2	Autoptr2 MOVX access, when APTREN=1	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW	
		UDMA CRC												
E67D	1	UDMACRCH ***see Section 15.14***	UDMA CRC MSB	CRC15	CRC14	CRC13	CRC12	CRC11	CRC10	CRC9	CRC8	01001010	RW	
E67E	1	UDMACRCL ***see Section 15.14***	UDMA CRC LSB	CRC7	CRC6	CRC5	CRC4	CRC3	CRC2	CRC1	CRC0	10111010	RW	
E67F	1	UDMACRC-QUALIFIER	UDMA CRC Qualifier	QENABLE	0	0	0	QSTATE	QSIGNAL2	QSIGNAL1	QSIGNAL0	00000000	brrrbbbb	
		USB CONTROL												
E680	1	USBCS	USB Control & Status	HSM	0	0	0	DISCON	NOSYNSOF	RENUM	SIGRSUME	x0000000	rrrrbbbb	
E681	1	SUSPEND	Put chip into suspend	x	x	x	x	x	x	x	x	xxxxxxxx	W	Write 0xFF to suspend

EZ-USB FX2 Registers & Buffers

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access	Notes
E682	1	WAKEUPCS	Wakeup Control & Status	WU2	WU	WU2POL	WUPOL	0	DPEN	WU2EN	WUEN	xx000101	bbbbrbbb	
E683	1	TOGCTL	Toggle Control	Q	S	R	IO	EP3	EP2	EP1	EP0	00000000	rbbbbbbb	
E684	1	USBFRAMEH	USB Frame count H	0	0	0	0	0	FC10	FC9	FC8	00000xxx	R	
E685	1	USBFRAMEL	USB Frame count L	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0	xxxxxxxx	R	
E686	1	MICROFRAME	Microframe count, 0-7	0	0	0	0	0	MF2	MF1	MF0	00000xxx	R	
E687	1	FNADDR	USB Function address	0	FA6	FA5	FA4	FA3	FA2	FA1	FA0	00000000	R	
E688	2	reserved												
		ENDPOINTS												
E68A	1	EP0BCH	Endpoint 0 Byte Count H	(BC15)	(BC14)	(BC13)	(BC12)	(BC11)	(BC10)	(BC9)	(BC8)	xxxxxxxx	RW	Even though the EP0 buffer is only 64 bytes, the EP0 byte count is expanded to 16-bits to allow using the Autoptr with a custom length, instead of USB-dictated length (from Setup Data Packet and number of requested bytes). The byte count bits in parentheses apply only when SDPAUTO = 0
E68B	1	EP0BCL	Endpoint 0 Byte Count L	(BC7)	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxxx	RW	
E68C	1	reserved												
E68D	1	EP1OUTBC	Endpoint 1 OUT Byte Count	0	BC6	BC5	BC4	BC3	BC2	BC1	BC0	0xxxxxxx	RW	
E68E	1	reserved												
E68F	1	EP1INBC	Endpoint 1 IN Byte Count	0	BC6	BC5	BC4	BC3	BC2	BC1	BC0	0xxxxxxx	RW	
E690	1	EP2BCH ***see Section 15.14***	Endpoint 2 Byte Count H	0	0	0	0	0	BC10	BC9	BC8	00000xxx	RW	EP2,6 can be 512 or 1024 EP4,8 are 512 only
E691	1	EP2BCL ***see Section 15.14***	Endpoint 2 Byte Count L	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxxx	RW	
E692	2	reserved												
E694	1	EP4BCH ***see Section 15.14***	Endpoint 4 Byte Count H	0	0	0	0	0	0	BC9	BC8	000000xx	RW	
E695	1	EP4BCL ***see Section 15.14***	Endpoint 4 Byte Count L	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxxx	RW	
E696	2	reserved												
E698	1	EP6BCH ***see Section 15.14***	Endpoint 6 Byte Count H	0	0	0	0	0	BC10	BC9	BC8	00000xxx	RW	
E699	1	EP6BCL ***see Section 15.14***	Endpoint 6 Byte Count L	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxxx	RW	
E69A	2	reserved												
E69C	1	EP8BCH ***see Section 15.14***	Endpoint 8 Byte Count H	0	0	0	0	0	0	BC9	BC8	000000xx	RW	
E69D	1	EP8BCL ***see Section 15.14***	Endpoint 8 Byte Count L	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxxx	RW	
E69E	2	reserved												
E6A0	1	EP0CS	Endpoint 0 Control and Status	HSNAK	0	0	0	0	0	BUSY	STALL	10000000	bbbbbbrb	
E6A1	1	EP1OUTCS	Endpoint 1 OUT Control and Status	0	0	0	0	0	0	BUSY	STALL	00000000	bbbbbbrb	
E6A2	1	EP1INCS	Endpoint 1 IN Control and Status	0	0	0	0	0	0	BUSY	STALL	00000000	bbbbbbrb	

EZ-USB FX2 Registers & Buffers

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access	Notes
E6A3	1	EP2CS	Endpoint 2 Control and Status	0	NPAK2	NPAK1	NPAK0	FULL	EMPTY	0	STALL	00101000	rrrrrrrb	NPAK2:0=number of packets in the FIFO, 0-4. NPAK1:0=number of packets in the FIFO, 0-2" OUT: Packets received from USB. IN: Packets loaded and armed. FULL / EMPTY status bits duplicated in SFR space, EP2468STAT
E6A4	1	EP4CS	Endpoint 4 Control and Status	0	0	NPAK1	NPAK0	FULL	EMPTY	0	STALL	00101000	rrrrrrrb	
E6A5	1	EP6CS	Endpoint 6 Control and Status	0	NPAK2	NPAK1	NPAK0	FULL	EMPTY	0	STALL	00000100	rrrrrrrb	
E6A6	1	EP8CS	Endpoint 8 Control and Status	0	0	NPAK1	NPAK0	FULL	EMPTY	0	STALL	00000100	rrrrrrrb	
E6A7	1	EP2FIFOFLGS	Endpoint 2 slave FIFO Flags	0	0	0	0	0	PF	EF	FF	00000010	R	Not affected by FIFOPINPOLAR bits. duplicated in SFR space, EP24FIFOFLGS and EP68FIFOFLGS
E6A8	1	EP4FIFOFLGS	Endpoint 4 slave FIFO Flags	0	0	0	0	0	PF	EF	FF	00000010	R	
E6A9	1	EP6FIFOFLGS	Endpoint 6 slave FIFO Flags	0	0	0	0	0	PF	EF	FF	00000110	R	
E6AA	1	EP8FIFOFLGS	Endpoint 8 slave FIFO Flags	0	0	0	0	0	PF	EF	FF	00000110	R	
E6AB	1	EP2FIFOBCH	Endpoint 2 slave FIFO total byte count H	0	0	0	BC12	BC11	BC10	BC9	BC8	00000000	R	OUT: full byte count; IN: bytes in current packet EP2 max 4096 EP$ max 1024 EP6 max 2048 EP* max 1024
E6AC	1	EP2FIFOBCL	Endpoint 2 slave FIFO total byte count L	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0	00000000	R	
E6AD	1	EP4FIFOBCH	Endpoint 4 slave FIFO total byte count H	0	0	0	0	0	BC10	BC9	BC8	00000000	R	
E6AE	1	EP4FIFOBCL	Endpoint 4 slave FIFO total byte count L	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0	00000000	R	
E6AF	1	EP6FIFOBCH	Endpoint 6 slave FIFO total byte count H	0	0	0	0	BC11	BC10	BC9	BC8	00000000	R	
E6B0	1	EP6FIFOBCL	Endpoint 6 slave FIFO total byte count L	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0	00000000	R	
E6B1	1	EP8FIFOBCH	Endpoint 8 slave FIFO total byte count H	0	0	0	0	0	BC10	BC9	BC8	00000000	R	
E6B2	1	EP8FIFOBCL	Endpoint 8 slave FIFO total byte count L	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0	00000000	R	
E6B3	1	SUDPTRH	Setup Data Pointer high address byte	A15	A14	A13	A12	A11	A10	A9	A8	xxxxxxxx	RW	
E6B4	1	SUDPTRL	Setup Data Pointer low address byte	A7	A6	A5	A4	A3	A2	A1	0	xxxxxxx0	bbbbbbbr	Must be word-aligned (i.e., must point to even-numbered addresses)
E6B5	1	SUDPTRCTL	Setup Data Pointer Auto Mode	0	0	0	0	0	0	0	SDPAUTO	00000001	RW	Clear b0 to supply SUDPTR length (override USB length)
	2	reserved												
E6B8	8	SETUPBUF	8 bytes of SETUP data	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	R	
			SETUPDAT[0] = bmRequestType											D7: Data Transfer Direction; 0=host-to-device, 1=device-to-host D6…5 Type; 0=standard, 1=class, 2=vendor, 3=reserved D4…0 Recipient; 0=device, 1=interface, 2=endpoint, 3=other, 4…31=reserved
			SETUPDAT[1] = bmRequest											specific request
			SETUPDAT[2:3] = wValue											word-sized field that varies according to request

EZ-USB FX2 Registers & Buffers

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access	Notes
			SETUPDAT[4:5] = wIndex											word-sized field that varies according to request; typ. used to pass an index or offset
			SETUPDAT[6:7] = wLength											number of bytes to transfer if there is a data stage
		GPIF												
E6C0	1	GPIFWFSELECT	Waveform Selector	SINGLEWR1	SINGLEWR0	SINGLERD1	SINGLERD0	FIFOWR1	FIFOWR0	FIFORD1	FIFORD0	11100100	RW	Select waveform
E6C1	1	GPIFIDLECS	GPIF Done, GPIF IDLE drive mode	DONE	0	0	0	0	0	0	IDLEDRV	10000000	RW	DONE=1: GPIF done (IRQ4). IDLEDRV=1: drive bus, 0:TS DONE duplicated in SFR space, GPIFTRIG bit 7
E6C2	1	GPIFIDLECTL	Inactive Bus, CTL states	0	0	CTL5	CTL4	CTL3	CTL2	CTL1	CTL0	11111111	RW	
E6C3	1	GPIFCTLCFG	CTL Drive Type	TRICTL	0	CTL5	CTL4	CTL3	CTL2	CTL1	CTL0	00000000	RW	0=CMOS, 1=open drn.
E6C4	1	GPIFADRH ***see Section 15.14***	GPIF Address H	0	0	0	0	0	0	0	GPIFA8	00000000	RW	GPIFADRH/L active immediately when written to
E6C5	1	GPIFADRL ***see Section 15.14***	GPIF Address L	GPIFA7	GPIFA6	GPIFA5	GPIFA4	GPIFA3	GPIFA2	GPIFA1	GPIFA0	00000000	RW	
		FLOWSTATE												
E6C6	1	FLOWSTATE	Flowstate Enable and Selector	FSE	0	0	0	0	FS2	FS1	FS0	00000000	brrrrbbb	
E6C7	1	FLOWLOGIC	Flowstate Logic	LFUNC1	LFUNC0	TERMA2	TERMA1	TERMA0	TERMB2	TERMB1	TERMB0	00000000	RW	
E6C8	1	FLOWEQ0CTL	CTL-Pin States in Flowstate (when Logic = 0)	CTL0E3	CTL0E2	CTL0E1/ CTL5	CTL0E0/ CTL4	CTL3	CTL2	CTL1	CTL0	00000000	RW	
E6C9	1	FLOWEQ1CTL	CTL-Pin States in Flowstate (when Logic = 1)	CTL0E3	CTL0E2	CTL0E1/ CTL5	CTL0E0/ CTL4	CTL3	CTL2	CTL1	CTL0	00000000	RW	
E6CA	1	FLOWHOLDOFF	Holdoff Configuration	HOPERIOD3	HOPERIOD2	HOPERIOD1	HOPERIOD0	HOSTATE	HOCTL2	HOCTL1	HOCTL0	00010010	RW	
E6CB	1	FLOWSTB	Flowstate Strobe Configuration	SLAVE	RDYASYNC	CTLTOGL	SUSTAIN	0	MSTB2	MSTB1	MSTB0	00100000	RW	
E6CC	1	FLOWSTBEDGE	Flowstate Rising/Falling Edge Configuration	0	0	0	0	0	0	FALLING	RISING	00000001	rrrrrrbb	
E6CD	1	FLOWSTBPERIOD	Master-Strobe Half-Period	D7	D6	D5	D4	D3	D2	D1	D0	00000010	RW	In units of IFCLK/2. Must be >= 2
E6CE	1	GPIFTCB3	GPIF Transaction Count Byte3	TC31	TC30	TC29	TC28	TC27	TC26	TC25	TC24	00000000	RW	Reading these registers give you the live Transaction Count. Default=1
E6CF	1	GPIFTCB2	GPIF Transaction Count Byte2	TC23	TC22	TC21	TC20	TC19	TC18	TC17	TC16	00000000	RW	
E6D0	1	GPIFTCB1	GPIF Transaction Count Byte1	TC15	TC14	TC13	TC12	TC11	TC10	TC9	TC8	00000000	RW	
E6D1	1	GPIFTCB0	GPIF Transaction Count Byte0	TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0	00000001	RW	
	2	reserved										00000000	RW	
		reserved												
		reserved												
E6D2	1	EP2GPIFFLGSEL ***see Section 15.14***	Endpoint 2 GPIF Flag select	0	0	0	0	0	0	FS1	FS0	00000000	RW	00: Programmable flag; 01: Empty, 10: Full, 11: reserved
E6D3	1	EP2GPIFPFSTOP	Endpoint 2 GPIF stop transaction on prog. flag	0	0	0	0	0	0	0	FIFO2FLAG	00000000	RW	1=override TC value, stop on FIFO Prog. Flag.
E6D4	1	EP2GPIFTRIG ***see Section 15.14***	Endpoint 2 GPIF Trigger	x	x	x	x	x	x	x	x	xxxxxxxx	W	Start GPIF transactions, duplicated in SFR - GPIFTRIG
	3	reserved												
		reserved												
		reserved												

EZ-USB FX2 Registers & Buffers

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access	Notes
E6DA	1	EP4GPIFFLGSEL ***see Section 15.14***	Endpoint 4 GPIF Flag select	0	0	0	0	0	0	FS1	FS0	00000000	RW	00: Programmable-Level; 01: Empty, 10: Full, 11: reserved
E6DB	1	EP4GPIFPFSTOP	Endpoint 4 GPIF stop transaction on GPIF Flag	0	0	0	0	0	0	0	FIFO4FLAG	00000000	RW	
E6DC	1	EP4GPIFTRIG ***see Section 15.14***	Endpoint 4 GPIF Trigger	x	x	x	x	x	x	x	x	xxxxxxxx	W	Start GPIF transactions, duplicated in SFR - GPIFTRIG
	3	reserved												
		reserved												
		reserved												
E6E2	1	EP6GPIFFLGSEL ***see Section 15.14***	Endpoint 6 GPIF Flag select	0	0	0	0	0	0	FS1	FS0	00000000	RW	00: Programmable flag; 01: Empty, 10: Full, 11: reserved (PF)
E6E3	1	EP6GPIFPFSTOP	Endpoint 6 GPIF stop transaction on prog. flag	0	0	0	0	0	0	0	FIFO6FLAG	00000000	RW	
E6E4	1	EP6GPIFTRIG ***see Section 15.14***	Endpoint 6 GPIF Trigger	x	x	x	x	x	x	x	x	xxxxxxxx	W	Start GPIF transactions, duplicated in SFR - GPIFTRIG
	3	reserved												
		reserved												
		reserved												
E6EA	1	EP8GPIFFLGSEL ***see Section 15.14***	Endpoint 8 GPIF Flag select	0	0	0	0	0	0	FS1	FS0	00000000	RW	00: Programmable flag; 01: Empty, 10: Full, 11: reserved (PF)
E6EB	1	EP8GPIFPFSTOP	Endpoint 8 GPIF stop transaction on prog. flag	0	0	0	0	0	0	0	FIFO8FLAG	00000000	RW	
E6EC	1	EP8GPIFTRIG ***see Section 15.14***	Endpoint 8 GPIF Trigger	x	x	x	x	x	x	x	x	xxxxxxxx	W	Start GPIF transactions, duplicated in SFR - GPIFTRIG
	3	reserved												
E6F0	1	XGPIFSGLDATH	GPIF Data H (16-bit mode only)	D15	D14	D13	D12	D11	D10	D9	D8	xxxxxxxx	RW	duplicated in SFR space, SGLDATH / SGLDATLX / SGLDATLNOX
E6F1	1	XGPIFSGLDATLX	Read/Write GPIF Data L & trigger transaction	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW	8051read or write triggers GPIF transaction
E6F2	1	XGPIFSGLDATLNOX	Read GPIF Data L, no transaction trigger	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	R	8051 reads data w/o GPIF transaction trig. (e.g. last byte)
E6F3	1	GPIFREADYCFG	Internal RDY,Sync/Async, RDY pin states	INTRDY	SAS	TCXRDY5	0	0	0	0	0	00000000	bbbrrrrr	**INTRDY** is 8051 'ready', like RDYn pins. RDYn indicate pin states
														SAS=1: synchronous, 0:asynchronous (2-flops) RDYn inputs.
E6F4	1	GPIFREADYSTAT	GPIF Ready Status	0	0	RDY5	RDY4	RDY3	RDY2	RDY1	RDY0	00xxxxxx	R	RDYn indicate pin states
E6F5	1	GPIFABORT	Abort GPIF Waveforms	x	x	x	x	x	x	x	x	xxxxxxxx	W	Go To GPIF IDLE state. Data is don't care.
E6F6	2	reserved												
		ENDPOINT BUFFERS												
E740	64	EP0BUF	EP0-IN/-OUT buffer	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW	
E780	64	EP10UTBUF	EP1-OUT buffer	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW	
E7C0	64	EP1INBUF	EP1-IN buffer	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW	

EZ-USB FX2 Registers & Buffers

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access	Notes
	2048	reserved											RW	
F000	1024	EP2FIFOBUF	512/1024-byte EP 2 / slave FIFO buffer (IN or OUT)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW	For 512 use only 0xF000-0xF1FF
F400	512	EP4FIFOBUF	512 byte EP 4 / slave FIFO buffer (IN or OUT)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW	
F600	512	reserved												
F800	1024	EP6FIFOBUF	512/1024-byte EP 6 / slave FIFO buffer (IN or OUT)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW	For 512 use only 0xF800-0xF9FF
FC00	512	EP8FIFOBUF	512 byte EP 8 / slave FIFO buffer (IN or OUT)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW	
FE00	512	reserved												
xxxx		**I²C Compatible Configuration Byte**		0	DISCON	0	0	0	0	0	400KHZ	xxxxxxxx	n/a	
												00000000 If no EPROM detected		**DISCON**=copied into DISCON bit (USBCS.3) for power-on USB connect state **400KHZ**=1 for 400 KHz I²C compatible bus operation NOTE: if no EEPROM is connected all bits default to register default values.
		Special Function Registers (SFRs)												
80	1	IOA(1)	Port A (bit addressable)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW	
81	1	SP	Stack Pointer	D7	D6	D5	D4	D3	D2	D1	D0	00000111	RW	
82	1	DPL0	Data Pointer 0 L	A7	A6	A5	A4	A3	A2	A1	A0	00000000	RW	
83	1	DPH0	Data Pointer 0 H	A15	A14	A13	A12	A11	A10	A9	A8	00000000	RW	
84	1	DPL1(1)	Data Pointer 1 L	A7	A6	A5	A4	A3	A2	A1	A0	00000000	RW	
85	1	DPH1(1)	Data Pointer 1 H	A15	A14	A13	A12	A11	A10	A9	A8	00000000	RW	
86	1	DPS(1)	Data Pointer 0/1 select	0	0	0	0	0	0	0	SEL	00000000	RW	
87	1	PCON	Power Control	SMOD0	x	1	1	GF1	GF0	STOP	IDLE	00110000	RW	
88	1	TCON	Timer/Counter Control (bit addressable)	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00000000	RW	
89	1	TMOD	Timer/Counter Mode Control	GATE	CT	M1	M0	GATE	CT	M1	M0	00000000	RW	
8A	1	TL0	Timer 0 reload L	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW	
8B	1	TL1	Timer 1 reload L	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW	
8C	1	TH0	Timer 0 reload H	D15	D14	D13	D12	D11	D10	D9	D8	00000000	RW	
8D	1	TH1	Timer 1 reload H	D15	D14	D13	D12	D11	D10	D9	D8	00000000	RW	
8E	1	CKCON(1)	Clock Control	x	x	T2M	T1M	T0M	MD2	MD1	MD0	00000001	RW	MOVX = 3 instr. cycles (default)
8F	1	reserved												
90	1	IOB(1)	Port B (bit addressable)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW	
91	1	EXIF(1)	External Interrupt Flag(s)	IE5	IE4	I²CINT	USBNT	1	0	0	0	00001000	RW	

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Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access	Notes
92	1	MPAGE(1)	Upper Addr Byte of MOVX using @R0 / @R1	A15	A14	A13	A12	A11	A10	A9	A8	00000000	RW	used with the indirect addressing instuction(s), ie. MOVX @R0,A _where MPAGE = upper addr byte and R0 contains lower addr byte _an app. example would be to copy EP1 out/in data to a buffer
93	5	reserved												
98	1	SCON0	Serial Port 0 Control (bit addressable)	SM0_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	00000000	RW	
99	1	SBUF0	Serial Port 0 Data Buffer	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW	
9A	1	AUTOPTRH1(1)	Autopointer 1 Address H	A15	A14	A13	A12	A11	A10	A9	A8	00000000	RW	
9B	1	AUTOPTRL1(1)	Autopointer 1 Address L	A7	A6	A5	A4	A3	A2	A1	A0	00000000	RW	
9C	1	reserved												
9D	1	AUTOPTRH2(1)	Autopointer 2 Address H	A15	A14	A13	A12	A11	A10	A9	A8	00000000	RW	
9E	1	AUTOPTRL2(1)	Autopointer 2 Address L	A7	A6	A5	A4	A3	A2	A1	A0	00000000	RW	
9F	1	reserved												
A0	1	IOC(1)	Port C (bit addressable)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW	
A1	1	INT2CLR(1)	Interrupt 2 clear	x	x	x	x	x	x	x	x	xxxxxxxx	W	
A2	1	INT4CLR(1)	Interrupt 4 clear	x	x	x	x	x	x	x	x	xxxxxxxx	W	
A3	5	reserved												
A8	1	IE	Interrupt Enable (bit addressable)	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0	00000000	RW	
A9	1	reserved												
AA	1	EP2468STAT(1)	Endpoint 2,4,6,8 status flags	EP8F	EP8E	EP6F	EP6E	EP4F	EP4E	EP2F	EP2E	01011010	R	Check Empty/Full status of EP 2,4,6,8 using MOV
AB	1	EP24FIFOFLGS(1)	Endpoint 2,4 slave FIFO status flags	0	EP4PF	EP4EF	EP4FF	0	EP2PF	EP2EF	EP2FF	00100010	R	Check Prg/Empty/Full status of EP 2,4 slave FIFO using MOV instr.
AC	1	EP68FIFOFLGS(1)	Endpoint 6,8 slave FIFO status flags	0	EP8PF	EP8EF	EP8FF	0	EP6PF	EP6EF	EP6FF	01100110	R	Check Prg/Empty/Full status of EP 6,8 slave FIFO using MOV instr.
AD	2	reserved												
AF	1	AUTOPTRSETUP(1)	Autopointer 1&2 Setup	0	0	0	0	0	APTR2INC	APTR1INC	APTREN	00000110	RW	APTRxINC=1 inc autopointer(s); APTRxINC=0 freeze autopointer(s) APTREN=1 RD/WR stobes asserted when using MOVX version
B0	1	IOD(1)	Port D (bit addressable)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW	
B1	1	IOE(1)	Port E (NOT bit addressable)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW	
B2	1	OEA(1)	Port A Output Enable	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW	
B3	1	OEB(1)	Port B Output Enable	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW	
B4	1	OEC(1)	Port C Output Enable	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW	
B5	1	OED(1)	Port D Output Enable	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW	
B6	1	OEE(1)	Port E Output Enable	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW	
B7	1	reserved												

EZ-USB FX2 Registers & Buffers

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access	Notes
B8	1	IP	Interrupt Priority (bit addressable)	1	PS1	PT2	PS0	PT1	PX1	PT0	PX0	10000000	RW	
B9	1	reserved												
BA	1	EP01STAT(1)	Endpoint 0&1 Status	0	0	0	0	0	EP1INBSY	EP1OUTBSY	EP0BSY	00000000	R	Check EP0 & EP1 status using MOV instr.
BB	1	GPIFTRIG(1) ***see Section 15.14***	Endpoint 2,4,6,8 GPIF slave FIFO Trigger	DONE	0	0	0	0	RW	EP1	EP0	10000xxx	brrrrbbb	RW=1 reads, RW=0 writes; EP[1:0] = 00 EP2, = 01 EP4, = 10 EP6, = 11 EP8
BC	1	reserved												
BD	1	GPIFSGLDATH(1)	GPIF Data H (16-bit mode only)	D15	D14	D13	D12	D11	D10	D9	D8	xxxxxxxx	RW	efficient version(s) of their MOVX buddies
BE	1	GPIFSGLDATLX(1)	GPIF Data L w/ Trigger	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW	
BF	1	GPIFSGLDATLNOX(1)	GPIF Data L w/ No Trigger	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	R	note READ only, this should help you decide when to appropriately use it
C0	1	SCON1(1)	Serial Port 1 Control (bit addressable)	SM0_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1	00000000	RW	
C1	1	SBUF1(1)	Serial Port 1 Data Buffer	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW	
C2	6	reserved												
C8	1	T2CON	Timer/Counter 2 Control (bit addressable)	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	CT2	CPRL2	00000000	RW	
C9	1	reserved												
CA	1	RCAP2L	Capture for Timer 2, auto-reload, up-counter	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW	
CB	1	RCAP2H	Capture for Timer 2, auto-reload, up-counter	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW	
CC	1	TL2	Timer 2 reload L	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW	
CD	1	TH2	Timer 2 reload H	D15	D14	D13	D12	D11	D10	D9	D8	00000000	RW	
CE	2	reserved												
D0	1	PSW	Program Status Word (bit addressable)	CY	AC	F0	RS1	RS0	OV	F1	P	00000000	RW	
D1	7	reserved												
D8	1	EICON(1)	External Interrupt Control	SMOD1	1	ERESI	RESI	INT6	0	0	0	01000000	RW	RESI - reflects D+ / WU / WU2 src while SUSPEND (PCON.1), clocks off
D9	7	reserved												
E0	1	ACC	Accumulator (bit addressable)	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW	
E1	7	reserved												
E8	1	EIE(1)	External Interrupt Enable(s)	1	1	1	EX6	EX5	EX4	EI²C	EUSB	11100000	RW	
E9	7	reserved												
F0	1	B	B (bit addressable)	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW	
F1	7	reserved												
F8	1	EIP(1)	External Interrupt Priority Control	1	1	1	PX6	PX5	PX4	PI²C	PUSB	11100000	RW	
F9	7	reserved												

(1) SFRs not part of the standard 8051 architecture.