CY7C68013A, CY7C68014A
CY7C68015A, CY7C68016A

EZ-USB® FX2LP™ USB Microcontroller
High-Speed USB Peripheral Controller

Features

- USB 2.0 USB IF high speed certified (TID # 40460272)
- Single chip integrated USB 2.0 transceiver, smart SIE, and enhanced 8051 microprocessor
- Fit, form, and function compatible with the FX2
  - Pin compatible
  - Object code compatible
  - Functionally compatible (FX2LP is a superset)
- Ultra low power: I_{CC} No more than 85 mA in any mode
  - Ideal for bus and battery powered applications
- Software: 8051 code runs from:
  - Internal RAM, which is downloaded through USB
  - Internal RAM, which is loaded from EEPROM
  - External memory device (128 pin package)
- 16 KB of on-chip code/data RAM
- Four programmable BULK, INTERRUPT, and ISOCHRONOUS endpoints
  - Buffering options: Double, triple, and quad
- Additional programmable (BULK/INTERRUPT) 64-byte endpoint
- 8-bit or 16-bit external data interface
- Smart media standard ECC generation
- GPIF (general programmable interface)
  - Enables direct connection to most parallel interfaces
  - Programmable waveform descriptors and configuration registers to define waveforms
  - Supports multiple ready (RDY) inputs and Control (CTL) outputs
- Integrated, industry standard enhanced 8051
  - 48 MHz, 24 MHz, or 12 MHz CPU operation
  - Four clocks per instruction cycle
  - Two USARTs
  - Three counter/timers
  - Expanded interrupt system
  - Two data pointers
- 3.3 V operation with 5 V tolerant inputs
- Vectored USB interrupts and GPIF/FIFO interrupts
- Separate data buffers for the setup and data portions of a CONTROL transfer
- Integrated I^2C controller, runs at 100 or 400 kHz
- Four integrated FIFOs
  - Integrated glue logic and FIFOs lower system cost
  - Automatic conversion to and from 16-bit buses
  - Master or slave operation
  - Uses external clock or asynchronous strobes
  - Easy interface to ASIC and DSP ICs
- Available in commercial and industrial temperature grade (all packages except VFBGA)

Features (CY7C68013A/14A only)

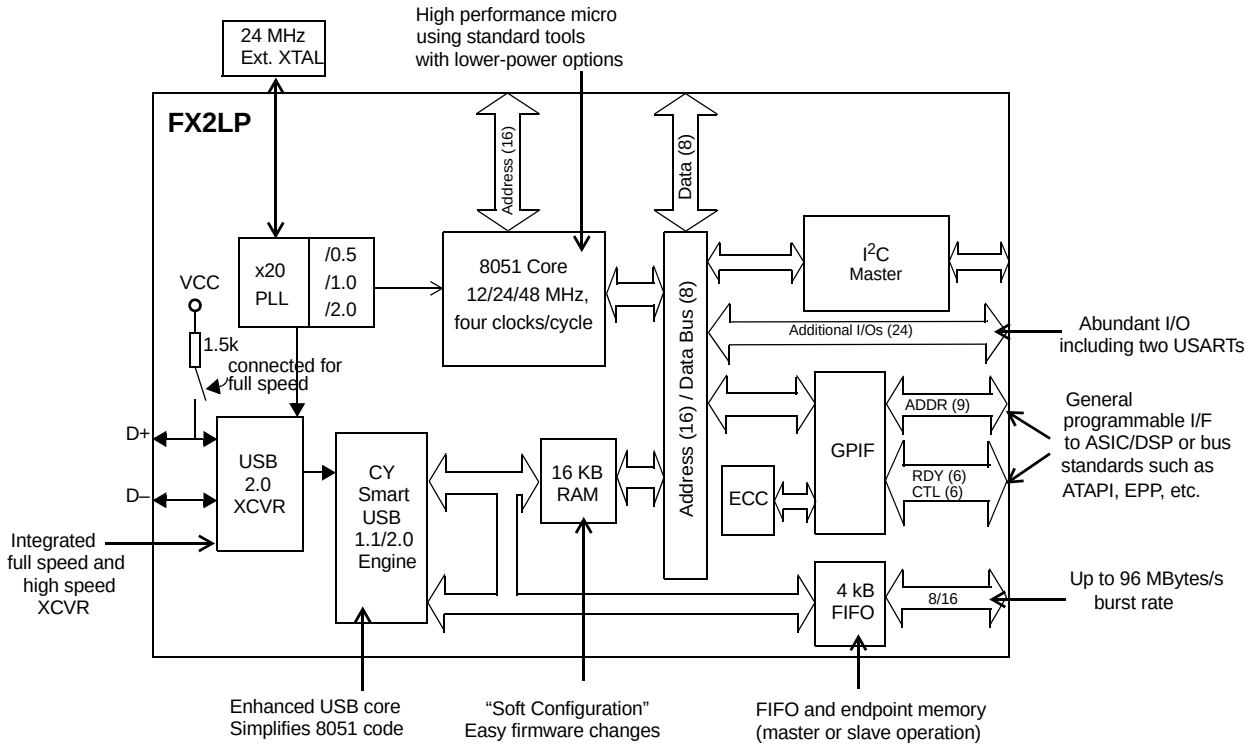
- CY7C68014A: Ideal for Battery Powered Applications
  - Suspend current: 100 µA (typ)
- CY7C68013A: Ideal for Non Battery Powered Applications
  - Suspend current: 300 µA (typ)
- Available in Five Pb-free Packages with Up to 40 GPIOs
  - 128-pin TQFP (40 GPIOs), 100-pin TQFP (40 GPIOs), 56-pin QFN (24 GPIOs), 56-pin SSOP (24 GPIOs), and 56-pin VFBGA (24 GPIOs)

Features (CY7C68015A/16A only)

- CY7C68016A: Ideal for Battery Powered Applications
  - Suspend current: 100 µA (typ)
- CY7C68015A: Ideal for Non Battery Powered Applications
  - Suspend current: 300 µA (typ)
- Available in Pb-free 56-pin QFN Package (26 GPIOs)
- Two more GPIOs than CY7C68013A/14A enabling additional features in same footprint

Errata: For information on silicon errata, see "Errata" on page 64. Details include trigger conditions, devices affected, and proposed workaround.

Logic Block Diagram



Cypress's EZ-USB® FX2LP™ (CY7C68013A/14A) is a low power version of the EZ-USB FX2™ (CY7C68013), which is a highly integrated, low power USB 2.0 microcontroller. By integrating the USB 2.0 transceiver, serial interface engine (SIE), enhanced 8051 microcontroller, and a programmable peripheral interface in a single chip,

Cypress has created a cost effective solution that provides superior time-to-market advantages with low power to enable bus powered applications.

The ingenious architecture of FX2LP results in data transfer rates of over 53 Mbytes per second, the maximum allowable USB 2.0 bandwidth, while still using a low cost 8051 microcontroller in a package as small as a 56 VFBGA (5 mm x 5 mm). Because it incorporates the USB 2.0 transceiver, the FX2LP is more economical, providing a smaller footprint solution than USB 2.0 SIE or external transceiver implementations. With EZ-USB FX2LP, the Cypress Smart SIE handles most of the USB 1.1 and 2.0 protocol in hardware, freeing the embedded microcontroller for application specific functions and decreasing development time to ensure USB compatibility.

The General Programmable Interface (GPIF) and Master/Slave Endpoint FIFO (8-bit or 16-bit data bus) provides an easy and glueless interface to popular interfaces such as ATA, UTOPIA, EPP, PCMCIA, and most DSP/processors.

The FX2LP draws less current than the FX2 (CY7C68013), has double the on-chip code/data RAM, and is fit, form and function compatible with the 56, 100, and 128 pin FX2.

Five packages are defined for the family: 56 VFBGA, 56 SSOP, 56 QFN, 100 TQFP, and 128 TQFP.

Contents

1. Applications

- Portable video recorder
- MPEG/TV conversion
- DSL modems
- ATA interface
- Memory card readers
- Legacy conversion devices
- Cameras
- Scanners
- Wireless LAN
- MP3 players
- Networking

The “Reference Designs” section of the Cypress web site provides additional tools for typical USB 2.0 applications. Each reference design comes complete with firmware source and object code, schematics, and documentation. Visit www.cypress.com for more information.

2. Functional Overview

2.1 USB Signaling Speed

FX2LP operates at two of the three rates defined in the USB Specification Revision 2.0, dated April 27, 2000:

- Full speed, with a signaling bit rate of 12 Mbps
- High speed, with a signaling bit rate of 480 Mbps

FX2LP does not support the low speed signaling mode of 1.5 Mbps.

2.2 8051 Microprocessor

The 8051 microprocessor embedded in the FX2LP family has 256 bytes of register RAM, an expanded interrupt system, three timer/counters, and two USARTs.

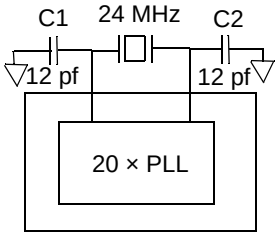
2.2.1 8051 Clock Frequency

FX2LP has an on-chip oscillator circuit that uses an external 24 MHz (±100 ppm) crystal with the following characteristics:

- Parallel resonant
- Fundamental mode
- 500 µW drive level
- 12 pF (5% tolerance) load capacitors

An on-chip PLL multiplies the 24 MHz oscillator up to 480 MHz, as required by the transceiver/PHY and internal counters divide it down for use as the 8051 clock. The default 8051 clock frequency is 12 MHz. The clock frequency of the 8051 can be changed by the 8051 through the CPUCS register, dynamically.

Figure 2-1. Crystal Configuration



12 pF capacitor values assumes a trace capacitance of 3 pF per side on a four-layer FR4 PCA

The CLKOUT pin, which can be three-stated and inverted using internal control bits, outputs the 50% duty cycle 8051 clock, at the selected 8051 clock frequency: 48 MHz, 24 MHz, or 12 MHz.

2.2.2 USARTs

FX2LP contains two standard 8051 USARTs, addressed through Special Function Register (SFR) bits. The USART interface pins are available on separate I/O pins, and are not multiplexed with port pins.

UART0 and UART1 can operate using an internal clock at 230 KBaud with no more than 1% baud rate error. 230 KBaud operation is achieved by an internally derived clock source that generates overflow pulses at the appropriate time. The internal clock adjusts for the 8051 clock rate (48 MHz, 24 MHz, and 12 MHz) such that it always presents the correct frequency for 230 KBaud operation.[1]

2.2.3 Special Function Registers

Certain 8051 SFR addresses are populated to provide fast access to critical FX2LP functions. These SFR additions are shown in Table 1 on page 5. Bold type indicates non standard, enhanced 8051 registers. The two SFR rows that end with “0” and “8” contain bit addressable registers. The four I/O ports A to D use the SFR addresses used in the standard 8051 for ports 0 to 3, which are not implemented in FX2LP. Because of the faster and more efficient SFR addressing, the FX2LP I/O ports are not addressable in external RAM space (using the MOVX instruction).

2.3 I^2C Bus

FX2LP supports the I^2C bus as a master only at 100/400 KHz. SCL and SDA pins have open-drain outputs and hysteresis inputs. These signals must be pulled up to 3.3V, even if no I^2C device is connected.

2.4 Buses

All packages, 8-bit or 16-bit “FIFO” bidirectional data bus, multiplexed on I/O ports B and D. 128-pin package: adds 16-bit output-only 8051 address bus, 8-bit bidirectional data bus.

Note
1. 115-KBaud operation is also possible by programming the 8051 SMOD0 or SMOD1 bits to a “1” for UART0, UART1, or both respectively.

Table 1. Special Function Registers

x	8x	9x	Ax	Bx	Cx	Dx	Ex	Fx
0	**IOA**	**IOB**	**IOC**	**IOD**	SCON1	PSW	ACC	B
1	SP	**EXIF**	**INT2CLR**	**IOE**	SBUF1	–	–	–
2	DPL0	**MPAGE**	**INT4CLR**	**OEA**	–	–	–	–
3	DPH0	–	–	**OEB**	–	–	–	–
4	**DPL1**	–	–	**OEC**	–	–	–	–
5	**DPH1**	–	–	**OED**	–	–	–	–
6	**DPS**	–	–	**OEE**	–	–	–	–
7	PCON	–	–	–	–	–	–	–
8	TCON	SCON0	IE	IP	T2CON	**EICON**	**EIE**	**EIP**
9	TMOD	SBUF0	–	–	–	–	–	–
A	TL0	**AUTOPTRH1**	**EP2468STAT**	**EP01STAT**	RCAP2L	–	–	–
B	TL1	**AUTOPTRL1**	**EP24FIFOFLGS**	**GPIFTRIG**	RCAP2H	–	–	–
C	TH0	**reserved**	**EP68FIFOFLGS**		TL2	–	–	–
D	TH1	**AUTOPTRH2**	–	**GPIFSGLDATH**	TH2	–	–	–
E	**CKCON**	**AUTOPTRL2**	–	**GPIFSGLDATLX**	–	–	–	–
F	–	**reserved**	**AUTOPTRSET-UP**	**GPIFSGLDATLNOX**	–	–	–	–

2.5 USB Boot Methods

During the power up sequence, internal logic checks the I^2C port for the connection of an EEPROM whose first byte is either 0xC0 or 0xC2. If found, it uses the VID/PID/DID values in the EEPROM in place of the internally stored values (0xC0), or it boot-loads the EEPROM contents into internal RAM (0xC2). If no EEPROM is detected, FX2LP enumerates using internally stored descriptors. The default ID values for FX2LP are VID/PID/DID (0x04B4, 0x8613, 0xAxxx where xxx = Chip revision).[2]

Table 2. Default ID Values for FX2LP

Default VID/PID/DID		
Vendor ID	0x04B4	Cypress Semiconductor
Product ID	0x8613	EZ-USB FX2LP
Device release	0xAnnn	Depends on chip revision (nnn = chip revision where first silicon = 001)

2.6 ReNumeration

Because the FX2LP's configuration is soft, one chip can take on the identities of multiple distinct USB devices.

When first plugged into USB, the FX2LP enumerates automatically and downloads firmware and USB descriptor tables over the USB cable. Next, the FX2LP enumerates again, this time as a device defined by the downloaded information. This patented two step process called ReNumeration™ happens instantly when the device is plugged in, without a hint that the initial download step has occurred.

Two control bits in the USBCS (USB Control and Status) register, control the ReNumeration process: DISCON and RENUM. To simulate a USB disconnect, the firmware sets DISCON to 1. To reconnect, the firmware clears DISCON to 0.

Before reconnecting, the firmware sets or clears the RENUM bit to indicate whether the firmware or the Default USB Device handles device requests over endpoint zero: if RENUM = 0, the Default USB Device handles device requests; if RENUM = 1, the firmware services the requests.

2.7 Bus-Powered Applications

The FX2LP fully supports bus powered designs by enumerating with less than 100 mA as required by the USB 2.0 specification.

2.8 Interrupt System

2.8.1 INT2 Interrupt Request and Enable Registers

FX2LP implements an autovector feature for INT2 and INT4. There are 27 INT2 (USB) vectors, and 14 INT4 (FIFO/GPIF) vectors. See EZ-USB Technical Reference Manual (TRM) for more details.

2.8.2 USB Interrupt Autovectors

The main USB interrupt is shared by 27 interrupt sources. To save the code and processing time that is required to identify the individual USB interrupt source, the FX2LP provides a second level of interrupt vectoring, called Autovectoring. When a USB interrupt is asserted, the FX2LP pushes the program counter to its stack, and then jumps to the address 0x0043 where it expects to find a "jump" instruction to the USB Interrupt service routine.

Note
2. The I^2C bus SCL and SDA pins must be pulled up, even if an EEPROM is not connected. Otherwise this detection method does not work properly.

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